Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5-D ICs

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***Abstract*— In this article, we present an effective methodology for co-design, co-analysis, and the system-level optimization of chiplet/interposer power delivery network (PDN) in 2.5-D integrated chip (IC) designs. In our methodology, we first generate a commercial-grade heterogeneous 2.5-D IC designs including full signal routing and power delivery. We then perform our PDN co-analysis in frequency and time domains on the entire PDN to evaluate various mechanisms added to our PDN designs. Based on our co-analysis results, we perform the system-level optimization on both interposer and chiplet PDNs with the stable performance of power delivery. Finally, we perform power, performance, and area (PPA) analysis and power integrity (PI) on our 2.5-D designs and discuss tradeoffs in chiplet and interposer levels due to PDN optimization. Our experiments show 27.17% improvement in the overall IR-drop in the optimized 2.5-D IC design by increasing the interposer PDN occupancy by 5.52% and inserting the additional PDN grids in chiplet designs. However, we also observe tradeoffs in terms of PPA and PI. By PDN optimization, the optimized design has an 11.6% increase of the total power, while the area of 2.5-D design remains the same. Moreover, from the perspective of PI, the tradeoffs are shown by 0.6% reduction of power efficiency, 32.6% higher output ripple, and 31.5% higher initial ringing because of an inductive behavior of interposer PDN in the optimized design.**

***Index Terms*— Electronic design automation (EDA) flow, interposer-based 2.5-D integrated chip (IC), power delivery network (PDN) co-design.**

I. Introduction

AS THE process technology scales continuously and the design complexity of system-on-chip (SoC) increases, traditional monolithic 2-D integrated chip (IC) designs are no longer able to follow Moore's law [1]. Moreover, in the case of the latest process, 2-D IC design has become difficult to meet the rapid increase in demand for high performance because design time cost has increased due to the complex design rules. Particularly in FinFET technologies, the complexity of the transistor has increased, requiring difficult and high-cost fabrication techniques, as well as yield and additional wafer cost problem [2].

2.5-D IC technology has gained a lot of traction lately as a promising candidate to redeem the limitations of existing 2-D ICs [3]. Moreover, Intel's recent FOVEROS technology indicates that the 2.5-D IC technology is no longer an alternative to the traditional 2-D ICs, but a new trend in SoC design. Unlike a monolithic 2-D IC design, interposer-based 2.5-D IC design divides a single SoC into several functional blocks, named "chiplet," and integrates chiplets onto the interposer layer. All interconnections between chiplets are implemented in the interposer layer to achieve high speed and throughput while avoiding off-chip communication.

This architecture enables not only the reuse of existing IP blocks but also heterogeneous integration using proper environments for each chiplet. This approach significantly reduces the design time and complexity by re-utilizing pre-designed chiplets as plug-and-play modules. Moreover, the system update is simplified compared with monolithic 2-D IC design because SoC designers can replace only the necessary chiplets instead of redesigning the entire SoC.

A well-optimized power delivery network (PDN) in 2.5-D IC design is fundamental to maximize the benefits of 2.5-D integration. As the clock speed tends to reach the GHz region, the PDN impedance needs to be characterized accurately over a large bandwidth to capture switching noise generated by ICs which can cause signal integrity (SI) issues. Moreover, the interposer PDN affects IR-drop on chiplet designs and vice versa due to its impedance. Unlike the ideal case, the actual level of supply voltage at each chiplet is lower than the value defined in the technology specification because the powers are supplied to chiplets through the interposer PDN. Therefore, a thorough analysis on 2.5-D PDN combining both interposer and chiplet PDNs should be performed to guarantee the performance of the 2.5-D IC design.

In this article, we claim the following novelty and contributions.

1) Our study is based on commercial-grade large-scale graphic design system (GDS) designs for both chiplets

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and interposers that feature full chiplet and full interposer signal and power delivery routing. Our chiplets are designed with multiple commercial technology nodes (=heterogeneous), and our interposer design is a result of TSMC technology.

2) We provide a comprehensive discussion of power, performance, area (PPA) versus power integrity (PI) tradeoffs that exist in heterogenous 2.5-D designs. Our PPA calculations are conducted with commercial electronic design automation (EDA) tools. Our multi-domain PI analysis is based on static IR-drop analysis, S-parameter analysis, and time-domain transient simulations to offer holistic perspectives.
3) We co-design, co-analyze, and co-optimize our chiplet and interposer PDNs. Our chiplet PDNs are optimized based on interposer PDN analysis, vice versa. We deploy integrated voltage regular (IVR) chiplets that provide stable currents to logic, memory, and communication chiplets, while maximizing power efficiency and response time. Our embedded passives are further optimized to keep the overall system-level PI high quality.
4) Our study shows that PPA and PI have to be traded off at both chiplet and interposer-level designs to strike a balance between the two overarching goals. A key part of this tradeoff study is to quantify the tradeoffs with high-quality designs and high-fidelity simulation results.

Our attempt to compare with existing work was not successful, mainly because none of them: 1) uses a full-system 2.5-D benchmark, 2) uses GDS layouts and sign-off PPA and PI simulations for both chiplets and their interposer, and 3) discusses PPA versus PI tradeoffs as ours.

II. Related Work

In a silicon interposer, the solid power and ground (P/G) plane cannot be fabricated unlike a package or printed circuit board (PCB). Previous studies have focused on mesh-type interposer PDN [4], [5] and discussed how to simplify the modeling and improve the analysis result of the interposer PDN.

Kim *et al.* [4] have proposed models for silicon interposer PDNs and through-silicon-via (TSV)-based stacked grid-type PDNs using a segmentation method. They have first modeled all transmission line sections which form the PDNs to RLGC-lumped models using a conformal mapping method and a phenomenological loss equivalence method (PEM). Using these verified models, they have estimated and analyzed a PDN impedance curve with various configurations of interposer PDN. Moreover, Cho *et al.* [5] have proposed the modeling methodology for the perforated P/G planes including substrate effects and multiarray TSVs for the first time. They have converted the perforated planes to solid planes with a dielectric mixture. As the perforated PDN consists of a periodic grid structure, they have designed and analyzed the unit cell of interposer PDN. With a small size of unit cell structure, they have obtained the model of the PDN impedance for a silicon interposer rapidly. However, those articles are only focused on the interposer PDN side. Therefore, their works are overly simplified and lack the analysis of interchiplet integration and interaction.

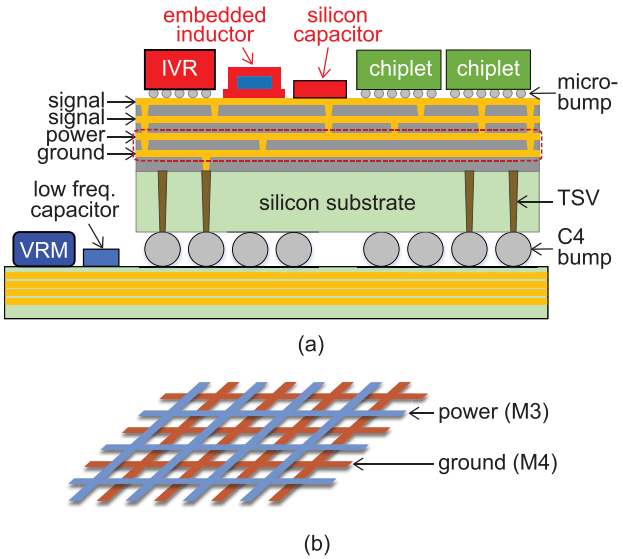

Fig. 1. Vertical stack-up and power delivery configuration of our 2.5-D IC. (a) Vertical stack-up of our 2.5-D IC. (b) Mesh-type PDN.

Zhang *et al.* [6] have proposed a PDN modeling framework for heterogeneous integration platform including 2.5-D systems. In this article, the distributed PDN is modeled as two layers and each node in the two layers is connected to six adjacent nodes using a resistor–inductor pairs. Based on this modeling method, the author has performed the design space exploration (DSE) of 2.5-D integration with various analysis results including IR-drop and transient analysis. However, their models are not entirely derived from commercial-grade 2.5-D design, the models are losing accuracy even with the analysis results in various aspects.

In this article, therefore, we suggest an interposer PDN design and analysis framework based on the commercial-grade 2.5-D IC designs. Moreover, we apply this framework to optimize the PDN designs of both chiplet and silicon interposer.

III. Benchmark and Technology Specs

We choose ROCKET-64 [7], which is a 64-core RISC-V processor, as our benchmark architecture. The vertical stack-up view of our 2.5-D IC design is shown in Fig. 1. We add four integrated voltage regulator (IVR) chiplets on the interposer to provide up to 12 A of current to our 2.5-D IC. Our IVR chiplet converts the external supply voltage of 3.6 V to the internal supply voltage of 0.9 V for our 28-nm chiplets. The converted supply voltage is fed to each chiplet through a mesh-type interposer PDN. An embedded solenoidal inductor with nickel-zinc (NiZn) ferrite magnetic core [8] and the low profile silicon capacitor are chosen for LC filter of the IVR chiplet.

As the design complexity of chiplet increases, dense interposers with fine pitch RDLs and micro-bumps are required to handle high I/O counts and the increasing number of interconnections between chiplets. Therefore, we choose a silicon interposer with 0.8-μm fine pitch RDLs and 40-μm-pitch micro-bumps for our benchmark. The design rules for our interposer design in this work are shown in Table I based on TSMC CoWoS technology [3]. We utilize a mesh-type PDN, which is more common in on-chip design, in our interposer design. The width and spacing of PDN are 40 and 100 μm for the initial 2.5-D IC design, and M3 and M4 layers are reserved for the interposer PDN mesh.

TABLE I
INTERPOSER DESIGN RULES BASED ON TSMC COWOS 65 nm. WE DO NOT CHANGE THESE SPECS IN THIS WORK EXCEPT PDN WIDTH/SPACING

Design rule	Value
Metal layer #	4
Metal thickness	$1\mu m$
Dielectric thickness	$1\mu m$
Min. line width/spacing	$0.4\mu m/0.4\mu m$
Via size	$0.7\mu m$
Through-Silicon-Via (TSV) size/depth	$10\mu m/100\mu m$
Die-to-die spacing	$100\mu m$
micro-bump pitch	$40\mu m$
C4 bump pitch	$400\mu m$
PDN width/spacing	$40\mu m/100\mu m$

IV. CO-DESIGN FOR PPA

A. Overview of the Design Flow

Fig. 2 shows the overall flow of the interposer-based 2.5-D IC design and the entire analysis on the 2.5-D system using commercial tools. We first generate the complete interposer and chiplet designs including PDNs. From our commercial-grade designs, we create an interposer PDN model using Ansys HFSS, a parameterized interposer transmission line model and behavioral chiplet models. We conduct PDN co-analysis and optimization, and PI analysis in frequency and time domains for the interposer and chiplet PDNs using these models. Finally, we perform a PPA analysis of our 2.5-D IC design to validate its performance.

In the interposer design step, we generate the full GDS layout of the interposer including the footprint of each chiplet and the routing information between chiplets. From the interposer design, we extract the wirelength distribution of interposer wires for the timing analysis. The interposer channels are then characterized with corresponding dimensions using Ansys HFSS. Next, we extract S-parameters of channels defining the impedance and coupling profile and convert those to SPICE models using Keysight ADS. Moreover, we generate the interposer PDN model in S-parameter and RLGC formats using MATLAB for our PDN co-analysis which will be discussed in Section V-A.

As the interposer design has a wide range of wirelengths, it is essential to optimize the design of the I/O driver to achieve high data rates. Therefore, we optimize I/O driver design according to the wirelength distribution of interposer with SPICE models of interposer channels generated by Lee *et al.* [9]. With the well-optimized I/O driver design, we generate physical layouts of chiplets in the chiplet design step. We use Cadence Innovus to perform place-and-route (P&R) of chiplets.

B. PPA Co-Analysis Methodology

Full-chip timing and PPA analysis of individual chiplets are straightforward and done with Synopsis PrimeTime after their layouts are constructed. Once our interchiplet I/O drivers are built and chosen to handle the given interconnect length, we calculate their propagation delays and power consumptions using their SPICE models. We then add these values to chiplet delay and power data. Our interposer interconnects are

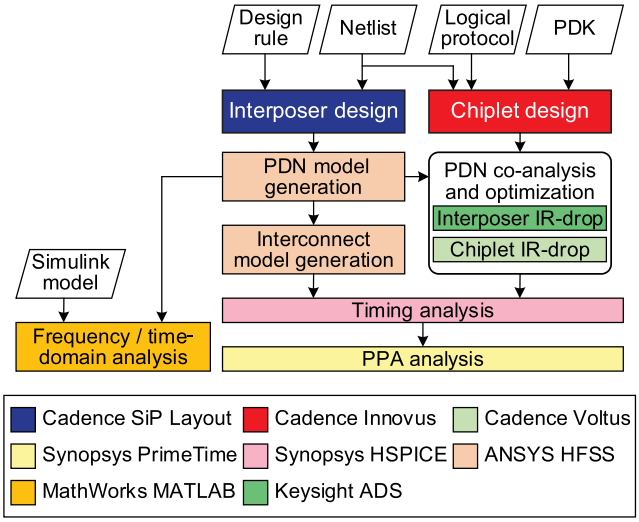

Fig. 2. Our chiplet/interposer co-design and co-analysis flow using commercial tools.

pipelined due to the flip-flops inside the I/O drivers, which simplifies timing calculation for the entire interposer design.

We perform timing analysis for our 2.5-D designs by generating a transmission line model of the interposer interconnect channel. We first generate S-parameter models of interposer transmission lines using Anysys HFSS from the wirelength distribution of interposer and convert these models to SPICE models with RLGC values using the broadband SPICE generator of Keysight ADS. We perform delay analysis of all the interconnect channels in the design by incorporating the corresponding RLGC models into HSPICE circuit simulations. We obtain the worst case propagation delay as 85.20 ps. As our design is targeted to run at a frequency of 1 GHz, this longest propagation delay is well within the limits to meet the setup and hold times of the receiver.

In our 2.5-D power analysis, we obtain the power consumption of each chiplet by using Synopsys PrimeTime and the AIB drivers from HSPICE simulations. Since the effect of the interposer wire on power estimation is not reflected in logic synthesis tool, we estimate the total power of our designs as described in [7] with the additional power loss of power management modules

$$P_{2.5D} = P_{\text{CORE}} + P_{\text{I/O}} + P_{\text{PM}} \tag{1}$$

where $P_{2.5\text{-D}}$ is the total power of 2.5-D IC design, P_{CORE} is the power of logic chiplets, $P_{\text{I/O}}$ is the power of AIBs, and P_{PM} is the power loss of IVR chiplets. Detailed analysis results of 2.5-D IC design including PPA are shown in Table VI as Design 1, and the thorough discussion is given in Section VI.

C. Chiplet Design Results

During our chipletization step, we perform P&R using Cadence Innovus as the physical design tool. The interchiplet interface protocol for 2.5-D system is important because each chiplet can use a different protocol and a standardized protocol is needed to allow easy system design and verification. Common protocols such as AXI and TileLink are not ideal due to their large I/O count which significantly increases the area

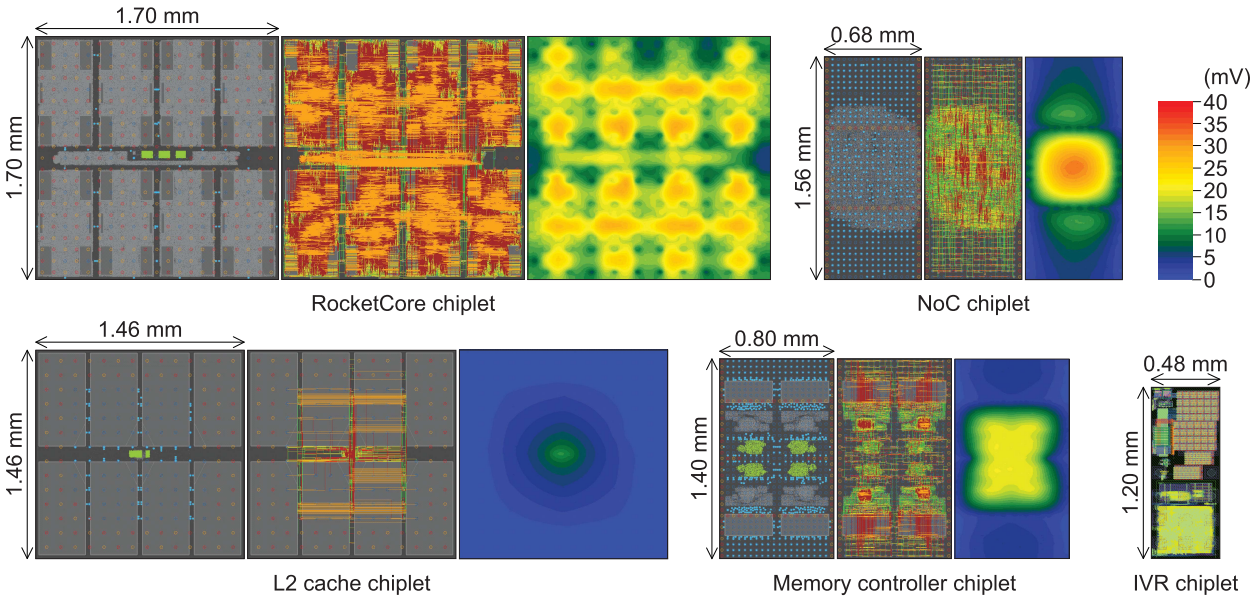

Fig. 3. Floorplan, GDS layout and IR-drop map of each chiplet. The green part shows protocol translator/bridge logic, and the blue part I/O driver. Chiplets except IVR are implemented in 28 nm, and IVR in 130 nm.

in 2.5-D IC designs, therefore, we choose Hybrid-Link [7] as our protocol interface. Hybrid-Link reduces the I/O count to a flit size of 40 and enables flexible functionality for various chiplets.

Moreover, special interchiplet I/O drivers are necessary for each input and output to drive the signals without any loss because the interposer wires have larger dimensions and longer wirelength compared to the on-chip wires. Based on interposer transmission line models from our interposer design, we optimize the size of I/O driver to meet the timing constraint. In this article, we choose Intel's Advanced Interface Bus (AIB) [10] as our I/O driver.

In chiplet P&R step, we add a minimum of 100 P/G bumps to each chiplet to ensure PI across the chiplet. However, in the case of chiplets with an aspect ratio of less than 0.5, such as NoC chiplet, we insert additional P/G bumps in the middle of the chiplet to avoid a high IR-drop in the chiplet power rail. To minimize the distance from AIB to the signal bump, we use the area I/O placement method [11] in our chiplets. With a well-defined micro-bump assignment, the tool places AIBs at the proper positions to meet the timing constraint.

GDS layouts of chiplets with 1-GHz target frequency are shown in Fig. 3. We choose a commercial 28 nm (logic chiplets) and a commercial 130 nm (IVR chiplet) as the technology nodes for our chipletization. In chiplet designs, M5 and M6 layers, which are top two metal layers, are used to generate the power grid for the chiplet PDN. We set the maximum utilization of chiplet PDN as 20%, and allow the maximum IR-drop up to 5% of the supply voltage which is 45 mV. Fig. 3 and Table II show the rail IR-drop analysis results that meet all constraints.

D. Interposer Design Results

GUI-based floorplanning and interposer routing are done using Cadence SiP Layout XL. We first setup technology file including design rules as shown in Table I, which provides

TABLE II
CHIPLETIZATION RESULTS INCLUDING PDN IR-DROP ANALYSIS. WE USE 0.9 V FOR THE SUPPLY VOLTAGE

	Rocket	L2 cache	NoC	Memory controller
Cell count (#)	923,764	3,670	80,986	52,074
Worst slack (ps)*	90.81	120.78	113.17	97.99
Total power (mW)	1,034.83	18.52	68.05	45.50
PDN M5/6 width (μm)	0.45	0.45	0.45	0.45
PDN M5/6 pitch (μm)	5.0	5.0	5.0	5.0
PDN utilization (%)	18.05	18.02	18.04	18.04
Worst IR-drop (mV)	29.51	12.42	32.94	21.20
IR-drop/Vdd (%)	3.28	1.38	3.66	2.36

* The positive slack is used in the table.

physical and electrical information. We place all chiplets and passive components on the top side of the interposer, and all C4 bumps at the bottom as shown in Fig. 4. For passive components, we choose the solenoidal inductor with NiZn ferrite magnetic core and integrate on the top metal layer of interposer. Our embedded inductor is designed with the inductance of 25 nH and the saturation current of 3 A due to the limited area of the silicon interposer. We also choose the silicon capacitor which has the capacitance of 200 nF and a low profile up to 80 μm due to the height of the package. Considering the IVR configuration with inductor and capacitor, we place both inductors and capacitors closest to the corresponding IVR chiplets.

In the routing step, we perform Manhattan routing similar to the on-chip routing for all interconnections of the interposer layer using the Automatic Router in Cadence SiP Layout XL. As the wires between chiplets reach several millimeters, the data skew problem should be considered thoroughly. To avoid this issue, we set a design constraint, named match group (MG), as 500 μm to limit the wirelength deviation. This causes less than 5 ps of propagation delay variation between nets in a single bus. The wirelength variation of one example

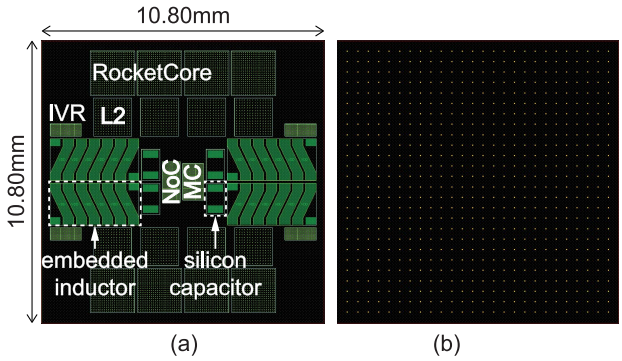

Fig. 4. Floorplan of our interposer design: top and bottom sides. (a) Top side (chiplets). (b) Bottom side (C4 bumps).

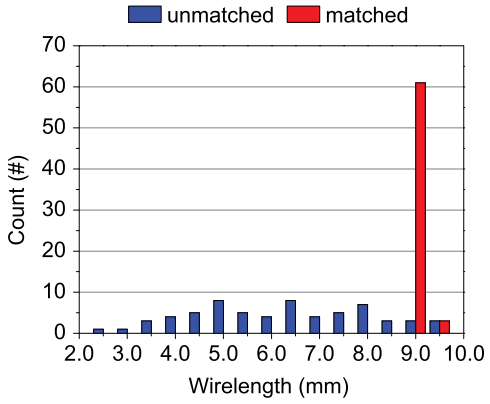

Fig. 5. Effect of MG on the wirelength of a single bus.

TABLE III
DESIGN RESULTS OF THE INTERPOSER SHOWN IN FIG. 6

Area (mm^2)	116.64
Routed net #	1,420
Metal layers used	4
Min wirelength (mm)	0.14
Ave wirelength (mm)	2.83
Max wirelength (mm)	6.97
Via usage	5,518
PDN occupancy (%)	61.65

bus in our interposer design is reduced from 6960 to 500 μm as shown in Fig. 5 with MG constraint.

Our silicon interposer design results are shown in Fig. 6 and Table III. A total of 1420 nets are routed through the silicon interposer layer and four metal layers are used. Our interposer PDN utilizes the lower two metal layers with the width and pitch shown in Table I, and occupies 61.65% of the design area. The maximum wirelength of interposer wire is 6.97 mm and the design area is 116.64 mm^2 with 676 of C4 bumps at the bottom.

V. CO-DESIGN FOR PI

A. Overview of the Design and Optimization Flow

The chiplet/interposer IR-drop co-analysis and co-optimization flow, which is one of the key features in our flow, is shown in Fig. 7. As the supply voltage (Vdd) of each chiplet is delivered through the interposer PDN, the voltage drops between the supply sources and chiplets should be considered carefully. These IR-drops affect the performance of chiplets, therefore, the IR-drop analysis is essential in 2.5-D design.

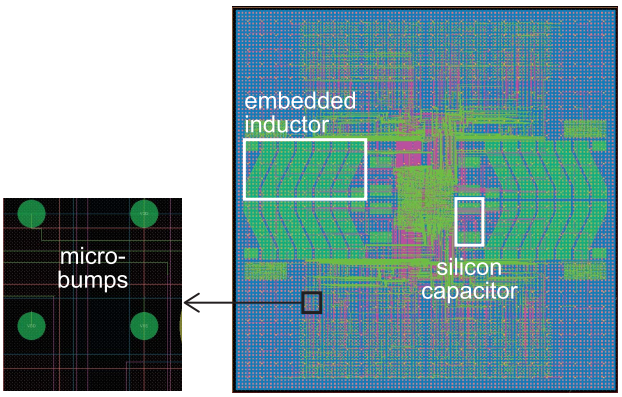

Fig. 6. Chiplet placement and routing results (GDS layout) of the silicon interposer shown in Fig. 1.

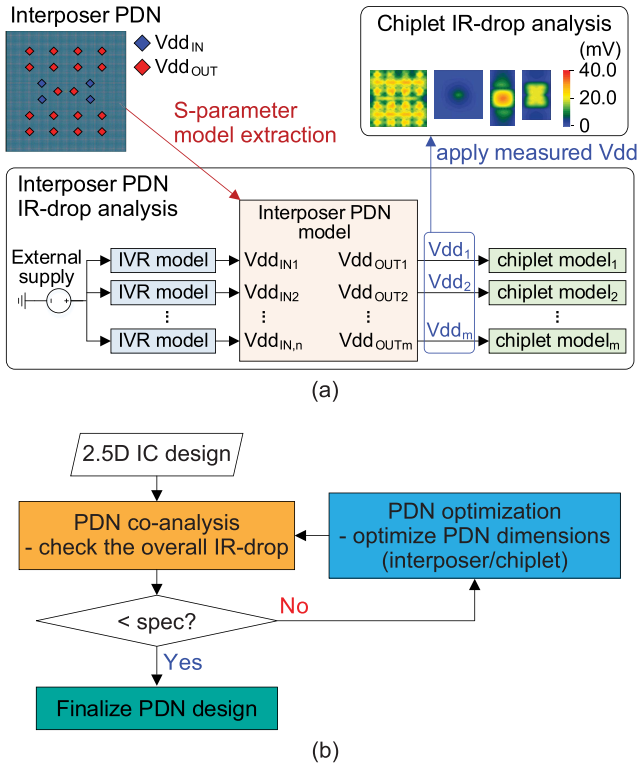

Fig. 7. Our chiplet/interposer PDN co-analysis and the system-level optimization flow. (a) 2.5-D PDN co-analysis flow. (b) Feedback loop of PDN optimization.

In our co-analysis flow, we perform IR-drop simulation of chiplets considering interposer PDN to show the effect of IR-drop from interposer PDN. First, we generate S-parameter model of the interposer PDN with multiple input and output ports using MATLAB. Then, we run time-domain simulation with IVR and chiplet models to obtain Vdd level of each chiplet using Keysight ADS. Finally, we analyze the effect of voltage drop on chiplet performance by performing IR-drop analyses of chiplets using Cadence Voltus.

We also perform PDN optimization to improve the overall IR-drop of 2.5-D IC design. From our PDN co-analysis result, we adjust the ratio of the interposer and chiplet out of the overall IR-drop and decide which part of PDN should be further improved. We optimize the physical dimensions of each interposer PDN and chiplet PDN to achieve the optimal

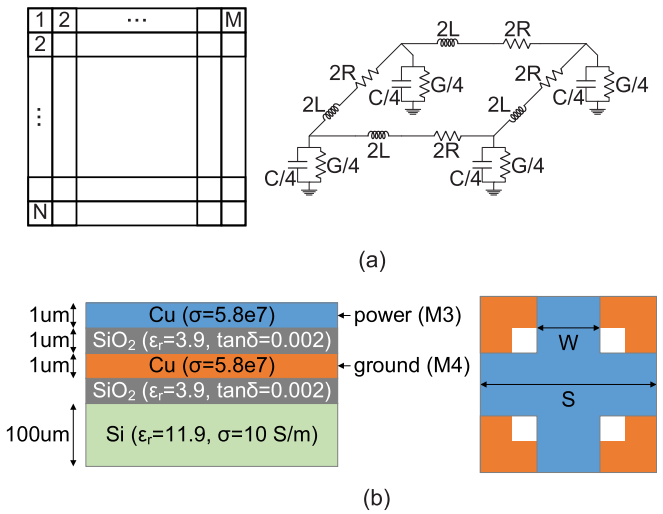

Fig. 8. Mesh-type silicon interposer PDN model used in our analysis. (a) Unit cell view. (b) Interposer PDN unit cell.

qualities of PDN designs and meet the power specification of our 2.5-D system.

B. Interposer PDN Modeling Methodology

For power delivery in silicon interposer, we adopt a mesh-type PDN, which is commonly used for on-chip power delivery solutions. As the clock frequency increases to GHz region, modeling and analyzing interposer PDN require significant computing resources because the P/G mesh becomes a large structure. In this work, we choose transmission matrix method (TMM) [12] to divide the interposer PDN mesh into $M \times N$ unit cells, each of which is modeled as a lumped Π model that consists of R, L, G, and C as shown in Fig. 8(a). They are obtained as follows:

$$R = R_s \cdot \left(\frac{S}{4W}\right) \tag{2}$$

$$L = S\left[0.13\epsilon^{(-S/45)} + 0.14\ln\left(\frac{S}{W}\right) + 0.07\right] \tag{3}$$

$$C_i = \frac{\epsilon_r}{10^3}\left[(44-28H)W^2 + (280+0.8S-64)W \cdots\cdots + 12S - 1500H + 1700\right] \tag{4}$$

$$C_f = \epsilon_0\epsilon_r 10^9\left[\frac{4SW\left(\ln\frac{S}{S'} + e^{-1/3}\right)}{W\pi + 2H\left(\ln\left(\frac{S}{S'} + e^{-1/3}\right)\right)} + \frac{2S}{\pi}\sqrt{\frac{2H}{S'}}\right] \tag{5}$$

$$C = C_i + C_f \tag{6}$$

$$G = 2\pi \cdot f \cdot C \cdot \tan(\delta) \tag{7}$$

where R_s is surface resistance, W and S are the width/spacing of PDN mesh as shown in Fig. 8(b), $S' = S - 2W$, H is the separation between P/G layer, and $\tan(\delta)$ is the loss tangent of dielectric layer.

We generate the unit cell model and cascade them into $M \times N$ for the full PDN model using MATLAB. The entire PDN model is characterized as S-parameter model and RLGC values for PDN IR-drop co-analysis and PI analysis.

C. Static IR-Drop Co-Analysis Results

As we discussed in Section V-A, we perform IR-drop co-analysis of 2.5-D design with the testbench as shown in Fig. 9. The testbench contains IVR models, PDN model, and chiplet models to consider the entire 2.5-D system. For simplicity, we set input and output ports as the center of chiplets, and each chiplet model as a static step current source. The IVR chiplets are modeled with a power converter model. Using Keysight ADS, we show the result of interposer PDN IR-drop in Fig. 10(a). The Vdd drop between IVR chiplets to logic chiplets ranges from 87.72 to 112.72 mV. The worst drop occurs at chiplets on the top and bottom edges, such as Rocket 3 chiplet, because the distance from the input source is longer than other chiplets.

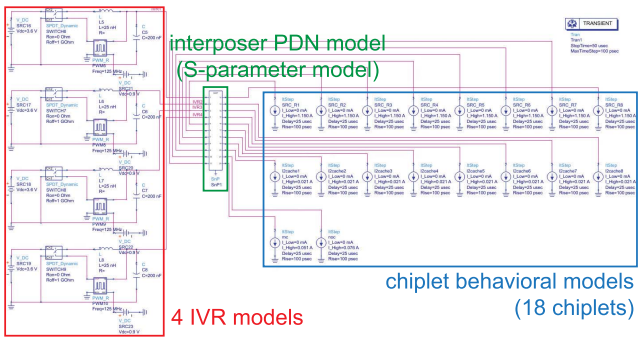

Fig. 9. Testbench of the interposer PDN IR-drop analysis.

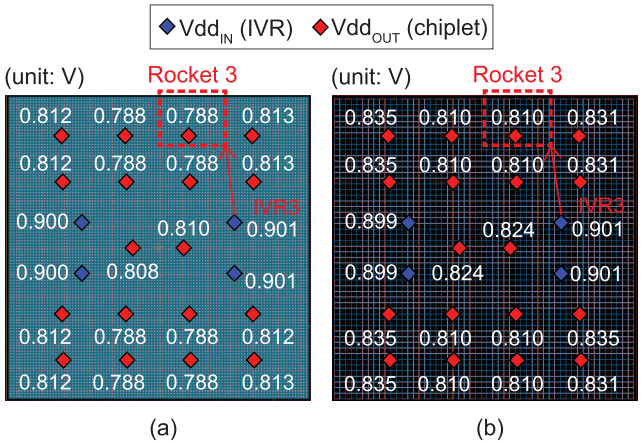

Fig. 10. Interposer IR-drop co-analysis results of two 2.5-D designs. (a) Design 1. (b) Design 2.

Using the simulation result of interposer PDN as the boundary conditions, we perform on-chip PDN IR-drop analysis. The result of Rocket 3 chiplet, which has the lowest Vdd level, is shown in Fig. 11(a). Compared with the ideal 0.9 V Vdd, the worst IR-drop has increased from 29.51 to 29.88 mV. This accurate IR-drop co-analysis opens up an opportunity to further optimize the on-chip PDN of Rocket chiplet 3.

The overall IR-drop from chip to package of our 2.5-D design is estimated as 142.60 mV. 79.05% of IR-drop has occurred from the interposer PDN, and 20.95% from the chiplet PDN. As the general power specification of Vdd level is ±10%, our PDN co-analysis result exceeds the limitation. Therefore, we perform 2.5-D PDN optimization to lower the overall IR-drop to guarantee the performance of the 2.5-D IC design.

In the new 2.5-D design with PDN optimization, which is Design 2, we enlarge the dimensions of interposer P/G lines as shown in Table IV. To lower the IR-drop in interposer PDN,

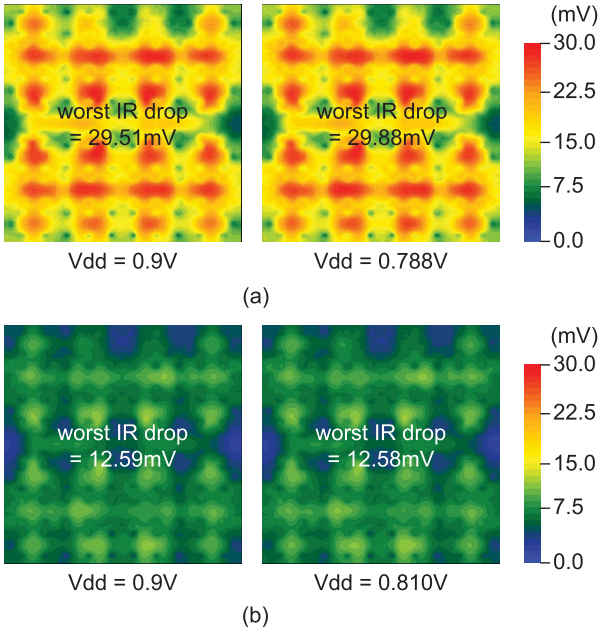

Fig. 11. Comparison of Rocket chiplet IR-drop reflecting interposer PDN optimization results. (a) Design 1: before PDN optimization. (b) Design 2: after PDN optimization.

TABLE IV
COMPARISON BETWEEN TWO INTERPOSER PDN DESIGNS

	Design 1	Design 2	
PDN optimization	N	Y	-
PDN width/spacing	$40\mu m/100\mu m$	$95\mu m/200\mu m$	-
PDN occupancy (%)	61.65	67.17	+5.52%
PDN DC resistance ($m\Omega$)	19.43	14.88	0.77×
Worst IR-drop (mV)	112.72	91.27	0.81×

we have increased the size of PDN unit cell with 95 μm width and 200 μm spacing. First, considering the signal routability in the interposer layer, we have increased the PDN spacing from 100 to 200 μm. The PDN width has also increased to 95 μm for higher PDN occupancy in the interposer layer. The interposer PDN in Design 2 has dc resistance of 14.88 mΩ which is smaller than that of Design 1 by 23.42% with 5.52% increased PDN occupancy. Fig. 10(b) shows the interposer IR-drop result of Design 2. The worst drop occurs at Rocket chiplet 3 same as Design 1, which is 91.27 mV.

D. Chiplet PDN Optimization Results

We optimize chiplet PDN as well as interposer PDN to improve the overall IR-drop in 2.5-D IC design. To reserve enough room for the IR-drop from interposer PDN, we re-specify the allowance of chiplet IR-drop as 1.5% instead of 5%. Since 5% of allowance results in 20.95% of the overall IR-drop, we have set 1.5% of IR-drop allowance to target 10% of the overall IR-drop from the chiplet side, approximately. As the PDN utilization of each chiplet has already reached to 20%, we insert the additional PDN grid in M3 and M4 layers as shown in Table V.

Through our PDN optimization, the IR-drop of each chiplet has decreased below 1.5% of Vdd to the maximum of 12.59 mV from Rocket chiplet. However, as the signal routability also decreases due to the additional PDN insertion,

TABLE V
CHIPLET DESIGN RESULTS WITH OPTIMIZED PDNS IN DESIGN 2. (Vdd = 0.9 V)

	Rocket	L2 cache	NoC	Memory controller
Cell count (#)	930,824	3,735	81,273	52,258
Worst slack (ps)*	84.10	105.83	102.72	92.937
Total power (mW)	1,153.31	18.98	73.07	49.18
PDN M5/6 width (μm)	0.5	0.5	0.5	0.5
PDN M5/6 pitch (μm)	3.0	3.0	3.0	3.0
PDN M3/4 width (μm)	0.3	0.3	0.3	0.3
PDN M3/4 pitch (μm)	2.5	2.5	2.5	2.5
PDN utilization (%)	31.67	37.48	29.59	30.40
Worst IR-drop (mV)	12.59	5.77	12.49	8.69
IR-drop/Vdd (%)	1.40	0.64	1.39	0.97

* The positive slack is used in the table.

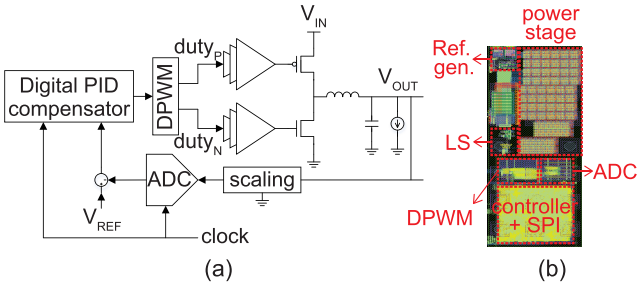

Fig. 12. Block diagram and GDS layout of our IVR chiplet. (a) Block diagram. (b) GDS layout.

the timing and power performance of each chiplet are degraded when compared to the chiplet designs in Design 1. For the maximum case, the total power has increased by 11.45% in case of Rocket chiplet as switching power has increased by 17.03% due to longer nets. Moreover, the worst positive slack has decreased by 12.37% in the case of L2 cache chiplet, but all chiplet designs are well within the limits to meet the target frequency at 1 GHz.

E. Interposer PDN Optimization Results

To evaluate the PI of our 2.5-D designs, the current path is set as {micro-bumps of IVR chiplets, via, P/G mesh on interposer, via, micro-bumps of target chiplets}. All physical parameters in Table I are used for evaluating PDN impedance of interposer designs. Fig. 13(a) shows the PDN impedance comparison between Design 1 and 2 with 10 × 10 array of micro-bump, via, TSV and C4 bump arrays each.

For the transient analysis of 2.5-D designs, we adopt the IVR design as shown in Fig. 12 [13]. This IVR is implemented as a system containing a power stage, feedback/control loop and an LC output filter. The feedback/control loop consists of ADC, type-III proportional integrate-differential (PID) controller, and a digital pulsewidth modulation (DPWM) block. The voltage error calculated from the reference and the output voltages, is compensated by the PID compensator and the resulting output is fed to a DPWM engine, generating gate drive signals with a duty cycle based on control word. In our 2.5-D design, IVR chiplet is designed using a commercial 130-nm technology node to introduce the heterogeneity of 2.5-D integration.

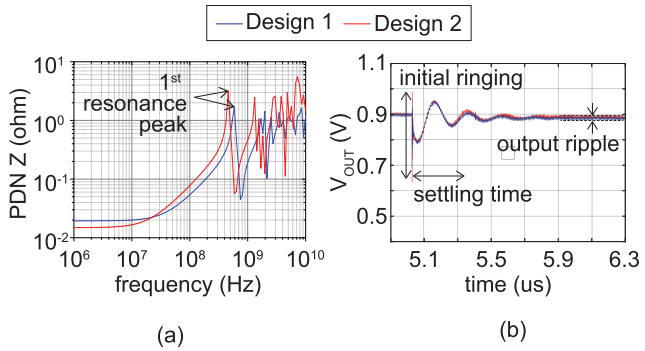

Fig. 13. PI analysis results of our 2.5-D IC designs. (a) Interposer PDN impedance. (b) Transient simulation.

The calculated interposer PDN impedance and the target load current of our benchmark design are imported into transient simulations with custom Simulink models to estimate voltage settling time, dynamic voltage and frequency scaling (DVFS), output ripple, and voltage conversion efficiency. Our Simulink model for IVR chiplet is adopted from MATLAB/Simulink switched-mode power converter models by CoPEC [14]. The results of the transient simulation are shown in Fig. 13(b). The detailed comparison of PI results between the two designs is given in Section VI.

VI. Overall PPA Versus PI Tradeoffs

A. PPA Tradeoffs

Table VI summarizes our design and analysis results so far and Fig. 14 shows the final GDS layout of Design 2, which PDNs are optimized. To minimize the area overhead, the footprint of Design 2 has remained the same as Design 1. As we are using mesh-type PDNs in both design, the spaces reserved for signal routing exist in each PDN unit cell. Therefore, the average wirelength of interposer lines remains similar even if we increase the PDN occupancy by 5.52%. The worst propagation delay in Design 2 is 84.90 ps same as Design 1 because the maximum wirelengths in both designs are the same.

The total power of Design 2 is 13.304 W which is 1.12× higher than Design 1. The power of chiplets has increased by 11.24% because of the additional power grids on M3 and M4 layers. As the additional power grids lower the signal routability, the worst positive slack has decreased by up to 12.37% in Design 2. However, this degradation is still within the boundary. I/O power remained similar because the average wirelength of the interposer design is similar to Design 1. The power loss at IVR chiplets has increased by 13.3% because the power efficiency of IVR chiplet in Design 2 is lower than Design 1 by 0.4%.

B. PI Tradeoffs

Using our IR-drop co-analysis and PDN optimization flow, the worst overall IR-drop including both IR-drops of the interposer and chiplet in Design 2 is 103.86 mV, whereas 142.60 mV in Design 1. The worst interposer IR-drop is 91.27 mV at Rocket chiplet in Design 2, which is 0.81× of Design 1 because the dimensions of PDN mesh line

TABLE VI
2.5-D IC Design Comparison Between Design 1 and 2

	Design 1	Design 2	
PDN optimization	N	Y	-
Area (mm^2)	116.64	116.64	-
Frequency (GHz)	1.0	1.0	-
Interposer metal layer (#)	4	4	-
Routed Wirelength in Interposer			
Min wirelength (mm)	0.14	0.15	1.08×
Ave wirelength (mm)	2.83	2.80	1.00×
Max wirelength (mm)	6.97	6.97	1.00×
Power Consumption			
Total power (W)	11.924	13.304	1.12×
Logic power (W)	8.540	9.501	1.11×
I/O power (W)	0.212	0.211	1.00×
IVR power (W)	3.172	3.592	1.13×
Power Integrity			
Worst PDN IR-drop (mW)	142.60	103.86	0.73×
Interposer PDN occupancy (%)	61.65	67.17	+5.52%
Interposer PDN DC R (mΩ)	19.43	14.88	0.77×
Conversion ratio (V/V)	3.6/0.9	3.6/0.9	-
Inductor (L,nH)	25	25	-
Capacitor (C,nF)	200	200	-
f_{SW} (MHz)	125	125	-
Decap. (nF)	25	25	-
Output voltage ripple (mV)	13.8	18.3	1.33×
Voltage droop (mV)	122	113	0.93×
Initial ringing (peak-to-peak, mV)	270	355	1.31×
Power efficiency (%)	73.4	73.0	-0.4%
Settling time (ns)	289	289	1.00×
DVFS (mV/ns)	200/440	200/440	1.00×

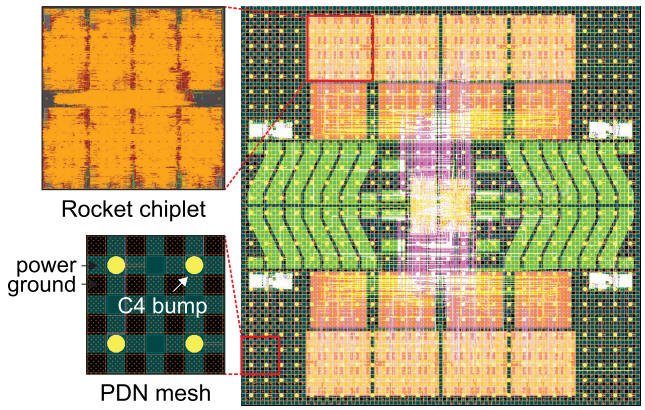

Fig. 14. GDS layout of our final 2.5-D IC design with PDN co-optimization. All chiplets are integrated on the interposer layer.

are larger than Design 1. Due to the expanded PDN mesh in Design 2, the PDN occupancy has increased by 5.52%. However, the number of metal layers and the footprint of silicon interposer remained the same as Design 1. From the perspective of chiplet PDNs, the worst IR-drop in chiplets of Design 2 has reduced by up to 57.9% compared to Design 1.

In terms of PDN impedance, Design 1 has a higher impedance at low frequencies because its geometrical features represent a more resistive behavior as shown in Fig. 13(a). The PDN in Design 1 shows 19.43 mΩ of dc impedance compared to 14.88 mΩ in Design 2. However, as the frequency increases, the impedance of Design 2 surpasses that of Design 1, showing a more inductive behavior. The first resonance peak in Design 1 comes at 0.6 GHz, whereas at 0.48 GHz in Design 2 which shows the bandwidth reduction in Design 2 by 0.8× approximately.

For the PI analysis in time domain, we use 25 nF of decoupling capacitor and give the load jump from 250 mA to 1.55 A. In both Design 1 and 2, the voltage settling time is 289 ns and DVFS is evaluated as 200 mV/440 ns. However, Design 2 shows 1.33× higher ripple and 1.31× higher initial ringing at the output node of IVR chiplet as shown in 13(b) because its PDN has a more inductive behavior than Design 1. Design 1 shows 73.4% of voltage conversion efficiency, while Design 2 has 73.0%. This efficiency loss of 0.4% in Design 2 happens because dc resistances of interposer PDNs are not different by a significant margin, the losses due to output voltage ripple are more significant. These comparisons between Design 1 and 2 show the tradeoffs in terms of PPA and PI depending on PDN optimization precisely.

VII. Conclusion

In this article, we perform chiplet/interposer co-design, co-analysis, and optimization of PDN in interposer-based 2.5-D IC design. Our analysis flow integrates frequency domain component models to time domain simulations for a co-analysis of PDN and power delivery modules. PDN co-analysis provides the weight of the overall IR-drop of 2.5-D design and IR-drop of the interposer and chiplet designs which are the initial points for PDN optimization. Our PDN optimization result shows a 27.17% reduction in the overall IR-drop from the interposer to chiplets. However, we also observe tradeoffs in terms of PPA and PI by lowering IR-drop with larger PDN dimensions. Design 2 which has optimized PDN designs shows 1.12× higher power consumption in terms of PPA compared to Design 1. In terms of PI, Design 2 has 1.33× higher output ripple, 1.31× higher ringing, and 0.6% lower power conversion efficiency than Design 1 due to an inductive behavior of its PDN. This work provides the thorough PDN co-design and co-analysis framework on interposer-based 2.5-D IC design and fundamentals for further PDN optimization.

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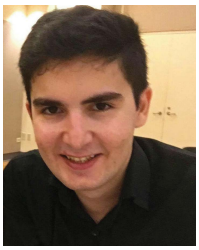

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