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Glass Interposer Integration of Logic and Memory Chiplets: PPA and Power/Signal Integrity Benefits

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***Abstract*—Glass interposers have become a compelling option for 2.5D heterogeneous integration compared to silicon. It allows 3D stacking configuration between the embedded dies and the conventional flip-chip dies mounted directly on top at low cost. Furthermore, the interconnect pitch and through-glass-via (TGV) diameter in glass are becoming comparable to their counterparts in silicon. In this study, we investigate the power, performance, area (PPA), signal integrity (SI) and power integrity (PI) advantages of 3D stacking afforded by glass interposers over silicon interposers. Our research employs a chiplet/package co-design approach, progressing from an RTL description of RISC-V chiplets to final graphic data system (GDS) layouts, utilizing TSMC 28nm for chiplets and Georgia Tech's 3D glass packaging for the interposer. Compared to silicon, glass interposers offer a 2.6X reduction in area, a 21X reduction in wire length, a 17.72% reduction in full-chip power consumption, a 64.7% increase in signal integrity and a 10X improvement in power integrity, with a 35% increase in thermal. Furthermore, we provide a detailed comparative analysis with 3D Silicon technologies. It not only highlights the competitive advantages of glass interposers, but also provides critical insights into each design's potential limitations and optimization opportunities.**

I. Introduction

Partitioning highly complex systems into "chiplets" is one promising approach today and in the future to enhance the yield and functionality of these systems [1]. These chiplets, which are relatively small and independently manufactured ICs, are integrated into the overall system, offering design flexibility and efficiency. The integration of chiplets can be achieved through two primary configurations: 2.5D interposers and 3D stacking. The 2.5D integration method has gained popularity for its ability to combine multiple off-the-shelf chiplets or intellectual properties (IPs) reuse on a single interposer substrate with different technology nodes (Heterogeneous integration). In this approach, chiplets are placed side-by-side on the interposer's surface as in Fig. 1(a), and connectivity is provided through the redistribution layer (RDL), metal layers on the passive interposer substrate that facilitate lateral connections among chiplets and distribute power from an external source. The materials commonly used for interposer packaging include silicon, organic compounds, and glass, each offering distinct advantages in terms of electrical performance, thermal management, and manufacturing costs.

In 3D integration, chiplets are stacked on top of each other. These chiplets are interconnected using micro-bumps or hybrid bondings. A technology called Through-Silicon-Via (TSV) is used to connect cross-over 3D nets and deliver power across these chiplets. This method has several advantages over 2.5D integration. It allows for a higher density of integration and improves the speed of signal transmission. This, in turn, enhances the overall performance of the system and reduces power usage. Furthermore, it enables the integration of different types of components, which allows the creation of more complex and multifunctional systems within a small form factor.

The glass interposer is emerging as a competitive option to these two integrations. Both silicon and organic interposers require TSVs for 3D integration (TSV-based 3D), resulting in low bandwidth and significant overhead because of the large TSV size. Conventional 3D integration also requires high costs to take advantage of chip performance improvements. However, glass is the only material that allows the chiplet to be placed within the substrate, naturally providing 3D stacking capability between the embedded die and the conventional flip-chip die on the top. Glass interposers also provide a cost-effective means for embedding chiplets, enhancing the system's 3D stacking configuration. Moreover, the advancements in through-glass-via (TGV) technology have led to interconnect pitches and TGV diameters in glass that are now comparable to those in silicon. This evolution positions glass as a particularly attractive option for achieving 2.5D heterogeneous integration, offering distinct advantages over traditional silicon-based solutions.

Despite significant advancements, further research is needed to fully realize the potential of glass interposers in enhancing system-level integration, particularly in 3D stacking configurations. A previous study [2] compared the processes and performance of glass and silicon interposers, but this comparison was limited to the packaging level, without considering a comprehensive chip design, leaving the impact of high-density connections unexplored. Another study [3] focused on system-level comparisons between silicon and organic interposers, yet did not examine glass interposers in a 3D context. In prior work [4], 3D glass stacking was evaluated alongside traditional silicon and organic interposers, though the comparison did not

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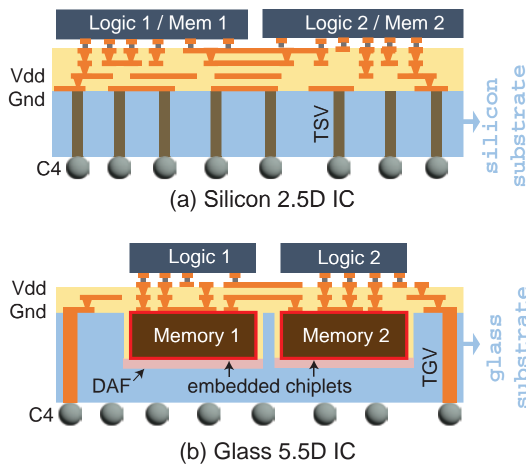

Fig. 1. Cross-sectional view of logic and memory chiplet integration. (a) "2.5D" silicon interposer using through-silicon-via (TSV), (b) "5.5D" glass interposer using die embedding and through-glass-via (TGV).

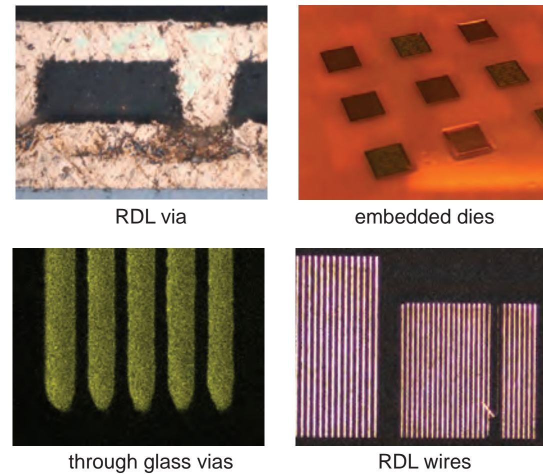

Fig. 2. Our manufactured samples of key elements in the glass interposer technology. Dimensions are reported in Table I.

include TSV-based 3D silicon technology. Building upon this foundation, our work aims to provide an in-depth system-level comparison of glass interposers in 3D stacked configurations, considering both traditional interposer counterparts—silicon and organic—as well as TSV-based 3D silicon designs. This will advance our understanding of the role glass interposers can play in future semiconductor technologies.

Therefore, in this paper, we explore the innovative integration of chiplets using glass interposers in a non-TSV based "5.5D" stacking (glass 3D) as in Fig. 1(b), performing a comprehensive comparison with state-of-the-art (SOTA) interposers such as glass, silicon and organic. Moreover, we investigated the benefits and limitations of glass interposer with stacking configuration compared to 3D Silicon from a 3D stacking perspective. Our contribution is as follows:

1) We introduce a novel co-design methodology for the RISC-V processor utilizing glass interposers, achieving significant advancements in 5.5D stacking technology.
2) We demonstrate marked improvements in power, performance, area (PPA), signal integrity (SI), power integrity (PI), and thermal integrity (TI) on our final design of glass interposer with stacking configurations.
3) Our findings reveal a 2.6X reduction in area, a 21X reduction in wire length, a 17.72% reduction in full-chip power consumption, a 64.7% increase in signal integrity, and a 10X improvement in power integrity, compared to conventional interposer materials.
4) We also highlight comparison between glass interposers and 3D Silicon and quantify the advantages and potential limitations of each technology.

II. Background & Related work

Heterogeneous integration is widely recognized as a crucial advancement in semiconductor technology, effectively meeting the increasing demands of modern computing applications, especially in the field of artificial intelligence (AI) [5]. This advanced approach involves combining a variety of components, such as processors, memory units, and RF modules, into a cohesive system [6]. By integrating the 2D and 3D packaging technologies, significant improvements in performance, efficiency, and functionality are achieved [7]. Exploring different packaging methods, each customized to specific material properties and manufacturing processes, offers a range of solutions customized to fulfill diverse application requirements [8]. This balance optimizes cost, performance, thermal regulation, and electrical efficiency.

A. 2.5D Interposers: Silicon and Organic

Silicon and organic materials are key in 2.5D interposer technologies, each offering unique advantages in electrical performance, integration density, and cost-efficiency. For instance, [3] compares silicon to liquid crystal polymer (LCP) interposers for 2.5D chiplet integration, analyzing power, performance, area, and signal and power integrity trade-offs. The study illustrates that silicon interposers excel in power consumption, area efficiency, and wire length minimization, whereas LCP interposers offer lower power delivery network (PDN) DC impedance and reduced wire delays. In addition, [9] and [10] evaluate 2D, 2.5D, and 3D interconnects and propose power-efficient transmission and channel optimization methods. However, existing research largely overlooks the need for chiplet/interposer design flow of glass interposers and lacks a comprehensive analysis of interposer types concerning PPA, signal/power integrity, and thermal aspects.

B. Comparison with Silicon 3D IC Technology

3D IC technology research marks a significant advancement, offering strategies to surpass the limitations of traditional 2D or 2.5D interposers through novel stacking techniques, material improvements, and thermal management. Recent studies, such as [11], concentrate on enhancing integration density and system performance while mitigating power and thermal challenges. Furthermore, research comparing 3D ICs with glass interposers, such as [2], indicates that glass interposers provide superior electrical isolation, cost benefits, and reduced thermal coupling among chips, positioning them as a feasible

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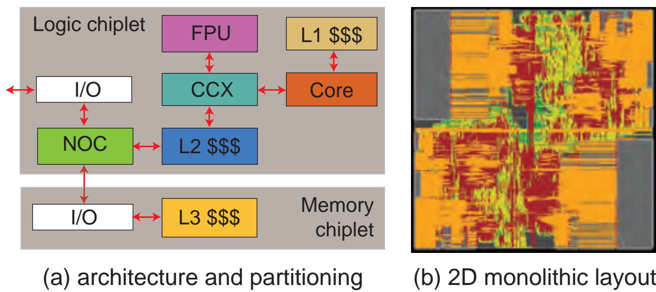

Fig. 3. (a) Single tile architecture of OpenPiton RISC-V [15] and our logic/memory chiplet partitioning, (b) single chip design using TSMC 28nm.

alternative to silicon, particularly where thermal management and cost-effectiveness are crucial. Nonetheless, there remains a research void in system-level design, PPA, and the signal/power integrity and thermal impacts of 3D ICs and glass interposers, highlighting the need for further investigation in these areas.

III. Glass Interposer Manufacturing

Recently, glass has been studied as an interposer substrate due to its favorable mechanical, electrical, and thermal properties [12]. Glass' ability to process large panels offers benefits for systems with many chiplets. Additionally, its smooth surface allows high-density wiring similar to silicon interposers at a lower cost. The finest line/space on a glass interposer with embedded dies is 2µm [13]. Also, glass in packaging offers electrical advantages, including a low loss tangent, reducing dielectric losses and improving signal quality. Its thicker metallization layers reduce conductor losses and increase bandwidth compared to silicon and customizable thermal expansion enhances chip reliability, making glass suitable for high-performance systems [14].

Our proposed "5.5D" interposer architecture (Fig. 1) embeds chips in glass cavities to create short chip-to-chip "microvia" interconnects through RDL. Blind or through cavities are formed via wet etching or laser drilling, with cavity depth controlled by etch rate or laser focus. The thickness of the glass substrate (ENA1) is 150∼160 µm. Therefore, the embedded die height is constrainted to be less or equal to the core substrate thickness for through cavities. For blind cavities where the cavity depth is less than the core thickness, a 10-µm-thick die-attach film (DAF) is applied to fix chips to the desired position in the cavity, as illustrated in Fig. 1(b). Surface planarization is used to mitigate RDL non-planarities caused by embedded dies. Microvia diameter is limited by dielectric thickness, and UV laser-drilled microvias typically have a 1:1 width-to-depth aspect ratio [16]. The RDL is patterned using a semi-additive process, with a 50nm Ti layer enhancing copper adhesion. Fig. 2 shows fabrication results, including RDL vias, embedded dies, TGVs, and RDL wires. Detailed glass stackup processes are described in [17] and [18].

IV. Design and Simulation Settings

A. Architecture Benchmark

We leverage the RISC-V OpenPiton architecture [15] as the primary benchmark, as depicted in Fig. 3. The structure of the

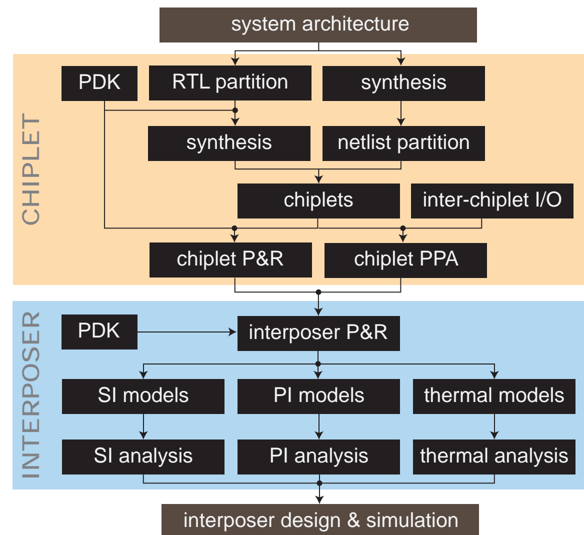

Fig. 4. Our chiplet/interposer co-design flow. Our chiplet tools are from Cadence, Synopsys, and in-house, while the interposer designs and simulations are done with tools from Siemens and Ansys. SI and PI respectively denotes signal and power integrity.

OpenPiton chip in this work comprises two interconnected OpenPiton tiles. Communication between tiles is facilitated through the Network-on-Chip (NoC) Router located within each tile, ensuring efficient data transmission and system-wide coherence. The OpenPiton tile consists of computational modules (Core, floating point unit (FPU), and CPU Cache-crossbar (CCX)), memory modules (L1 caches, L2 caches, and L3 caches), and a network-con-chip (NOC Router).

We chipletize each OpenPiton single tile into two parts through hierarchical-based partitioning. Initially, we aggregate the L3 cache and its interfacing logic into a memory chiplet, and classify the remaining modules as a logic chiplet. This partitioning strategy aims to achieve the minimum possible cut-size between the two chiplets, thereby minimizing the die size within the parameters defined by the bump pitch constraints for each I/O pin. This approach ensures an optimized configuration that carefully balances the physical dimensions of the die against the technical requirements for I/O connectivity, facilitating efficient inter-chiplet communication while adhering to essential design constraints.

Given the substantial number of connections between two OpenPiton tiles, characterized by six 64-bit buses and 20 control signals, the integration of I/O bumps directly onto the chiplet faces a significant challenge due to the micro-bump pitch constraints. These constraints limit practical cell utilization, making it unfeasible to accommodate the extensive I/O requirements within the chiplet's spatial confines. To address this issue, we incorporate a Serializer/Deserializer (SerDes) module, which effectively reduces the bandwidth demands from 64-bit parallel interfaces to more manageable 8-bit serial connections. This adaptation maintains the integrity of the control signals without alteration, with the cost of 8 additional cycles for inter-tile communications. Consequently, the total number of connections required for inter-tile communication is reduced to 68, whereas the internal connections within a

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TABLE I
INTERPOSER SPECIFICATIONS USED IN THIS PAPER.

	Glass		Silicon	Organic	
	2.5D	3D		Shinko	APX
# Metal Layer	7	3	4	7	8
Metal thickness	4µm		1µm	2µm	6µm
Dielectric thickness	15µm		1µm	3µm	14µm
Dielectric constant	3.3		3.9	3.5	3.1
Min. Wire W / S	2µm/2µm		0.4µm/0.4µm	2 µm/2µm	6µm/6µm
Via size	22µm		0.7µm	10µm	32µm
Bump size	16µm		20µm	25µm	32µm
Die-to-Die spacing	100µm		100µm	N/A	150µm
Micro-bump pitch	35µm		40µm	40 µm	50µm

single tile are quantified at 231. This strategic implementation of SerDes technology facilitates a significant reduction in the physical space required for interconnects, enabling efficient utilization of chiplet area while adhering to the strict micro-bump pitch limitations.

B. Chiplet/Interposer Co-design Flow

Our design flow is shown in Fig. 4, where we design both chiplet and interposer and perform the analysis, including PPA simulation, interposer design analysis, SI, PI, and TI analysis. The design flow consists of two approaches of chipletization: hierarchical-based partitioning, flattening partitioning. In this study, we utilize the hierarchical-based partitioning (left branch). From the OpenPiton architecture in Section IV-A, we first generate the register-transfer-level (RTL) of the OpenPiton chip design with two tiles setting. Next we partition modules based on Fig. 3(a) and synthesize the netlist with process design kit (PDK) for a particular technology node. Each logic and memory chiplet netlist is reused for each OpenPiton tile. Furthermore, to meet target timing even with off-chip connections, we design our inter-chip I/O driver to support the maximum interconnect length determined by the interposer design. And, we insert them into the chiplet netlist for each I/O pin and perform the chiplet design with Cadence Innovus. Finally, we analyze the chiplet PPA with Cadence Tempus.

In the interposer design step, we import in the chiplet footprint and interposer stack-up information such as metal layers, dielectrics, vias, and substrate. We insert the power delivery network (PDN) into the interposer and perform routing using Siemens Xpedition tool. Next, we analyze the SI, PI, and TI from interposer layout. Lastly, we verify all the design with simulation to ensure the performance, power, and thermal constraints are met.

C. Interposer Design Rules

We implement Glass, Silicon, and organic interposers using the design rule as defined in Table I. For glass interposer, we refer to the specification from the manufacturing capabilities of Georgia Tech's Packaging Research Center (PRC), where we are capable of manufacturing fine line 2µm line and spacing. The micro-bump pitch supports with a minimum of 35µm, which allows high-density I/O connections. The glass interposer allows the creation of a cavity and embeds the die inside. For the Silicon interposer, we leverage the Chip-on-Wafer-on-Substrate (CoWoS) technology [19], which provides

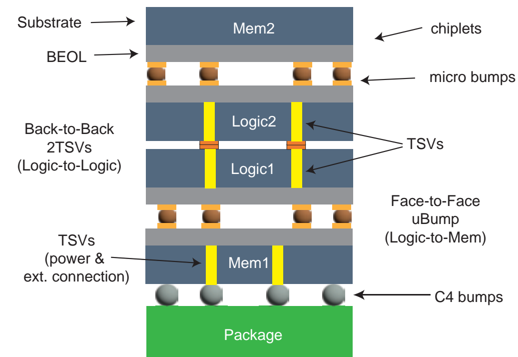

Fig. 5. Cross-sectional view of 4-tier TSV-based Silicon 3D design.

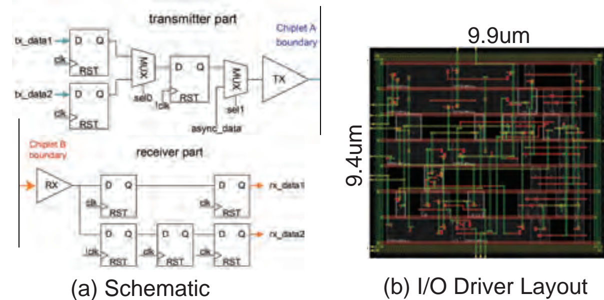

Fig. 6. I/O Driver schematic and layout used in this work.

0.4µm line and spacing with 40µm micro bump pitch. For Organic interposers, we have two types of organic interposers: Shinko [20] and Advance Packaging X (APX) [21]. The Shinko interposer provides fine-line from an additional thin film layer on top of conventional organic build-up layer. The APX is the conventional organic interposer which has improved over the year to support high-density connections.

D. Design flow for TSV-based 3D IC

Unlike interposer-based design (2.5D IC), the TSV-based 3D design strategy involves stacking chiplets on top of each other, interconnecting them through the use of microbumps and through-silicon vias (TSVs). Given partitioned netlists, the I/O driver for off-chip connections is incorporated in a manner similar to the 2.5D design, ensuring acceptable propagation delay and signal integrity. Prior to initiating the chiplet design process, both the micro-bump and TSV are modeled, selecting dimensions that align with timing targets and fabrication capabilities. Upon finalizing the dimensions of the 3D interconnects, chiplet design proceeds using Cadence Innovus. The chiplet's power, performance, and area (PPA) metrics are subsequently analyzed with Cadence Tempus to verify adherence to timing constraints prior to proceeding with 3D integration.

In the chiplet 3D integration step, we extract each chiplet's parasitics and interconnect's parasitics and perform the timing and power analysis. We also analyze the signal integrity and thermal integrity of the design. In the signal integrity analysis, we perform the eye-diagram analysis and transmission delay and power.

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TABLE II
CHIPLET BUMP USAGE AND AREA COMPARISON. ALL CHIPLETS ARE SQUARE.

	Glass				Silicon				Organic			
	Glass 2.5D		Glass 3D		Silicon 2.5D		Silicon 3D		Shinko		APX	
	logic	mem	logic	mem	logic	mem	logic	mem	logic	mem	logic	mem
Micro-bump pitch	35μm		35μm		40μm		40μm		40μm		50μm	
Signal bump	299	231	299	231	299	231	299	231	299	231	299	231
P/G bump	165	131	165	121	165	130	165	165	165	130	150	116
Total bump	464	362	464	352	464	361	464	396	464	361	449	347
Width (mm)	0.82	0.78	0.82	0.82	0.94	0.82	0.94	0.94	0.94	0.82	1.15	1.00
Area (mm2)	0.67	0.61	0.67	0.67	0.88	0.67	0.88	0.88	0.88	0.67	1.32	1.00
Area ratio	1.00	1.00	1.00	1.11	1.31	1.11	1.31	1.45	1.31	1.11	1.97	1.64

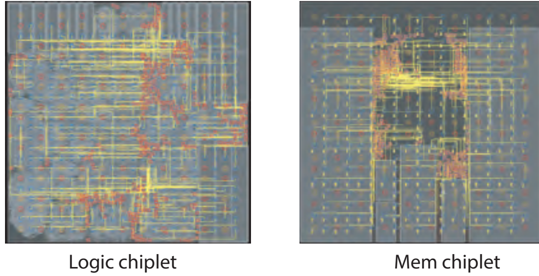

Fig. 7. Bump-to-AIB I/O driver layout of glass interposer's chiplets. Note that the yellow line represents the nets, and the red rectangle denotes the AIB I/O driver.

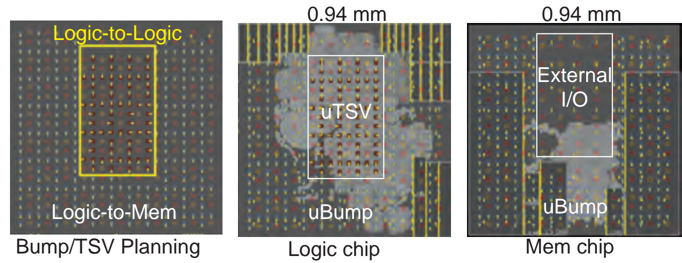

Fig. 8. Microbump/TSV Partitioning of logic and memory chiplets of Silicon 3D, and logic and memory chiplet layout.

V. CHIPLET DESIGN RESULTS

A. Chipletization Results

We group the RTL based on Fig. 3(a) and synthesize the netlist of the logic and memory chiplet. Since the chiplet are to be connected via an interposer RDL or 3D interconnects, we utilize the I/O driver design from [3], which supports the maximum transmission length of $10mm$. The I/O driver is designed based on Intel's Advance Interface Bus (AIB) with pipe-lining for data transmission. Therefore, the connection between chiplets would take one clock cycle to transmit, accommodating more flexible timing closure. We insert the I/O driver into the chiplet netlist. For the inter-tile connection (Logic-to-Logic), we insert the serialized connection module before the I/O driver.

In the interposer-based design, the micro bumps are placed with the minimum pitch for each interposer design as defined in Table I. Finally, we implement the layout and generate the Liberty model library to be used as hard macros in the chiplet design.

We calculate and design the chiplet footprint as in Table II. The signal bump to power bump ratio is 2 to 1 to have a compact footprint with high density. The number of total bumps in the logic chiplet is higher than the memory chiplet because the logic chiplet contains the connection across the different OpenPiton tiles and the connection within the tile (to the memory chiplet).

In the exploration of heterogeneous 3D integration options, it becomes evident that the choice of interposer substrate significantly influences the dimensions of the interposer, specifically in terms of width and height. This dimensionality is intrinsically linked to the micro bump pitch specified in the design rules for each type of interposer. Notably, the glass interposer exhibits the most minimal dimensions, attributed to its micro bump pitch of 35 μm, which is the smallest compared to alternative interposer technologies. Consequently, as the bump pitches for Silicon and Shinko interposers align, the resulting chiplet footprints for these substrates are commensurate in size. In contrast, the APX interposer supports a chiplet with substantially larger dimensions, a consequence of its expanded micro-bump pitch.

This variation in micro bump pitch leads to a consistent area ratio between logic and memory components across the different interposer substrates, maintaining a uniform architecture across various materials. Nonetheless, the divergence in footprint dimensions across distinct interposers induces variations in footprint density, quantified as a percentage. Such differences illuminate the pivotal role of interposer substrate selection in optimizing space utilization within chiplet-based system architectures.

In the case of Silicon 3D design, the 4-die stacking configuration includes two logic chiplets and two memory chiplets. Additionally, an I/O driver is incorporated for off-chip connections to account for the parasitics associated with micro-bumps and Through-Silicon Vias (TSVs), which are non-negligible for ensuring reliable signal transmission. The chiplets are stacked as depicted in Fig. 5, positioning the memory chiplet of the first processing tile at the base, followed by the logic chiplet, and subsequently the chiplets of the second processing tile. Given that the memory chiplet facilitates external I/O for the logic chiplet, the dimensions of the memory chiplet in Silicon 3D are matched to that of the logic chiplet. With the micro-bump pitch set at 40μm, the dimensions of the logic chiplet in Silicon 3D align with those of the Silicon 2.5D logic chiplet, as this represents the minimal footprint required to accommodate all the I/Os. Consequently, both the logic and

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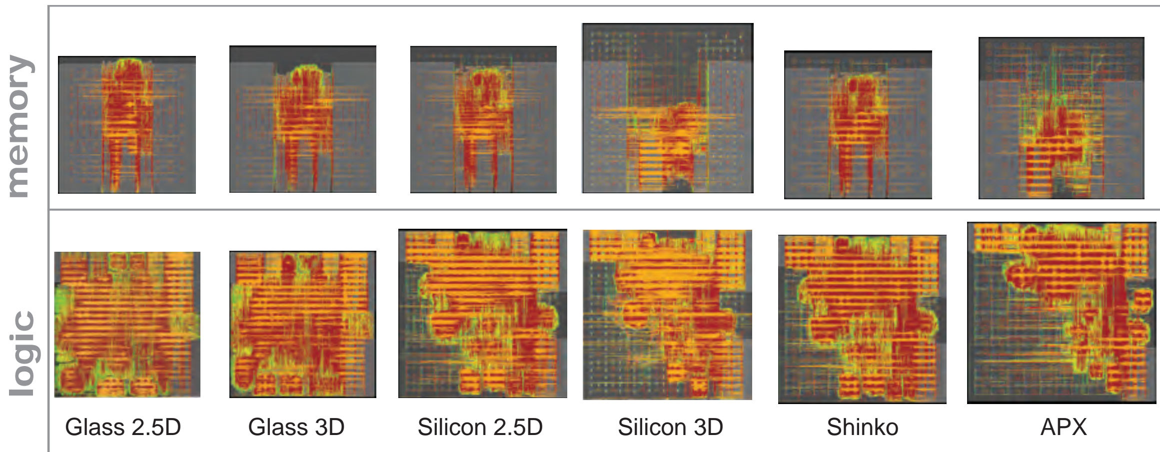

Fig. 9. GDS layout of chiplets used in our interposer designs. The dimensions are provided in Table II and power & performance in Table III

memory chiplets of Silicon 3D measure 940µm in both width and height.

B. I/O Driver Design

The design of the I/O driver is aimed at facilitating off-chip connections among chiplets. This driver architecture is divided into two primary components: the transmitter and the receiver, as illustrated in Fig. 6(a)-(b). Each component of the I/O driver is conFig.d to support Double-Data-Rate (DDR) transmission, allowing data flow during both the rising and falling phases of the clock cycle, as depicted in $tx_{data1-2}$ and $rx_{data1-2}$. However, within the scope of this study, data transmission is limited exclusively to the clock's rising edge. The operational strength of both the transmitting (TX) and receiving (RX) units is based on the guidelines posited in [22], which support a transmission wire length of up to 10mm. The I/O drivers are synthesized using the TSMC 28nm Process Design Kit (PDK). The layout of the I/O driver, displayed in Fig.6(c) with 9.9µm by 9.4µm in size.

C. Interconnect Planning for TSV-based 3D

In 3D silicon technology, two types of interconnects are utilized: through-silicon vias (TSVs) for inter-tile connections and micro bumps for intra-tile connections. Due to the stacking of memory and logic dies, precise alignment of the 3D interconnects is required. To facilitate the integration of external I/O between the memory and logic chiplets, distinct dedicated regions are allocated for each type of connection.

In the memory chiplet, the regions for bumps and TSVs are divided into two distinct zones. The central region is designated for logic-to-logic connections, while the logic-to-memory connections form a U-shaped arrangement around the center. Micro-bump connections are established through bump pads. For the TSVs, I/O pads are positioned on the bottom metal layer, with placement blockages introduced to reserve space for the TSVs. In the case of the lowermost memory chiplet, I/O pads are similarly created for logic-to-logic connections, enabling the transfer of external I/O from the TSVs to the logic chiplet.

The logic chiplet adopts a similar bump partitioning approach to ensure alignment with the memory chiplet. The designated bump partition area is depicted in Fig. 8, employing a bump pattern similar to that used in the 2.5D design. The layouts of both memory and logic chips are shown in Fig. 8, illustrating the strategic arrangement and connectivity between these components.

D. Chiplet Power and Performance Comparison

The chiplet place-and-route (PnR) process is conducted using the footprint specifications detailed in Table II, employing a commercial 28nm Process Design Kit (PDK) and leveraging Cadence Innovus for the physical design, incorporating selected protocol translators and the I/O driver. Initially, the placement of I/O pins is determined based on micro-bump configurations for both signal and Power/Ground (P/G) pins. Furthermore, the I/O driver is preliminarily positioned as a hard macro adjacent to the micro-bump locations to minimize wire delay from the input to the micro-bump pad locations. Nonetheless, the Place and Route (PnR) tool is granted flexibility during the optimization phase to adjust placements for enhanced timing closure. The arrangement of bump-to-Advanced Interface Bus (AIB) nets and the I/O driver within the glass interposer's chiplet is depicted in Fig. 7. The serialization module's placement is determined by the auto-placement engine to refine its location strategically. The definitive layout for each chiplet is presented in Fig. 9, with the power and performance metrics for each chiplet enumerated in Table III. A target frequency of 700MHz is established for both logic and memory chiplets across all design variants.

From Table III, it is observed that the majority of chiplets achieve closure at a frequency of 700MHz. Notably, the chiplet utilizing a glass 2.5D interposer exhibits the most compact footprint in comparison to chiplets associated with other interposer types. This distinction arises from the glass interposer's utilization of the smallest bump pitch. In the case of glass 3D, despite having a smaller bump pitch than Silicon 2.5D, the memory chiplet size is same because of the chiplet stacking between memory and logic chiplets. We also observe that the smaller chiplet size does not necessary provide

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TABLE III
POWER AND PERFORMANCE COMPARISON OF THE CHIPLETS USED IN OUR INTERPOSER DESIGNS. THE FP DENOTES THE FOOTPRINT OF THE CHIPLET IN mm. WE ALSO REPORT THE AREA AND POWER OVERHEAD OF INTEL AIB DRIVERS.

	Glass 2.5D		**Glass 3D**		**Silicon 2.5D**		**Silicon 3D**		**Shinko**		**APX**	
	Logic	**Memory**	**Logic**	**Memory**	**Logic**	**Memory**	**Logic**	**Memory**	**Logic**	**Memory**	**Logic**	**Memory**
Fmax (MHz)	686	699	684	697	689	698	687	694	676	697	690	694
FP ($mmxmm$)	0.82x0.82	0.77x0.77	0.82x0.82		0.94x0.94	0.82x0.82	0.94x0.94		0.94x0.94	0.82x0.82	1.1x1.1	1.0x1.0
Cell Count	167,495	37,091	166,871	37,087	167,495	37,090	166,124	37,272	167,042	37,102	167,779	37,219
Cell Utilization	64.20%	83.54%	64.14%	73.65%	48.70%	73.65%	48.40%	56.05%	48.80%	73.65%	34.00%	49.50%
Wirelength (m)	5.03	1.17	5	1.19	4.89	1.17	4.42	1.07	4.94	1.17	5.13	1.33
Tot. Power (mW)	142.35	46.06	141.73	45.9	138.76	45.6	133.4	44.85	141.9	45.85	141.93	47.29
→Internal	67.83	26.02	67.51	26.03	67.11	26.08	65.65	25.89	67.79	26.09	67	26.19
→ Switching	67.67	18.49	67.34	18.32	64.88	18.03	61.12	17.4	67.3	18.2	68.13	19.53
→ Leakage	6.85	1.55	6.87	1.55	6.76	1.54	6.64	1.54	6.84	1.55	6.79	1.55
Pin capacitance (pF)	395.11	162.42	395.4	81.5	390.2	81.5	381.5	80.9	394.54	81.58	390	81.82
Wire capacitance (pF)	696.24	81.76	700.2	161.6	665.1	158.9	634.8	150.1	684.27	161.12	703	174.6
AIB area (μm^2)	22,507 3.40%	17,388 2.90%	22,507 3.40%	17,388 2.90%	22,507 3.30%	17,388 2.90%	22,507 3.30%	17,388 1.90%	22,507 2.90%	17,388 2.80%	22,507 2.20%	17,388 1.70%
AIB power (mW)	0.54 0.40%	0.16 0.30%	0.54 0.40%	0.16 0.30%	0.59 0.40%	0.18 0.40%	0.35 0.26%	0.177 0.39%	0.59 0.40%	0.18 0.40%	0.54 0.38%	0.16 0.34%

the lower total power consumption because of higher routing congestion from the increased in switching power in the case of memory chiplet in glass 2.5D and glass 3D. Consequently, the power consumption across all chiplets demonstrates uniformity, with the power attributed to the I/O driver (AIB) being comparatively negligible to the overall power consumption.

The placement of micro-bumps in Glass 3D and Silicon 2.5D chiplets presents significant differences. In Glass 3D chiplets, micro-bumps are precisely aligned with those on the logic chiplet, whereas in Silicon 2.5D chiplets, the entire footprint area is utilized to accommodate all pins. This results in a larger footprint for the Silicon 2.5D logic chiplet, primarily due to its wider micro-bump pitch. Among the available interposer options, the APX interposer results in the largest chiplet size, which in turn reduces cell utilization efficiency. Power consumption remains relatively stable across different interposer types, with only minor variations. Additionally, the area and power overhead associated with the AIB I/O driver are negligible compared to the overall area and power demands of the chiplet.

In contrast to chiplet designs using interposers, the footprint area (FP) in Silicon 3D remains uniform for both logic and memory chips to enable die stacking. As a result, the memory chiplet in Silicon 3D demonstrates the lowest cell utilization compared to designs using glass and silicon interposers. Regarding wirelength, the logic chiplet in Silicon 2.5D exhibits a shorter wirelength than its glass counterpart, despite its larger footprint. This is due to routing congestion in the smaller footprint of the glass interposer, which increases wirelength. In Silicon 3D, the logic chiplet achieves a reduced wirelength even with the same footprint, owing to the distinct assignment of bumps and TSVs for I/O ports. The strategic placement of external TSV ports contributes to a shorter wirelength compared to conventional pin placements on the top metal layer. This wirelength reduction is also observed in the memory chiplet, following the same pattern as the logic chiplet. With the shortest wirelength, Silicon 3D achieves the lowest power consumption, primarily due to reduced switching power from lower wire capacitance. Pin capacitance remains relatively consistent across all designs, reflecting the number of cells used.

VI. INTERPOSER PLACE/ROUTE RESULTS

Upon acquiring the GDSII layouts for the chiplets corresponding to each interposer type, we proceeded to integrate these chiplets onto the interposers utilizing the Siemens Xpedition tool. Each chiplet is characterized by specific footprint dimensions and micro-bump locations designated for all Input/Output (I/O) and Power/Ground (P/G) pins.

A. Interposer Placement Method

Both signal and Power/Ground (P/G) bumps, along with the chiplet footprint, are defined within the commercial tool to represent the chiplet accurately. The assignment of signal and P/G bumps follows a structured unit pattern within a 2X4 grid array, where six of the eight bumps are allocated for signal transmission, and the remaining two serve as P/G bumps. This pattern is systematically repeated until all I/O pins are appropriately assigned. Subsequently, any micro bumps that are not utilized are removed to minimize routing obstruction in the design. In the final step, each micro-bump location is precisely labeled with the net name from the top-level netlist. This precise labeling ensures the accurate representation of both inter-tile and intra-tile connections within the commercial tool, aligning the physical design with the intended connectivity schema.

Upon assigning net names to the micro bumps on each chiplet, the dies are positioned according to the die-spacing constraints specific to each type of interposer. For the glass 3D interposer, the architecture uniquely embeds the memory chiplet directly beneath the logic chiplet at an identical location. This configuration facilitates connections through stacked vias in the Redistribution Layer (RDL), which efficiently uses the metal layers and shortens the length of interconnections. This arrangement capitalizes on the die-embedding capabilities intrinsic to the glass interposer. Utilizing two OpenPiton tiles, the placement of the second tile mirrors that of the first, ensuring that logic chiplets between tiles are interconnected.

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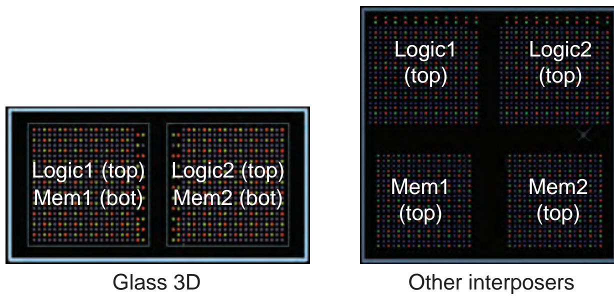

Fig. 10. Top-down view of the placement of the four chiplets, two logic and two memory. (a) logic and memory are stacked vertically in glass, (b) chiplets are placed side-by-side only in silicon, Shinko, and APX. See Fig. 1 for cross-sectional view.

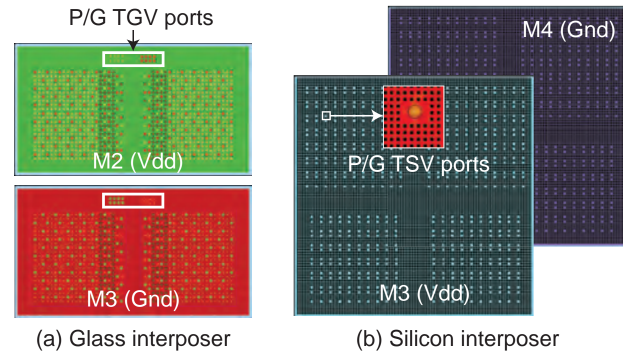

Fig. 11. Power delivery network of glass and silicon interposers.

This is necessitated by the placement of the Network-on-Chip (NOC) Router module within the logic chiplet, following chipletization and module grouping processes. Fig. 10(a) displays the die placement strategy employed for the glass 3D interposer. In contrast, for other substrates such as Glass 2.5D, Silicon 2.5D, Shinko (organic), and APX (organic), chiplets are arranged side-by-side, as depicted in Fig. 10(b). This is due to the substrate's limitation in supporting chiplet embedding.

B. Interposer Routing Method

An advanced metal stack configuration was designed specifically for the specifications of the interposer materials outlined in Table I. This methodology includes different routing strategies for glass, silicon, and organic interposers. For glass and silicon interposers, Manhattan-style routing is utilized in accordance with manufacturing guidelines, whereas diagonal routing is adopted for organic interposers to address their requirements for wider wire widths and constrained track space, thus maintaining the requisite micro-bump spacing. Auto-routing with guided directionality is employed to ensure a balanced comparison across different materials. Additionally, the power delivery network (PDN) has been enhanced by the inclusion of two additional metal layers, positioning the power metal layer directly above the ground metal layer, thus improving signal routing efficiency.

For the glass interposer, through-glass vias (TGVs) are incorporated to facilitate external power and ground connections, as depicted in Fig. 11(a). Power and ground are conFig.d as planes interconnected with vias to distribute power efficiently to the chiplets. In contrast, conventional through-silicon vias (TSVs) are employed for the silicon interposer, enabling the connection of external power and ground via C4 bumps. The power and ground planes for the Silicon interposer commence at metals 3 and 4, reflecting the requirement for a greater number of metal layers to complete signal routing compared to the glass interposer. For organic interposers, such as Shinko and APX, the power delivery network (PDN) is implemented similarly to that of the Silicon interposer. The completed layout of the interposer, showcasing the PDN, is illustrated in Fig. 12. The layout's dimensions articulate the comparative sizes and configurations of the various interposers.

C. Interposer Routing Comparison

Table IV shows that the Glass 3D interposer uses the fewest metal layers, with one for signal routing and two for power delivery, aided by stacked vias for vertical connections. In contrast, the Silicon 2.5D interposer requires one extra layer for routing, but due to its narrow line spacing, it does not need more layers than Glass 2.5D, Shinko, or APX.

Glass 3D achieves the shortest wirelengths by using stacked vias for intra-tile connections, while Silicon 2.5D has shorter wirelengths than Glass 2.5D and organic interposers due to finer line spacing. Glass 2.5D has longer wirelengths than Shinko due to Manhattan routing limitations, and APX has the longest wirelength due to its wider line width.

In summary, Glass 3D offers routing advantages, reducing wirelength, footprint, and cost compared to other interposers. The APX interposer shows the highest via usage, while the Glass 3D interposer achieves the smallest footprint through die stacking.

VII. Interposer Reliability Results

A. Interposer Signal and Power Integrity Analysis Method

The interposer transmission line, along with the I/O driver for both the driver and receiver, is modeled to facilitate signal transmission through the interposer wire and ultimately to the receiver end. An inverting signal is initially generated as an I/O driver. The selected I/O driver size, consistent with [3], is x128, featuring an output impedance of 47.4Ω. The model for the interposer transmission is created using HyperLynx Advanced Solver and subsequently converted into a SPICE netlist for timing and power simulation purposes. Following this, timing and power analyzes are conducted using custom-generated SPICE models, which incorporate the I/O drivers and the interposer model SPICE circuits.

To assess signal integrity, the longest net along with two adjacent nets within the interposer design are identified. The longest net is designated as the victim net, whereas the adjacent two are considered aggressors. A segment of the interposer layout, encompassing these three selected nets, is extracted to construct the S-parameter model utilizing the Siemens HyperLynx Advanced Solver tool. Subsequently, the S-parameter data is imported into Keysight Advanced Design System (ADS) for the creation of the eye diagram. The

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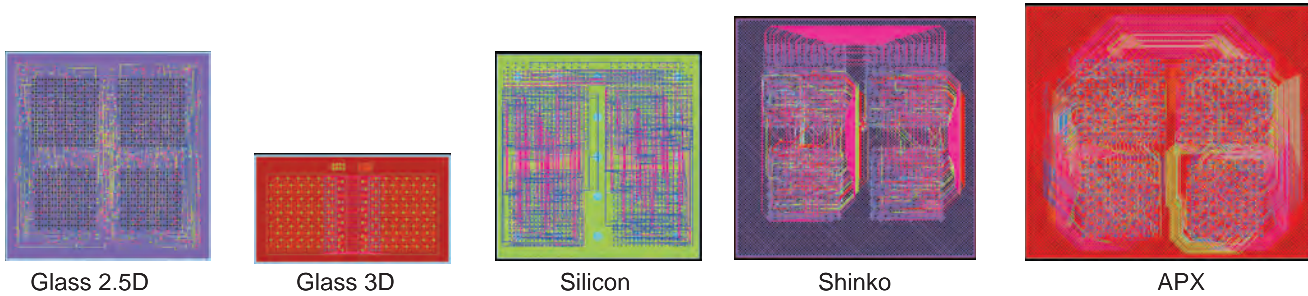

Fig. 12. Interposer routing layouts. All metals including signal and power/ground are superimposed in each design.

TABLE IV
INTERPOSER DESIGN RESULTS. ALL WIRE LENGTHS (WL) ARE REPORTED IN mm.

	2D Monolithic	Glass 2.5D	Glass 3D	Silicon 2.5D	Silicon 3D	Organic (Shinko)	Organic (APX)
Metal layer used ($signal + P/G$)	-	5 + 2	1 + 2	2 + 2	-	4 + 2	6 + 2
Total wirelength (mm)	-	924	29.69	620.21	-	803	881
Min wirelength (mm)	-	0.25	0.11	0	-	0.03	0.04
Average wirelength (mm)	-	1.75	0.43	0.5	-	1.4	1.6
Max wirelength (mm)	-	5.98	0.67	3.01	-	3.5	6.5
Via usage	-	3140	21 + 924	1542	-	2190	3178
Footprint ($mm \times mm$)	1.6 x 1.6	2.2 x 2.2	1.84 x 1.02	2.2 x 2.2	0.94 x 0.94	2.5 x 2.5	3.2 x 2.7
Area (mm^2)	2.56	4.84	1.87	4.84	0.883	6.25	8.64
Power (mW)	330.92	484.84	399.75	414.47	372.1	437.81	506.33
PDN Impedance (Ω)	-	20.7	0.97	7.4	-	180	58
Settling time (μs)	-	4.8	3.7	4.1	-	4.9	5.4
IR drop (mV)	-	18.6	17	27	-	23	17

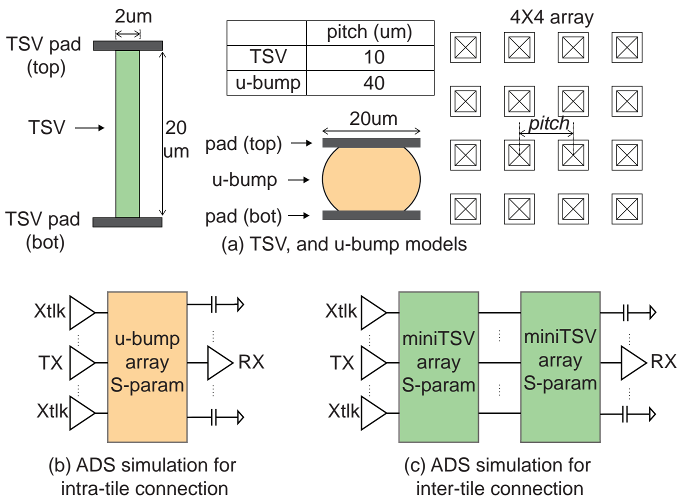

Fig. 13. F2F and B2B connection modeling using Keysight ADS tool: (a) ADS techbench for F2F, and (b) ADS testbench for B2B. Note that the S-parameter file are generated from Ansys HFSS.

simulations are conducted at a data rate of 0.7Gbps, with an I/O impedance of 50Ω, and take into account the parasitics of the receiver chiplet pad.

The power integrity of the design is evaluated by creating the Power Delivery Network (PDN) impedance profile from the interposer layout, utilizing the HyperLynx Advanced Solver tool. The PDN impedance simulation spans a frequency range from 10^6 to 10^9 Hz. Furthermore, power transient analysis is performed by extracting the S-parameter of the PDN and integrating it with an Integrated Voltage Regulator operating at 125MHz. This process allows for the measurement of voltage drop and the time required for voltage stabilization across each interposer type.

B. 3D Interconnect Modeling Method

Given that standard Through-Silicon Vias (TSVs) exhibit high parasitic effects and are sizeable, the decision was made to utilize mini TSVs for inter-tile connections, featuring a 2μm diameter and a 10μm pitch. To facilitate the integration of these smaller TSVs, the substrate is reduced to a thickness of 20μm. For intra-tile connections, a bump pitch of 40μm with a 20μm diameter is selected. The TSV and microbump arrays were modeled using Ansys HFSS, and their S-parameters were extracted with a port impedance of 50Ohm. These S-parameters are subsequently employed to calculate the resistance-capacitance (RC), create an equivalent circuit model (SPICE), and conduct signal integrity analysis. For inter-tile connections, two TSV S-parameter models are cascaded to represent the Back-to-Back (B2B) connections as depicted in Fig. 13. For intra-tile connections, the micro-bump model is utilized directly.

The micro-bump and Through-Silicon Via (TSV) models are developed based on [23]. Initially, an HFSS model is created to represent both the micro-bump and TSV as depicted in Fig.13(a). This model is structured in a 4X4 array to account for crosstalk from adjacent bumps or TSVs. The S-parameter is then extracted from the HFSS model and imported into the ADS tool for eye-diagram analysis. A victim bump is chosen alongside two neighboring aggressors, aligning the number of

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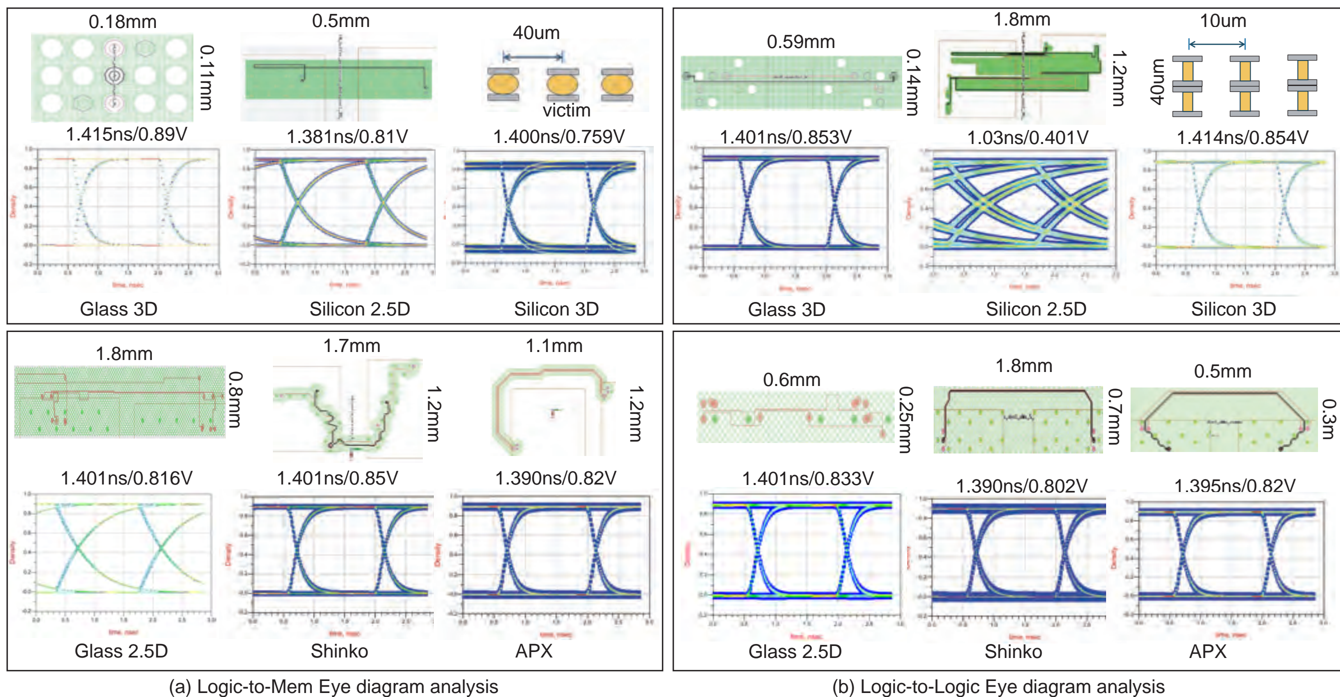

Fig. 14. Eye diagram comparison of the worst-case victim nets.

aggressors with those in the interposer designs for comparative analysis.

C. Signal Integrity Comparison

In the interposer layout, the S-parameter is extracted from the longest net to generate eye diagrams for each interposer type. Signal integrity analysis compares logic-to-logic (inter-tile) and logic-to-memory (intra-tile) connections across designs.

For logic-to-memory connections (Fig. 14), both Glass 3D and Silicon 3D use vertical stacking connections. Glass 3D employs 35µm-pitched stacked vias, while Silicon 3D uses 40µm-pitch micro-bumps. Other interposers, such as Glass 2.5D, Silicon 2.5D, APX, and Shinko, rely on lateral connections. Glass 3D shows the widest eye diagram (1.415 ns eye width, 0.89 V eye height), outperforming Silicon 3D due to its superior dielectric properties. Among lateral connections, Silicon 2.5D has the narrowest eye diagram due to longer wire lengths and limited metal layers. Glass 2.5D and Shinko show similar eye widths, but Glass 2.5D has a shorter eye height due to longer wire lengths and more vias. APX, with wider wire spacing, reduces crosstalk and achieves a broader eye than Silicon 2.5D.

For logic-to-logic connections, Silicon 3D has the widest eye diagram, benefiting from 3D interconnects. Glass 3D, despite using lateral connections, matches Silicon 3D's eye height but has a slightly narrower width. Silicon 2.5D performs the worst, with a 1.03 ns eye width and 0.401 V eye height, attributed to its long wire lengths. Glass 2.5D suffers from routing congestion, increasing crosstalk, while APX achieves a wider eye than Shinko due to its larger line spacing and thicker wires.

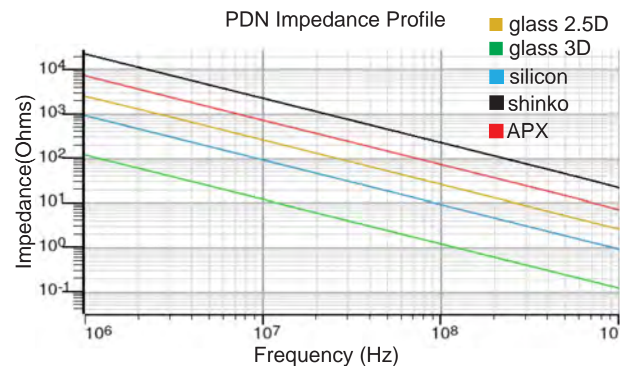

Fig. 15. PDN Impedance profile comparison for different type of interposers

In summary, Silicon 3D offers the best eye diagrams for logic-to-logic connections due to 3D stacking, but requires costly substrate thinning. Glass 3D delivers comparable signal integrity at a lower cost by avoiding extreme substrate thinning, performing well in both inter-tile and intra-tile connections.

D. Power Integrity Comparison

The impact of the power delivery network (PDN) impedance across various interposer materials was analyzed using a constant PDN density and a plane-type PDN configuration. As shown in Fig. 15, the Glass 3D interposer exhibits the lowest impedance, attributed to its favorable metal-to-dielectric thickness ratio and the use of thicker metal layers. Silicon interposers demonstrate the second-lowest impedance, while Glass 2.5D, APX, and Shinko interposers show higher impedance levels.

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The higher impedance observed in the Glass 2.5D interposer compared to Glass 3D and Silicon interposers is due to the increased distance between the PDN and the chiplet, as well as the need for more metal layers and vias. For the Shinko and APX interposers, the higher impedance is influenced by the PDN distance and the lower metal-to-dielectric thickness ratio. This impedance behavior is similar to that of capacitors, where impedance decreases at higher frequencies.

In the analysis of power transients and voltage drops, a 125 MHz switching power was applied to chiplets across all interposer types. The Glass 3D interposer exhibited the fastest settling time and the smallest voltage drop, attributed to its superior PDN impedance characteristics. Moreover, the Glass 3D interposer achieved the lowest system power consumption among the evaluated interposer materials, although it remains higher than that of 2D monolithic integrated circuits (ICs).

E. Interconnect/Interposer Delay and Power Analysis

Given the pipelined architecture, the timing budget for off-chip connections must remain within the clock period. HSPICE simulations, incorporating the AIB I/O driver, interposer line, micro-bumps or TSVs, and receiver, were performed to evaluate delay and power consumption.

For micro-bumps and TSVs, the S-parameter from HFSS was simplified from 32-port to 2-port and converted to a SPICE circuit using BBSpice in Keysight ADS. The interposer line subcircuit, derived from a real layout, captured the longest net for logic-to-logic and logic-to-memory connections. This S-parameter was converted into SPICE using HyperLynx.

Simulations were run at 700 MHz with a 0.9V supply, and driver (TX) and receiver (RX) strengths were set to 128X and 16X, respectively. The worst-case net for inter- and intra-tile connections was compared across Glass 3D, Silicon 2.5D, Silicon 3D, Glass 2.5D, Shinko, and APX designs (Table V).

For logic-to-memory connections, Silicon 3D shows the lowest delay and power due to minimal parasitics from micro-bumps. Glass 3D ranks second, benefiting from stacked vias. Silicon 2.5D has increased delay and power due to longer wirelengths and higher resistance. Glass 2.5D achieves better delay than APX, thanks to superior dielectric properties, while Shinko interposers have shorter wirelengths than APX and Glass 2.5D.

Similarly, for logic-to-logic connections, Silicon 3D performs best due to low-parasitic TSVs, despite the high cost of substrate thinning. Glass 3D ranks second with dedicated routing resources. Silicon 2.5D shows moderate wirelengths, while Glass 2.5D outperforms it in delay and power due to lower resistance. Organic interposers, like APX, exhibit longer wirelengths, resulting in higher delay and power, largely due to routing congestion and via usage.

In summary, Silicon 3D offers the best delay and power performance at the cost of substrate thinning, while glass interposers provide a low-cost solution with competitive performance.

F. Material impact on interposer delay and timing

We analyzed the impact of material properties on propagation delay and power across different interposer materials, as shown in Table VI. A transmission line model was developed using a pair of built-up vias and a 400 µm line, based on interposer specifications. The model, created with HyperLynx Advanced Solver, extracted a SPICE circuit to capture parasitic effects, and delay and power metrics were derived from HSPICE simulations, including I/O drivers and the interposer.

Table VI compares propagation delay (ps) and power consumption (µW) across interposers, with ”L2L” denoting logic-to-logic connections. APX interposer shows the lowest delay and power due to thicker metal lines, reducing resistance and power loss. The glass interposer ranks third in both metrics, while the silicon interposer exhibits the highest delay and power due to narrower wires, increasing resistance.

In summary, wire width plays a key role in propagation delay and power consumption. Shinko and glass interposers have similar line widths, but the larger via size in the glass interposer slightly increases capacitance, leading to marginally higher delay and power consumption.

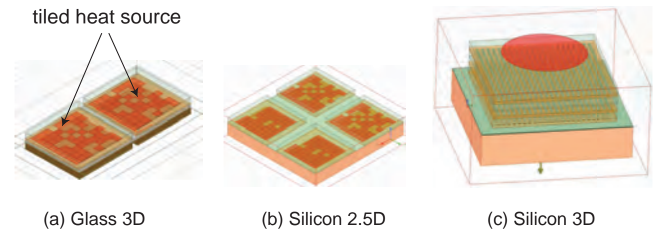

Fig. 16. Thermal model and extracted chiplet heat source in different interposers.

G. Interposer Thermal Reliability Results

Fig. 16. For thermal analysis, a Chip Thermal Model (CTM) for each chiplet is developed using Ansys Redhawk, incorporating tile-based power and metal density maps. An 8x8 power density map is generated with Ansys CPS, allowing finer granularity. In Ansys IcePak, the interposer is modeled using a coarse-grained tile approach, including the substrate, redistribution layer (RDL), micro bumps, and chiplets. Heat sources are applied to the bottom of flip-chip dies and the top of embedded dies, ensuring both packaging and chiplets are considered. Thermal performance is evaluated at a minimum airspeed of 0.1 m/s, confirming operation within temperature limits without active cooling, as shown in Fig. 16.

The thermal distribution across different interposer materials reveals that the memory chiplet in the Glass 3D interposer experiences higher temperatures compared to others, as shown in Fig. 17. The thermal number highlights the worst hotspot within the chiplet, driven by heat generated by the embedded die, which primarily dissipates through Through-Glass Vias (TGVs) to the Redistribution Layer (RDL).

In contrast, the logic chiplet in the Glass 3D interposer shows lower temperatures as its heat dissipates into the ambient air. Logic chiplets in other interposers maintain similar temperatures, typically between 27°C and 29°C. The peak temperatures for the Glass 3D interposer's logic and memory chiplets are 27°C and 34°C, respectively, whereas memory chiplets in other interposers range from 22°C to 23°C.

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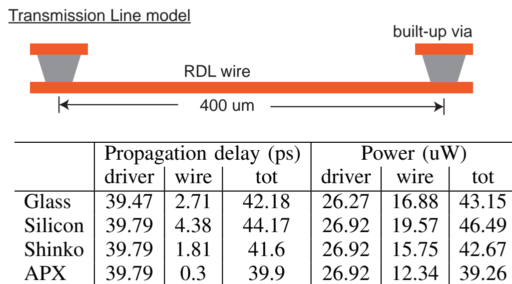
TABLE V
POWER AND PERFORMANCE COMPARISON OF THE SILICON 3D VERSUS GLASS INTERPOSER AND SILICON INTERPOSER (SILICON 2.5D).

	Monitor Net	Interconnect (μm)		WL	Propagation delay (ps)			Power (μW)		
		width	spacing	(μm)	IO drivers	Interconnect	total	IO drivers	Interconnect	total
Glass 3D	Logic-to-Mem	15	35	65 (thickness)	39.47	0.85	40.32	26.27	4.94	31.21
	Logic-to-Logic	2	2	582	39.47	2.71	42.18	26.27	20.54	46.81
Silicon 2.5D	Logic-to-Mem	0.4	0.4	1,952	39.79	17.77	57.56	26.92	65.82	92.74
	Logic-to-Logic			1,063	39.79	10.69	50.48	26.92	63.52	90.44
Silicon 3D	Logic-to-Mem	20	20	20 (bump)	39.79	0.29	40.08	26.92	1.26	28.18
	Logic-to-Logic	2	8	2TSVs	39.79	1.53	41.32	26.92	9.91	36.83
Glass 2.5D	Logic-to-Mem	2	2	5,980	39.47	6.63	46.1	26.27	200.8	227.07
	Logic-to-Logic			1,794	39.47	1.87	41.34	26.27	12.33	38.6
Shinko	Logic-to-Mem	2	2	3,700	39.79	31.88	71.67	26.92	92.45	119.37
	Logic-to-Logic			2,600	39.79	24.6	64.39	26.92	71.96	98.88
APX	Logic-to-Mem	6	6	5,900	39.79	43.66	83.45	26.92	194.38	221.3
	Logic-to-Logic			3,500	39.79	19.81	59.6	26.92	116.89	143.81

TABLE VI
INTERPOSER INTERCONNECT DELAY AND POWER COMPARISON. WE CHOOSE LOGIC-TO-LOGIC CHIPLET CONNECTIONS FOR THIS EXPERIMENT. THE WIRELENGTH IS FIXED AT $400um$ FOR ALL INTERPOSERS.



	Propagation delay (ps)			Power (uW)		
	driver	wire	tot	driver	wire	tot
Glass	39.47	2.71	42.18	26.27	16.88	43.15
Silicon	39.79	4.38	44.17	26.92	19.57	46.49
Shinko	39.79	1.81	41.6	26.92	15.75	42.67
APX	39.79	0.3	39.9	26.92	12.34	39.26

We analyze the thermal distribution across four interposer materials, as shown in Fig. 18. In the glass interposer, hotspots are concentrated in the chiplet area due to the insulating properties of the glass substrate, which limit heat conduction. In contrast, the silicon interposer shows a broader thermal spread with merged hotspots. For organic interposers, such as Shinko and APX, the Shinko thermal map is more concentrated than APX, due to the thin-film material properties. The maximum temperature in the glass interposer matches that of the memory chiplet, as heat becomes trapped in the substrate. However, active cooling mechanisms allow heat to dissipate more efficiently, localizing the hotspots. In the silicon interposer, heat dissipates between the logic and memory chiplets, leading to thermal expansion across the substrate.

Thermal distribution across four interposer materials, shown in Fig. 18, reveals concentrated hotspots in the glass interposer due to its insulating properties. Silicon interposers display broader thermal spread, while organic interposers like Shinko show more concentrated heat zones. The use of thermal vias could aid in transferring heat from the embedded die to the package substrate. However, larger thermal vias may increase the chiplet size, potentially affecting yield, which is why bottom-side cooling is often preferred [24]. In silicon interposers, heat dissipation occurs between logic and memory chiplets, contributing to higher temperatures in the die-to-die area.

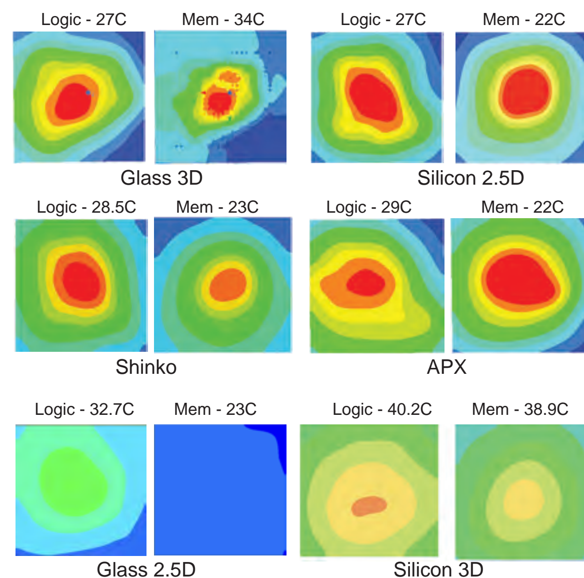


Fig. 17. Chiplet thermal distribution comparison. Our thermal analysis covers both the chiplets and the interposer for each interposer material choice.

H. Full-chip Timing and Power Analysis

To calculate total chip power, we sum the power consumption of networks within both intra- and inter-tile connections:

$$\text{total power} = P_{\text{chiplet}} + P_{\text{intra-tile}} + P_{\text{inter-tile}}$$

In timing analysis, the goal is to ensure that off-chip propagation delays do not exceed the clock period in the pipelined architecture. Table V shows that inter- and intra-tile delays in the Silicon 3D design meet clock period constraints, with the system's frequency set by the slowest chiplet (logic chiplet at 684 MHz).

For non-pipelined architectures, 3D interconnect RC parasitics are specified for off-chip connections. The netlist captures off-chip chiplet linkages, and static timing analysis extracts timing and power metrics.

Table IV compares Power, Performance, and Area (PPA) for Silicon 3D, Glass interposer, and Silicon 2.5D, highlighting trade-offs across integration technologies.

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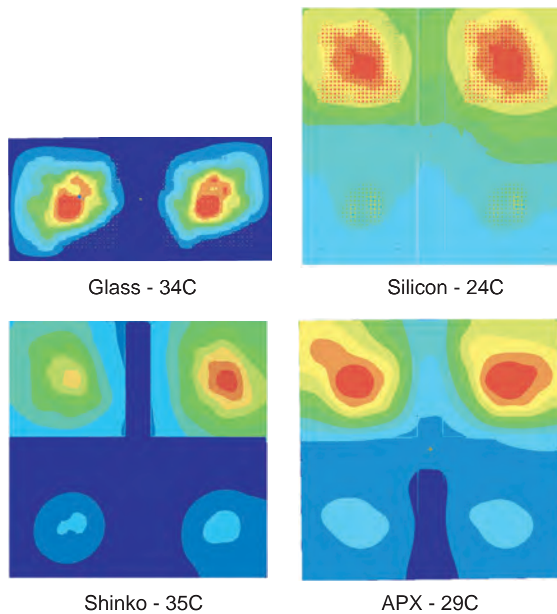

Fig. 18. Interposer thermal distribution comparison. Our thermal analysis covers both the chiplets and the interposer for each interposer material choice.

VIII. CONCLUSION

We present a novel 5.5D IC chiplet integration approach utilizing a glass interposer, co-designed with the chiplet. This approach analyzes key factors such as Power, Performance, Area (PPA), interposer routing efficiency, signal/power integrity, and thermal distribution, compared to silicon and organic interposers. The glass interposer shows clear advantages, including shorter wire lengths, reduced footprint, and improved signal and power integrity over conventional 2.5D technologies. Additionally, our chiplet partitioning strategy maintains the embedded die's thermal conditions within acceptable ranges. While Silicon 3D technology offers better performance and power efficiency, it suffers from higher thermal dissipation and manufacturing costs. In contrast, the glass interposer provides better thermal management and remains a cost-effective solution for 3D chiplet stacking, with superior signal and power integrity.

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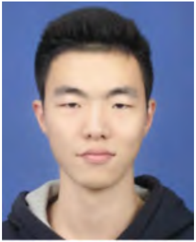

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