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Gate structuring on n-type bilayer MoS_2 field-effect transistors for ultrahigh current density

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Junyoung Kwon[1,6], Kyoung Yeon Kim[2,6] ✉, Dongwon Jang[3,6], Min Seok Yoo[1], Alum Jung[1], Dong-Su Ko[1], Yoonhoo Ha[1], Huije Ryu[1], Woon Ih Choi[2], Yeonchoo Cho[1], Changhyun Kim[1], Eunji Yang[1], Eun Kyu Lee[1], Chang-Seok Lee[1], Sang Won Kim[1], Uihui Kwon[2], Dae Sin Kim[2], Sung Kyu Lim[4] ✉, Kyung-Eun Byun[1] ✉, Minsu Seol[1] ✉ & Jeehwan Kim[1,5] ✉

The foundry industry and academia are confronting the limits of Moore's Law scaling for logic transistors. Silicon field-effect transistors (FETs) now rely on gate-all-around structures and ultrathin channels, even at the cost of decreased carrier mobility and complex fabrication processes. Two-dimensional (2D) semiconductors offer a promising alternative because they retain their crystalline quality at atomic thicknesses. Nonetheless, whether they truly exhibit higher performance than silicon remains questionable. Here, by implementing a dual-gate structure on bilayer MoS_2 FETs, we mitigate the fringing-field barrier created by the elevated top contact and achieve high carrier densities without increasing fabrication complexity. Simulations and statistical analysis confirm that the dual-gate compensates the fringe field, enabling a drain current of 1.55 mA μm^{-1} even with conventional gold contacts. Quantum-transport simulation indicates that, with further gate-length and equivalent-oxide-thickness scaling, the on-state current can reach levels comparable to silicon FETs at the 3-nm node, and monolithic 3D integration can extend the applicability of dual-gate 2D transistors to future logic technologies.

Silicon field-effect transistors (FETs) are now reaching the physical limit of gate-length (L_g) scaling. To keep improving electrostatic control, the semiconductor industry has successively enlarged the gate–channel interface area: from planar, through Fin-FET, and now to gate-all-around (GAA) FET[1,2]. At the same time, channel thickness has been reduced to strengthen gate coupling, but silicon carrier mobility collapses sharply below 5 nm, causing a large loss of on-state current (I_{on})[3]. Multichannel architectures could, in principle, restore current, yet they require new and highly challenging contact and gate processes and still cannot sustain Moore's Law for nodes below 1 nm (refs. 4–6). Two-dimensional (2D) transition-metal dichalcogenides (TMDs) have emerged as a compelling alternative. Because a monolayer or bilayer crystal retains high mobility even at 1- to 2-nm thickness, its channel can be fully electrostatically controlled at $L_g \approx 5$ nm or less[3,7,8]. Consequently, ultrathin geometry also allows a dual-gate design to achieve the same electrostatic control as a GAA structure. Moreover, large-area growth or transfer of TMDs onto

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A full list of affiliations appears at the end of the paper. ✉e-mail: k77y.kim@samsung.com; limsung@usc.edu; ke14.byun@samsung.com; minsu.seol@samsung.com; jeehwan@mit.edu

amorphous substrates is straightforward, which makes the sequential fabrication of dual-gate structures relatively easy[9–11]. Despite these advantages, most high-performance 2D TMD FETs reported to date use a single-gate architecture[12,13], probably because (1) many researchers have believed that the ultrathin channel needs only one gate for sufficient accumulation, and (2) forming a high-quality top-gate dielectric on chemically inert 2D surfaces is technically difficult[14].

In this study, to maximize carrier density in the channel we deliberately introduced a dual-gate configuration on monolayer and bilayer MoS_2. Technology computer-aided design (TCAD) simulations uncovered a previously overlooked potential barrier generated by the fringing field of the elevated source/drain contacts. This barrier hampers the accumulation of a high carrier density in the channel, and is especially problematic in bilayer devices; therefore, adding a top-gate to the conventional single back-gate can partially cancel the field and lower the barrier. Consequently, simulations predict that for monolayer devices the introduction of a dual-gate yields roughly a 2-fold increase in I_{on} compared with a single-gate, whereas for bilayer devices an increase as large as 5-fold is anticipated. Statistical experiments on 200-mm-scale monolayer and bilayer MoS_2 wafers confirm this expectation: dual-gate devices exhibit ~2-fold higher I_{on} for monolayer and ~3.5-fold higher I_{on} for bilayer, and the transfer-length-method (TLM) shows a pronounced reduction of contact resistance (R_C) in bilayers, exactly as the simulations anticipate. By concentrating the electric field of both gates on an ultrathin channel, the dual-gate architecture raises the sheet carrier density (n_{2D}) to 5.5×10^{13} cm^{-2}. Such a massive number of carriers can flow efficiently, enabling an outstanding I_{on} of 1.55 mA μm^{-1} even with the moderate carrier mobility of polycrystalline MoS_2 and conventional gold contacts. High-*k* dielectrics on both sides of the channel also lower the operating voltage, bringing the device closer to the voltage window of industrial silicon transistors.

Finally, quantum-transport TCAD simulations, performed on a supercomputer with an in-house solver, were used to evaluate the scalability of our devices beyond the 3-nm node. The calibrated model reproduces the experimental data and shows that silicon GAAFETs suffer severe short-channel effects for $L_g < 12$ nm, whereas the MoS_2 dual-gate FET retains performance down to $L_g = 5$ nm. The reduced contacted-gate pitch (CGP) and the intrinsically low parasitic capacitance of the atomically thin channel promise power-performance-area (PPA) advantages over silicon GAAFETs. Moreover, the ability to transfer or selectively grow single-crystal 2D layers on amorphous substrates supports monolithic 3D (M3D) integration concepts, making dual-gate bilayer TMD FETs a promising pathway for sub-1-nm technology nodes[9,10].

I_{on} and electrical potential in single- and dual-gate MoS_2 FETs as predicted by TCAD simulations

Monolayer MoS_2, a widely recognized 2D semiconductor, provides excellent gate control but its large bandgap limits performance[15,16]. Bilayer MoS_2 has higher mobility and a smaller bandgap, reducing the Schottky barrier and improving performance[17,18]. Its larger quantum capacitance also yields higher carrier density[19]. Hence, a dual-gate on bilayer MoS_2 should combine strong gate control with high performance, making it a promising architecture. We first evaluated dual-gate effects on monolayer and bilayer MoS_2 with TCAD simulations. We also examined the impact of the elevated top contacts. Unlike silicon, 2D TMDs cannot be heavily doped and therefore metal contacts must be made directly on the undoped channel[20]. Consequently, a strong fringing field arises from the metal-channel potential and work-function difference and from the surface dipole[21]. Previous work shows that this fringing capacitance substantially affects the contact potential and device current[22]. We hypothesize that a dual-gate can compensate this effect and improve performance.

A back-gate MoS_2 FET can be fabricated readily and adding a top gate yields the dual-gate architecture (Fig. 1a). Here, high performance requires balanced top- and bottom-gate stacks[23]. However, forming a high-quality top-gate dielectric layer on a 2D material is challenging due to the noble surface, as widely acknowledged[24]. We utilized a low-temperature interlayer deposition method to deposit the high-quality top-gate dielectric[14]. Gold was chosen for the source-drain and gate electrodes to eliminate artefacts originating from the native oxides. Figure 1b,c respectively shows top-view scanning electron microscopy (SEM) and cross-sectional transmission electron microscopy (TEM) images of the dual-gate device.

The TCAD model was built directly from the measured device geometry (Fig. 1d). Earlier 2D material simulations did not fully consider the true electrode shape and relied on silicon-based tools that treat the channel only as a thickness-scaled bulk, which leads to large errors[25–27]. To accurately capture the physics of bilayer MoS_2, we explicitly incorporated the van der Waals (vdW) gap between the two layers and used experimentally validated material parameters (Extended Data Table 1). Using this geometry we simulated four configurations: monolayer/bilayer combined with single-gate/dual-gate, under gate-source voltage $V_{gs} = 3$ V and drain-source voltage $V_{ds} = 1$ V. For the monolayer, adding a top gate roughly doubles the total gate capacitance, giving an ~2-fold increase in electron density and I_{on}. In the bilayer the dual-gate device shows an ~5-fold I_{on} boost relative to the single-gate case; the extra gain (marked by a question mark in Fig. 1e) exceeds the simple capacitance scaling and originates from a reduction of a contact-side potential barrier. Transfer curves (Extended Data Fig. 1) reveal that the threshold voltage (V_{th}) is unchanged, while the subthreshold swing (SS) and leakage improve because short-channel effects are suppressed.

Figure 1f–g shows the simulated on-state electrostatic potential of monolayer and bilayer MoS_2 FETs (see Supplementary Fig. 1 for enlarged view). In both devices a pronounced potential drop appears near the source electrode when only a back gate is used; this drop disappears when a top gate is added. The corresponding conduction-band-edge and electron-density line profiles (Fig. 1h–i) reveal that the narrow metal-channel gap produces a strong fringing field that lifts the conduction band, creating an energy barrier that suppresses charge injection. In the bilayer, the top MoS_2 layer—directly contacted by the metal—experiences the largest barrier because the bottom layer screens the gate field. Meanwhile, the top gate efficiently compensates the fringing field at the top layer and therefore reduces the barrier height. (For the bottom layer, see Supplementary Fig. 2.) In contrast, in the monolayer the barrier is already tightly regulated by the back gate and changes only marginally. We demonstrated a low-fringing-field structure, suppressing the fringing field and consequently lowering the barrier. A low-fringing-field geometry further lowers the barrier and raises I_{on} (Supplementary Fig. 3). Capacitance-model analysis (Supplementary Fig. 4) confirms that the barrier-reduction effect yields more than 2-fold I_{on} improvement for bilayers. Length-scaling simulations (Supplementary Fig. 5) show that the I_{on} ratio between single- and dual-gate devices remains essentially constant up to a channel length (L_{ch}) of 300 nm, indicating that the improvement is rooted in contact-side barrier mitigation rather than channel-length effects. In addition to the I_{on} boost, the dual-gate configuration also improves SS and reduces leakage (Extended Data Fig. 1).

Growth of 200-mm-scale wafer monolayers and bilayers of MoS_2

After our simulations demonstrated that a bilayer MoS_2 channel provides a clear electrostatic advantage over a monolayer, we shifted our focus to the far more demanding task of fabricating a wafer-scale, uniform bilayer on a 200-mm wafer—a milestone that has been reported infrequently because wafer-scale, layer-by-layer growth is intrinsically difficult[28,29]. By introducing a small amount of potassium-iodide (KI) additive into the metal–organic chemical vapour deposition (MOCVD) chemistry, we substantially increased the surface diffusion length of the molybdenum and sulfur adatoms. This change allowed us to suppress

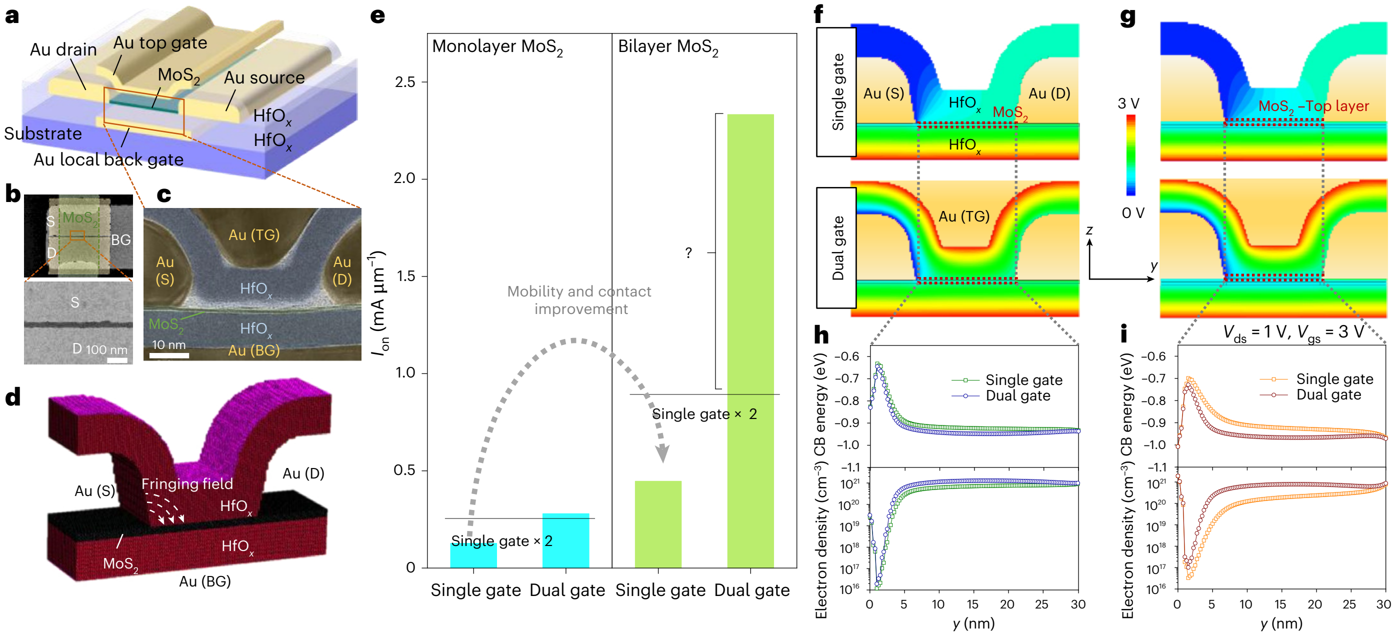

Fig. 1 | TCAD simulation results based on the actual MoS_2 dual-gate FET. **a**, Schematic illustrating the MoS_2 dual-gate FET with elevated gold contacts. **b**, False-colour top-view SEM images of a device with an L_{ch} of 30 nm among the actually fabricated MoS_2 FETs before the fabrication of the top gate. S, source; D, drain; BG, back gate. **c**, False-colour cross-sectional TEM image of a representative MoS_2 dual-gate FET. **d**, TCAD simulation model of the MoS_2 dual-gate FET fabricated based on the observed TEM image. MoS_2 is represented in black, HfO_x in red, and the S, D and BG metals are implemented in the form of the potential touching the surface. The top surface, represented in purple, is calculated as empty in the case of single-gate simulation and with the potential of the gold in the case of dual-gate simulation. The reproduction of such an elevated contact structure in the simulation makes it possible to calculate the role played by the fringing field. **e**, The I_{on} values calculated through TCAD modelling for single- and dual-gate configurations in monolayer (sky blue) and bilayer (yellowish green) MoS_2 FETs. The on-state is defined at $V_{ds} = 1$ V and $V_{gs} = 3$ V. Primarily, due to the smaller bandgap in bilayer MoS_2, an ~3-fold increase in I_{on} was calculated in the same single-gate configuration compared with the monolayer. An ~2-fold increase in I_{on} in the dual gate compared with the single gate is expected due to the 2-fold gating effect. However, in the case of bilayer, a >2-fold unidentified increase in I_{on} is observed. **f**, Visualized electrical potential of a monolayer MoS_2 FET in HfO_x and MoS_2 at the on-state ($V_{ds} = 1$ V, $V_{gs} = 3$ V) for both single- and dual-gate configurations. **g**, Visualized electrical potential of a bilayer MoS_2 FET in HfO_x and MoS_2 at the on-state for both single- and dual-gate configurations. **h**, Line profile along the *y* direction of the conduction band (CB) energy and corresponding electron density within monolayer MoS_2. While the presence of a fringing field-induced barrier near the source electrode is evident, the difference between single- and dual-gate configurations is not substantial. **i**, Line profile along the *y* direction of the CB energy and corresponding electron density within the top layer of bilayer MoS_2. The reduction in the barrier due to the introduction of the dual gate through the fringing field is clearly evident.

premature nucleation of secondary layers, thereby extending the lateral growth of the first layer until it coalesced, after which the second layer could nucleate uniformly. The result is a bilayer-dominated MoS_2 film that spans the entire 200-mm wafer, as confirmed by the subsequent statistical analyses (see Supplementary Fig. 6 and Supplementary Fig. 7 for SEM and plan-view TEM images of bilayer MoS_2 film).

Figure 2a,b respectively displays cross-sectional TEM images of the grown monolayer and bilayer MoS_2 films. In Fig. 2c, characteristic Raman peaks of monolayer and bilayer MoS_2, including E^1_{2g} and A_{1g} peaks, along with the silicon substrate peak near 520 cm^{-1}, are presented. The intensity of the *A* peak relative to the silicon peak is substantially higher in the bilayer than in the monolayer. Moreover, the distance between the *E* and *A* peaks directly related to the layer number is precisely in line with the values reported in the literature, measuring 19.8 cm^{-1} for the monolayer and 21.9 cm^{-1} for the bilayer[30]. Of course, it would be challenging to claim that the entire film is perfectly monolayer or bilayer, due to the presence of adlayer patches. However, through statistical Raman analysis, we can track the average number of layers. In Fig. 2d, the distribution of the analysed *E*–*A* peak distances from 100 Raman spectra within a 10 cm × 10 cm area of as-grown MoS_2 films is plotted. Also, as evident from the Raman mapping in Extended Data Fig. 2, it can be confirmed that a generally uniform monolayer and bilayer were fabricated. We also analysed the compositions of the two films to be nearly identical using X-ray photoelectron spectroscopy (XPS) analysis. The composition ratios derived from the molybdenum (Mo) 3*d* peak (Fig. 2e) and the sulfur (S) 2*p* peak (Fig. 2f) for the monolayer and bilayer are respectively 32.91:67.09 and 32.41:67.59, indicating a negligible difference in quality, with only a difference in layer number. The slight redshift observed in both the Mo and S peaks of the bilayer seems to result from the mitigation of the substrate effect and enhanced screening. Additionally, it has been confirmed in Supplementary Fig. 6 that the KI additive used during the bilayer MoS_2 growth remains after growth but is easily removable in most solvents such as acetone, alcohols or water. Consequently, after the transfer and subsequent processes, it is undetectable by atomic force microscopy (AFM) and XPS, as shown in Supplementary Fig. 8.

Statistical assessment of monolayer and bilayer MoS_2 FETs with single- and dual-gate configurations

Using the wafer-scale mono- and bilayer MoS_2 films, we fabricated FET arrays on 200-mm wafers (Fig. 3a, inset). The devices have the same architecture as the TCAD model shown in Fig. 1a; the detailed process flow is given in Supplementary Fig. 9 and the Methods, and cross-section TEM images are shown in Fig. 1c and Supplementary Fig. 10. To directly compare single-gate and dual-gate operation we measured each transistor before and after adding the top-gate metal. The top-gate-only configuration was not studied in the scaled devices because its electric field contributes little to contact-region doping, whereas the back gate strongly modulates the contacts in the on-state. Extended Data Fig. 3 (L_{ch} > 500 nm devices made by photolithography) confirms that top-gate-only devices show 10-fold lower performance

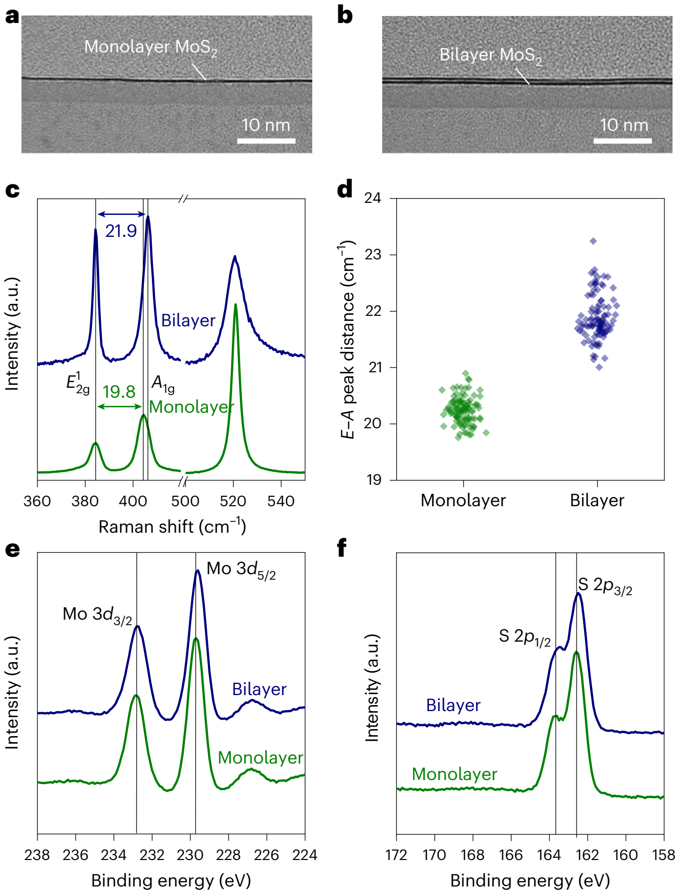

Fig. 2 | Characterization of 200-mm-scale MoS$_2$ film. a, Cross-sectional TEM image of a monolayer MoS$_2$ film. **b**, Cross-sectional TEM image of a bilayer MoS$_2$ film. **c**, Representative Raman spectra of monolayer and bilayer MoS$_2$ film. A clear blue-shift of the A_{1g} peak resulted from the increase in the layer number, leading to the enhanced distance between peaks A_{1g} and E^1_{2g}. The peak around 520 cm^{-1} on the far right is attributed to silicon, and, likewise, an increase in the layer number leads to both broadening and a decrease in intensity. **d**, Distribution of the E–A peak distances obtained from Raman spectra at 1-cm intervals across a 10 cm × 10 cm area for monolayer and bilayer MoS$_2$ films. The distinct separation of film thickness is clearly evident on average. **e**, XPS of Mo 3d peaks in monolayer and bilayer MoS$_2$. **f**, XPS of S 2p peaks in monolayer and bilayer MoS$_2$. The Mo:S atomic ratio, derived from the XPS of Mo and S, is 32.91:67.09 for the monolayer and 32.41:67.59 for the bilayer. a.u., arbitrary units.

than back-gate devices, which is attributed to the lower quality of the top-gate dielectric and the absence of contact gating.

Transfer curves (sheet conductance σ_{sh} versus V_{gs}) for hundreds of monolayer and bilayer MoS$_2$ FETs (Fig. 3a,b) were measured over L_{ch} ranging from 30 nm to 300 nm; σ_{sh} normalizes the current to device geometry. In every case the dual-gate configuration yields lower SS and higher I_{on} than the single-gate device. Plotting I_{on} versus L_{ch} (Fig. 3c,d) shows a pronounced increase for dual-gate transistors across the entire L_{ch} range, consistent with the long-channel TCAD results (Supplementary Fig. 5) and the statistical analysis of long-channel devices (Extended Data Fig. 3). Moreover, we demonstrated that inserting a low-k SiO$_2$ spacer between metal and channel reduces the fringing field, further raising I_{on} and tightening device-to-device variation (Extended Data Fig. 4). The experimental improvement matches the low-fringing-field simulations (Supplementary Figs. 3 and 4). Despite being fabricated from polycrystalline MoS$_2$, the bilayer-dual-gate FETs deliver an average I_{on} of 700 µA µm^{-1} at an L_{ch} of 30 nm. In bilayers the I_{on} gain from the dual gate is essentially constant across all L_{ch} values, whereas in monolayers the gain becomes larger as the channel length increases. This trend reflects the different operating regimes: short-channel devices are contact limited, while longer devices are channel limited. To elucidate the origin of the gain we performed transfer-length-method (TLM) analysis on devices of varying L_{ch} (Extended Data Fig. 5). After converting the gate voltage to overdrive voltage (V_{od}) and then to n_{2D} using capacitances extracted from metal–insulator–metal (MIM) test structures (Supplementary Fig. 11), we plotted R_C versus n_{2D} (Fig. 3e,f). Both mono- and bilayer devices exhibit roughly ~2-fold larger gate capacitance in the dual-gate configuration, giving a broader n_{2D} range. For monolayers the lowest R_C is similar for single- and dual-gate devices (~4 kΩ µm), consistent with the simulated minimal barrier difference. In contrast, bilayers show a dramatic reduction of R_C from 4.3 kΩ µm (single gate) to 1.3 kΩ µm (dual gate), in line with the simulated barrier mitigation as previously shown in Fig. 1h,i. Consequently, the dual-gate monolayer I_{on} is ~2-fold higher, while the bilayer I_{on} is ~3.6-fold higher (Fig. 3g), matching the TCAD prediction (Fig. 1e). The extra boost in bilayers arises from the dual gate's ability to compensate the fringing-field-induced barrier at the elevated contacts.

Figure 3h shows the partition of total resistance into R_C and channel resistance (R_{ch}). For the shortest L_{ch} = 30 nm devices, R_C dominates; the dual-gate reduces R_{ch} (and, for bilayers, also R_C), yielding a large overall resistance drop. The experimental mobility extracted by TLM varies between single- and dual-gate devices (Supplementary Fig. 12), indicating that the dual-gate field improves carrier accumulation and thus effective mobility. Stacking order and occasional defects have only a minor effect (Supplementary Fig. 13). Overall, the data confirm that a dual-gate architecture is essential to fully exploit the thin-channel advantage of 2D materials, especially for bilayer MoS$_2$ where it both lowers the contact barrier and enhances channel conductance.

Benchmarking I_{on} of dual-gate bilayer MoS$_2$ FET and further L_g scaling with quantum transport simulation

To probe the ultimate current capability of MoS$_2$ we selected the best bilayer-dual-gate device (the 'hero' transistor) and extended the gate bias to +4 V. With a V_{th} of ~−1.4 V, the channel reaches an n_{2D} of ~5.5 × 10^{13} cm^{-2}. Because the equivalent oxide thickness (EOT >3 nm) makes the oxide capacitance much smaller than the quantum capacitance, the classical capacitance model accurately predicts this density[19,31]. The transfer curve (Fig. 4a) shows only a mild saturation at high V_{gs}, indicating that the bilayer can accommodate still larger carrier populations; a transconductance peak appears in the high-V_{gs} region (Supplementary Fig. 14). The output characteristic (I_{ds}–V_{ds}, Fig. 4b) is linear at low V_{ds}, confirming ohmic contacts. From the slope we extract a total resistance of ~600 Ω µm at V_{gs} = 4 V, which corresponds to a contact-plus-channel resistance of ~300 Ω·µm and yields an outstanding I_{on} of 1.55 mA µm^{-1} despite a moderate mobility (~20 cm^2 V^{-1} s^{-1}). The top-ten highest-I_{on} devices are shown in Supplementary Fig. 15. The lower R_C observed here, compared with the TLM-extracted value in Fig. 3, stems from the much higher n_{2D} (5.5 × 10^{13} cm^{-2} versus 1.7 × 10^{13} cm^{-2}) used in this measurement.

Figure 4c,d presents a benchmark of the I_{on} of our n-type bilayer MoS$_2$ dual-gate FETs against reported 2D devices. To focus on logic-relevant operation we excluded devices that draw current at V_{ds} > 3 V and plotted I_{on} versus V_{ds} (Fig. 4c). Even with the simple dual-gate/bilayer architecture, our transistors deliver a higher I_{on} than single-crystal MoS$_2$ FETs and surpass the I_{on} target set by the IEEE International Roadmap for Devices and Systems 2022 roadmap[4]. Importantly, this performance is achieved at relatively low V_{ds}, whereas many previously reported high-I_{on} 2D FETs operate at high V_{ds} or require large V_{gs} (tens of volts) because of a highly negative V_{th} or use of high EOT dielectrics[12,13,28,32–37]. To enable a fair comparison we therefore plotted I_{on} versus the overdrive voltage (V_{od}) (Fig. 4d). The data show that most high-I_{on} MoS$_2$ devices rely on high V_{od}, explaining why few 2D a.c. circuits have been demonstrated[26,38,39]. Our device attains a competitive I_{on} at

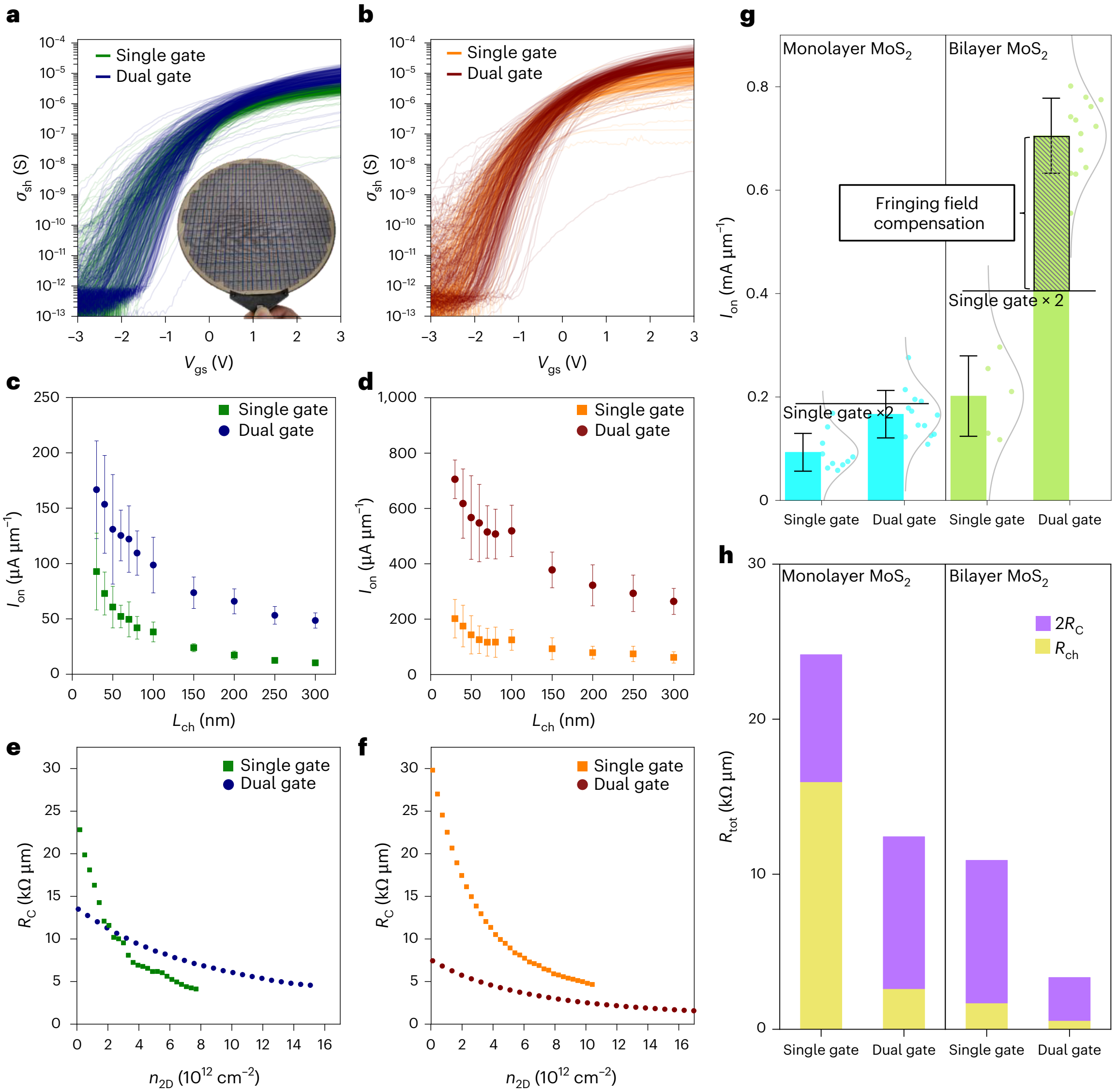

Fig. 3 | Statistical electrical property analysis of a 200-mm-scale FET array. **a**, Transfer curves (σ_{sh}–V_{gs}) of fabricated monolayer MoS$_2$ FETs with single- and dual-gate configurations. The transistor L_{ch} varies from 30 nm to 300 nm, and the channel width varies from 500 nm to 3 μm. To normalize for the various channel dimensions, the *y* axis is plotted in terms of conductance. Inset: photograph showing the MoS$_2$ FET array fabricated on a 200-mm wafer. For the single-gate devices, 271 out of a total of 324 devices were measured; for the dual-gate devices, 317 out of a total of 324 devices were measured. **b**, Transfer curves of bilayer MoS$_2$ FETs with single- and dual-gate configurations. For the single-gate devices, 202 out of a total of 324 devices were measured; for the dual-gate devices, 282 out of a total of 324 devices were measured. **c**, Graph plotting the I_{on} values extracted from transfer curves at V_{ds} = 1 V and V_{gs} of 3 V of a monolayer MoS$_2$ FET array as a function of L_{ch}. For the single gate, we measured 10 devices for L_{ch} = 30 nm, 52 for 40 nm, 67 for 50 nm, 16 each for 60, 70, 80, 150, 200, 250 and 300 nm, and 15 for 100 nm; for the dual gate, we measured 13 devices for 30 nm, 69 for 40 nm, 85 for 50 nm, and 18 each for 60, 70, 80, 100, 150, 200, 250 and 300 nm. **d**, The same graph of a bilayer MoS$_2$ FET array. For the single gate, we measured 5 devices for L_{ch} = 30 nm, 32 for 40 nm, 55 for 50 nm, 14 for 60 nm, 15 for 70 nm, 14 for 80 nm, 14 for 100 nm, 16 for 150 nm, 16 for 200 nm, 16 for 250 nm and 17 for 300 nm; for the dual gate, we measured 13 devices for 30 nm, 57 for 40 nm, 78 for 50 nm, 16 for 60 nm, 15 for 70 nm, 16 for 80 nm, 17 for 100 nm, 17 for 150 nm, 17 for 200 nm, 18 for 250 nm and 17 for 300 nm. **e**, Graph plotting the statistically extracted R_C from the monolayer FET array using the TLM method as a function of the n_{2D}. The minimum R_C values for single- and dual-gate configurations are at a similar level. **f**, The same graph for the bilayer FET. A pronounced drop in R_C is cleanly observed in the dual-gate configuration. **g**, The average I_{on} for both single- and dual-gate configurations in bilayer and monolayer MoS$_2$ FET arrays with a 30-nm L_{ch}. As predicted in the simulation, an ~2-fold increase in current was observed in the dual gate compared with the single gate in the monolayer, and similarly, a >2-fold increase in current was observed in the bilayer. As validated by the simulation, it was discovered that this additional increase in current is due to the compensation of the fringing field by the top gate. For the monolayer, 10 single- and 13 dual-gate FETs were measured; for the bilayer, 5 single- and 13 dual-gate FETs were measured. **h**, Total resistance (R_{tot}) of single gate and dual gate configurations for monolayer and bilayer FETs with a L_{ch} of 30 nm. 2R_C (purple) and channel resistance (R_{ch}) (yellow) extracted through TLM are shown. All data in this figure are presented as mean values ± s.d.

supply voltage (V_{dd}) comparable to that of a 45-nm silicon transistor (L_g ≈ 30–40 nm, V_{dd} ≈ 1 V), although a direct Si–MoS$_2$ comparison is limited by the larger EOT of our gate stack[40,41].

Because today's lithography, high-*k* gate-oxide deposition and reliable doping techniques are not yet compatible with MoS$_2$, a direct I_{on} comparison with state-of-the-art silicon FETs is difficult. To determine whether our dual-gate bilayer device can outperform silicon under aggressive (L_g < 10 nm) scaling we carried out quantum-transport simulations. Non-equilibrium Green's function (NEGF) calculations were performed with an in-house solver on a supercomputer, using

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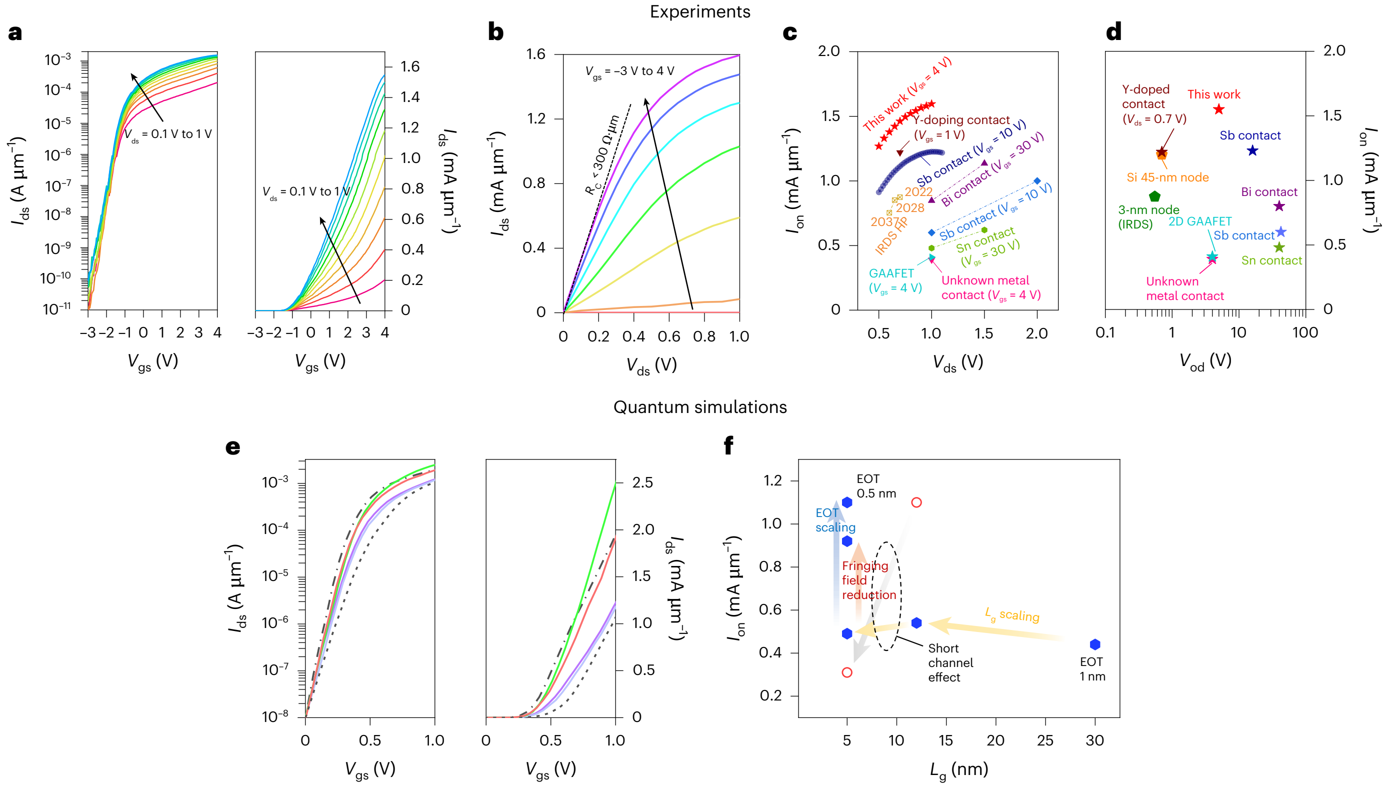

Fig. 4 | Performance benchmark and quantum-simulation-based scaling of the best device. a, Transfer curves (I_{ds}–V_{gs}) of the best bilayer MoS$_2$ dual-gate FET measured under V_{ds} varying from 0.1 V to 1 V with a step of 0.1 V, plotted in semilog scale (left) and linear scale (right). **b**, Output curves (I_{ds}–V_{ds}) of the same FET plotted in linear scale under V_{gs} varying from −3 V to 4 V with a step of 1 V. The observation of linear curves in the subsaturation regime for all curves suggests the formation of ohmic contacts. **c**, Benchmark plot comparing the outstanding I_{on} observed in our device with other studies as a function of V_{ds} (refs. 6,12,13,32–35). Despite being obtained at lower V_{ds} compared with results using other single crystals, our I_{on} is the highest. The yellow boxes represent the I_{on} and V_{ds} requirements for the International Roadmap for Devices and Systems High Performance Logic specifications in the years 2022, 2028 and 2037 (ref. 4). While direct comparison with advanced silicon transistors is not possible due to the broad operating voltage range of our device, it can be demonstrated that the 2D channel allows for sufficiently high current. **d**, Plot benchmarking the I_{on} of MoS$_2$ FETs from **c** based on overdrive voltage ($V_{od} = V_{gs} - V_{th}$) for fair comparison. Stars, MoS$_2$ FETs; pentagons, silicon FETs[41]. Notably, the actual I_{on} values of our best device are represented by red stars. **e**, Transfer curves (I_{ds}–V_{gs}), plotted in semilog scale (left) and linear scale (right), at I_{off} = 10 nA μm^{-1} with V_{ds} = 0.7 V, obtained after L_g and EOT scaling through NEGF simulations based on experimental data. The dot-dashed line and dashed line represent the transfer curves of a silicon GAAFET with L_g = 12 nm and 5 nm, respectively, obtained from quantum simulations, while all solid lines correspond to the transfer curves of MoS$_2$ devices. The purple and light blue lines represent the transfer curves after scaling L_g to 12 nm and 5 nm, respectively. The green line corresponds to further scaling of EOT to 0.5 nm at L_g = 5 nm, while the red line represents the transfer curve after removing the fringing field effect at L_g = 5 nm. **f**, Comparison of I_{on} as a function of L_g for MoS$_2$ and Si, plotted based on I_{off} = 10 nA μm^{-1}, with V_{dd} = 0.7 V, obtained through NEGF simulations. Blue hexagons, MoS$_2$ FETs; red circles, silicon FETs. MoS$_2$ exhibits less short-channel effect compared with silicon for L_g of <5 nm, preventing performance degradation. Through L_g scaling (yellow arrow), area gain can be achieved while maintaining performance. Furthermore, by eliminating the fringing field (red arrow) or scaling the EOT down to 0.5 nm (blue arrow), additional performance gains over silicon can be realized. Note that all data presented in **e**,**f** were obtained from simulations.

the exact 3D device geometry instead of the simplified silicon-based models used in earlier works[42]. The model was calibrated to the experimental transfer curves (Fig. 4a,b) by fitting the effective mass, dielectric constant and other material parameters obtained from density functional theory (DFT) calculations (Supplementary Figs. 16 and 17 and Extended Data Table 1). Ballisticity as a function of channel length was extracted (Supplementary Fig. 18) and incorporated together with scattering to predict the *I*–*V* characteristics of scaled devices (Extended Data Fig. 6). For comparison we also simulated a 4-nm-thick silicon single-channel GAAFET at L_g = 12 nm and 5 nm (Extended Data Fig. 7). Using an I_{off} = 10 nA μm^{-1} criterion, the MoS$_2$ dual-gate device lags silicon at L_g = 12 nm but surpasses it at L_g = 5 nm because silicon suffers severe short-channel effects (Fig. 4e,f). The dual-gate structure reduces the fringing-field barrier, but a residual field remains as long as metal contacts are used; eliminating the fringing field in the simulation yields an ~2-fold I_{on} increase. Because further reduction of the fringing field is impractical, the only viable route is to scale the EOT. With a high-*k* dielectric that can be deposited to EOT ≈ 0.5 nm (ref. 43), the series capacitance (centroid + quantum) becomes comparable to the oxide capacitance. In atomically thin 2D channels the centroid capacitance is negligible, while the quantum capacitance of MoS$_2$ (large effective mass and density of states) is high; consequently, sub-0.5-nm EOT gives MoS$_2$ I_{on} values comparable to those of silicon[19]. Finally, to be relevant for advanced nodes the CGP must be reduced. Although our device's CGP is relatively large, the L_{ch} is comparable, and both literature and short-gate MoS$_2$ FETs shown in Supplementary Fig. 19 confirm that even a 10-nm contact length in MoS$_2$ FETs provides robust contact performance[12,44]. Because GAAFETs suffer from a large capacitance penalty, a planar dual-gate MoS$_2$ device can achieve similar a.c. performance while benefiting from lower parasitic capacitance.

Outlook

The performance improvements observed in this work, although substantial, are not yet sufficient to justify a complete replacement of the existing silicon-based manufacturing infrastructure. The wafer-scale devices reported here were fabricated from polycrystalline MoS_2 to enable large-area synthesis, but the resulting high trap density limits mobility, uniformity and SS. Demonstrating single-crystalline growth of 2D materials would eliminate many of these traps, raise the carrier mobility and push I_{on} and SS toward the scaling targets for V_{dd} and I_{off} (ref. 11). Recent advances in confined-growth techniques are already delivering high-quality 2D layers on wafer scales and will be essential for this transition[9,10]. Besides, more fundamental bottleneck is the absence of controllable heavy doping for 2D channels. Without reliable doping, R_C remains high and precise V_{th} engineering is difficult. Parallel efforts on surface-charge transfer dopants, substitutional dopants and contact-region alloying are therefore required. Process reliability must also address stability and adhesion: bare 2D surfaces are chemically active, yet once encapsulated with high-*k* dielectrics and spacer layers they exhibit excellent thermal and long-term stability. The low adhesion energy to typical substrates can cause delamination during back-end-of-line (BEOL) processing; a promising mitigation strategy is to treat the 2D channel as a stress-free transferable layer, moving it between front-end-of-line (FEOL) and BEOL stacks instead of growing it directly on the wafer.

The present study has shown that the fringing field from elevated source/drain contacts forms a dominant barrier that limits charge injection in 2D transistors. By employing a balanced dual-gate architecture, this barrier is partially screened, leading to a pronounced boost in I_{on}. TCAD/NEGF simulations and extensive statistical measurements (hundreds of devices on a 200-mm wafer) confirm that the dual gate not only lowers the injection barrier but also increases the effective channel mobility through additional conduction pathways. Our best polycrystalline bilayer device achieved an outstanding d.c. I_{on} of 1.55 mA μm^{-1} with a modest mobility (~20 $cm^2 V^{-1} s^{-1}$). Quantum-transport scaling simulations, calibrated to the experimental data, reveal that while silicon GAAFETs lose performance for L_g <12 nm, the MoS_2 dual-gate device remains functional down to L_g = 5 nm. When the EOT is reduced to 0.5 nm, the series (centroid + quantum) capacitance of MoS_2 becomes comparable to the oxide capacitance, further closing the I_{on} gap with silicon. Moreover, the planar dual-gate layout avoids the 3D gate formation required for silicon GAAFETs, resulting in lower parasitic capacitance and superior power–performance–area–cost metrics. Fabricating a true GAA device from 2D materials is extremely complex[45]; the simpler dual-gate approach therefore offers a more realistic pathway toward integration. Finally, the atomically thin nature of MoS_2 enables M3D integration, where multiple 2D stacks can be assembled with minimal pitch penalties, delivering additional area and performance gains.

In summary, the dual-gate bilayer MoS_2 platform demonstrates that a modest, planar architecture can meet the electrostatic control and current requirements of sub-5-nm logic nodes. Realizing its full potential will require (1) wafer-scale single-crystal growth, (2) reliable heavy-doping or contact-doping schemes, (3) robust encapsulation and adhesion strategies and (4) stress-free transfer processes compatible with BEOL integration. With these advances, MoS_2-based transistors could become a practical complement—or eventual alternative—to silicon in advanced technology nodes.

Online content

Any methods, additional references, Nature Portfolio reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41563-025-02452-y.

References

1. Cao, W. et al. The future transistors. *Nature* **620**, 501–515 (2023).
2. Ferain, I., Colinge, C. A. & Colinge, J.-P. Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors. *Nature* **479**, 310–316 (2011).
3. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
4. *International Roadmap for Devices and Systems* https://irds.ieee.org/editions/2022 (IEEE, 2022).
5. Jeong, J. et al. World's first GAA 3nm foundry platform technology (SF3) with novel multi-bridge-channel-FET (MBCFET^{TM}) process. In *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* 1–2 (IEEE, 2023); https://doi.org/10.23919/VLSITechnologyandCir57934.2023.10185353
6. Chou, B.-J. et al. High-performance monolayer MoS_2 nanosheet GAA transistor. *Nanotechnology* **35**, 125204 (2024).
7. O'Brien, K. P. et al. Advancing 2D monolayer CMOS through contact, channel and interface engineering. In *2021 IEEE International Electron Devices Meeting (IEDM)* 7.1.1–7.1.4 (IEEE, 2021); https://doi.org/10.1109/IEDM19574.2021.9720651
8. O'Brien, K. P. et al. Process integration and future outlook of 2D transistors. *Nat. Commun.* **14**, 6400 (2023).
9. Kim, K. S. et al. Non-epitaxial single-crystal 2D material growth by geometric confinement. *Nature* **614**, 88–94 (2023).
10. Kim, K. S. et al. Growth-based monolithic 3D integration of single-crystal 2D semiconductors. *Nature* **636**, 615–621 (2024).
11. Moon, D. et al. Hypotaxy of wafer-scale single-crystal transition metal dichalcogenides. *Nature* https://doi.org/10.1038/s41586-024-08492-9 (2025).
12. Shen, P.-C. et al. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).
13. Li, W. et al. Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).
14. Ko, J.-S. et al. Ultrathin gate dielectric enabled by nanofog aluminum oxide on monolayer MoS_2. In *ESSDERC 2023—IEEE 53rd European Solid-State Device Research Conference (ESSDERC)* 1–4 (IEEE, 2023) https://doi.org/10.1109/ESSDERC59256.2023.10268527
15. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **6**, 147–150 (2011).
16. Ugeda, M. M. et al. Giant bandgap renormalization and excitonic effects in a monolayer transition metal dichalcogenide semiconductor. *Nat. Mater.* **13**, 1091–1095 (2014).
17. Kwon, J. et al. Thickness-dependent Schottky barrier height of MoS_2 field-effect transistors. *Nanoscale* **9**, 6151–6157 (2017).
18. Zhang, S. et al. Wafer-scale transferred multilayer MoS_2 for high performance field effect transistors. *Nanotechnology* **30**, 174002 (2019).
19. Bennett, R. K. A. & Pop, E. How do quantum effects influence the capacitance and carrier density of monolayer MoS_2 transistors? *Nano Lett.* **23**, 1666–1672 (2023).
20. Kim, K. S. et al. The future of two-dimensional semiconductors beyond Moore's law. *Nat. Nanotechnol.* **19**, 895–906 (2024).
21. Kita, Y. et al. Systematic study on work-function-shift in metal/Hf-based high-*k* gate stacks. *Appl. Phys. Lett.* **94**, 122905 (2009).
22. Guo, Y. et al. Field-effect at electrical contacts to two-dimensional materials. *Nano Res.* **14**, 4894–4900 (2021).
23. Lv, J., Shen, Z., Meng, D., Peng, L.-M. & Qiu, C. High-performance dual-gate transistors based on aligned carbon nanotubes. *ACS Appl. Mater. Interfaces* **16**, 58864–58871 (2024).
24. Illarionov, Y. Y. et al. Insulators for 2D nanoelectronics: the gap to bridge. *Nat. Commun.* **11**, 3385 (2020).
25. Pasadas, F. et al. Large-signal model of 2DFETs: compact modeling of terminal charges and intrinsic capacitances. *npj 2D Mater. Appl.* **3**, 47 (2019).
26. Fan, D. et al. Two-dimensional semiconductor integrated circuits operating at gigahertz frequencies. *Nat. Electron.* **6**, 879–887 (2023).

27. Silvestri, L. et al. Hierarchical modeling for TCAD simulation of short-channel 2D material-based FETs. *Solid State Electron.* **200**, 108533 (2023).
28. Liu, L. et al. Uniform nucleation and epitaxy of bilayer molybdenum disulfide on sapphire. *Nature* **605**, 69–75 (2022).
29. Hwangbo, S., Hu, L., Hoang, A. T., Choi, J. Y. & Ahn, J.-H. Wafer-scale monolithic integration of full-colour micro-LED display using MoS_2 transistor. *Nat. Nanotechnol.* **17**, 500–506 (2022).
30. Li, H. et al. From bulk to monolayer MoS_2: evolution of Raman scattering. *Adv. Funct. Mater.* **22**, 1385–1390 (2012).
31. Ma, N. & Jena, D. Carrier statistics and quantum capacitance effects on mobility extraction in two-dimensional crystal semiconductor field-effect transistors. *2D Mater.* **2**, 015003 (2015).
32. Jiang, J. et al. Yttrium-doping-induced metallization of molybdenum disulfide for ohmic contacts in two-dimensional transistors. *Nat. Electron.* https://doi.org/10.1038/s41928-024-01176-2 (2024).
33. Chou, A.-S. et al. High on-current 2D nFET of 390 μA/μm at VDS = 1 V using monolayer CVD MoS_2 without intentional doping. In *2020 IEEE Symposium on VLSI Technology* 1–2 (IEEE, 2020); https://doi.org/10.1109/VLSITechnology18217.2020.9265040
34. Chou, A.-S. et al. Antimony semimetal contact with enhanced thermal stability for high performance 2D electronics. In *2021 IEEE International Electron Devices Meeting (IEDM)* 7.2.1–7.2.4 (IEEE, 2021); https://doi.org/10.1109/IEDM19574.2021.9720608
35. Chou, A.-S. et al. High on-state current in chemical vapor deposited monolayer MoS_2 nFETs with Sn ohmic contacts. *IEEE Electron Device Lett.* **42**, 272–275 (2021).
36. Li, L. et al. Epitaxy of wafer-scale single-crystal MoS_2 monolayer via buffer layer control. *Nat. Commun.* **15**, 1825 (2024).
37. Xiong, X. et al. Demonstration of vertically-stacked CVD monolayer channels: MoS_2 nanosheets GAA-FET with $I_{on} > 700$ μA/μm and MoS_2/WSe_2 CFET. In *2021 IEEE International Electron Devices Meeting (IEDM)* 7.5.1–7.5.4 (IEEE, 2021); https://doi.org/10.1109/IEDM19574.2021.9720533
38. Zou, T. et al. High-performance solution-processed 2D p-type WSe_2 transistors and circuits through molecular doping. *Adv. Mater.* **35**, 2208934 (2023).
39. Li, N. et al. Large-scale flexible and transparent electronics based on monolayer molybdenum disulfide field-effect transistors. *Nat. Electron.* **3**, 711–717 (2020).
40. Cheng, K.-L. et al. A highly scaled, high performance 45 nm bulk logic CMOS technology with 0.242 μm^2 SRAM cell. In *2007 IEEE International Electron Devices Meeting* 243–246 (IEEE, 2007); https://doi.org/10.1109/IEDM.2007.4418913
41. Mistry, K. et al. A 45 nm logic technology with high-*k* + metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging. In *2007 IEEE International Electron Devices Meeting* 247–250 (IEEE, 2007); https://doi.org/10.1109/IEDM.2007.4418914
42. Pal, A., Chavan, T., Jabbour, J., Cao, W. & Banerjee, K. Three-dimensional transistors with two-dimensional semiconductors for future CMOS scaling. *Nat. Electron.* **7**, 1147–1157 (2024).
43. Tang, J. et al. Low-power 2D gate-all-around logics via epitaxial monolithic 3D integration. *Nat. Mater.* https://doi.org/10.1038/s41563-025-02117-w (2025).
44. English, C. D., Shine, G., Dorgan, V. E., Saraswat, K. C. & Pop, E. Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).
45. Kim, C. et al. Transfer free 2D CMOS multi bridge channel FET. In *2024 IEEE International Electron Devices Meeting (IEDM)* 1–4 (IEEE, 2024); https://doi.org/10.1109/IEDM50854.2024.10873503

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[1]Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd, Suwon, Republic of Korea. [2]Computational Science Engineering Team, Semiconductor R&D Center, Samsung Electronics Co., Ltd, Giheung, Republic of Korea. [3]School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA. [4]Department of Electrical and Computer Engineering, University of Southern California, Los Angeles, CA, USA. [5]Department of Mechanical Engineering, and Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, MA, USA. [6]These authors contributed equally: Junyoung Kwon, Kyoung Yeon Kim, Dongwon Jang. ✉e-mail: k77y.kim@samsung.com; limsung@usc.edu; ke14.byun@samsung.com; minsu.seol@samsung.com; jeehwan@mit.edu

Methods

TCAD simulations

Classical simulations. We use the multi-subband Boltzmann transport equation (MSBTE) solver, implemented in our in-house simulator. It calculates the Schrödinger equation perpendicular to the transport direction and the one-dimensional MSBTE for each subband. Mode decomposition is used to reduce the computational burden at the realistic device scale, and a periodic boundary condition is applied for the width direction. Layer-dependence effective mass and bandgap are considered as in Extended Data Table 1, and a multilayer model considering the vdW gap is used to accurately reflect the electrostatic effects depending on the device structure. DFT results show that the MoS_2 layer has a high dielectric constant, while the vdW layer has a low dielectric constant[46,47]. This causes most of the potential drop to occur in the vdW layer, resulting in a considerable difference in the electrical operation of monolayer and multilayer devices. The MSBTE solver is a semiclassical transport equation that cannot originally consider tunnelling effects. However, the tunnelling current is accurately included as a non-local intravalley interaction based on the Wentzel–Kramers–Brillouin tunnelling model[48]. This allows for the accurate consideration of the source-induced injection barrier. In bilayer modelling, another challenge is calculating the current path correctly. In a few-layer top-contact device, the main current path is the top layer because carriers with a small electric field are rarely injected from the source to the bottom layer. However, the MSBTE solver considers the 1D transport equation and imposes the injection boundary condition on the sides, leading to the misleading conclusion that most of the current path is formed in the bottom layer, which is less susceptible to the source fringe field effect. To mimic the low current injection to the bottom layer by tunnelling through the vdW layer, a thin tunnelling layer is added to the bottom layer as in Supplementary Fig. 2. Through these detailed modelling efforts, the origin of the substantial gain of I_{on} and decrease of the R_C when using dual-gate in a bilayer device is clearly identified.

Quantum simulations. Quantum simulation was performed on realistic short-channel devices ($L_g \approx 5$–30 nm) to capture the experimentally observed electrostatic structure, including fringing fields. We utilized an in-house simulator (Polaris Quantum) which is based on the NEGF method[49,50], utilizing 5,760 CPU cores, to overcome the computational demand for simulating realistic device geometry. Here, the retarded Green's function is computed to obtain the electron and current density:

$$G(E) = [EI - H - \Sigma]^{-1}$$

where G is the retarded Green's function, E is the electron energy, I is the identity matrix and Σ is the retarded self-energy that accounts for the coupling to contacts and electron–phonon interactions. For the Hamiltonian H, we incorporated the effective mass approximation (EMA) for non-parabolicity corrections. The effective mass and non-parabolic factor of MoS_2 were further refined by DFT (Supplementary Fig. 17), yielding values consistent with recent literature[42]. Inter- and intra-valley scattering were introduced via the self-consistent Born approximation (SCBA) and calibrated to reproduce the measured channel resistance, allowing realistic ballistic-to-diffusive ratios without resorting to a simple 'ballistic-current × ballistic-ratio' scaling as described in Supplementary Fig. 18. As shown in Extended Data Figs. 6 and 7, MoS_2 was modelled with a top-metal direct contact, whereas silicon used a silicide contact[51]; source/drain metals were represented as virtual conductive regions at fixed electrostatic potential, enabling flexible contact shapes and complex boundary conditions. Real-space NEGF was used to resolve intricate current paths, and matrix blocks were decomposed with the recursive Green's function algorithm to maximize parallel efficiency. The bilayer MoS_2 stack was treated as two distinct layers separated by a vdW gap, each assigned its own dielectric constant obtained from first-principles orbital-separation calculations[52,53] (Supplementary Fig. 17). This layered electrostatic model reproduces the fringing-field-induced increase in injection barrier and the concomitant reduction in ballistic current (Supplementary Fig. 20). The simulation was slightly underfitted to experimental data to avoid overestimating the scaled-device performance. For silicon devices, realistic silicide contacts and constriction geometries were included, capturing quantum access-resistance effects omitted in conventional NEGF models that consider only the channel; consequently, simulated I_{on} match experimental values without the overestimation typical of simplified structures[50]. The self-consistent NEGF + SCBA framework, calibrated against experimental resistance and fringing-field effects, thus provides a quantitative description of both MoS_2 and silicon short-channel devices while avoiding the pitfalls of empirical ballistic-ratio scaling.

MOCVD of monolayer and bilayer MoS_2. The growth of 200-mm-scale monolayer MoS_2 was conducted under the same conditions as in our previous studies[54–56]. We used a showerhead-type cold-wall MOCVD reactor for the growth of MoS_2, utilizing $Mo(CO)_6$ as the molybdenum precursor and $(C_2H_5)_2S_2$ as the sulfur precursor. The flow rates of the precursors were 0.001 sccm for $Mo(CO)_6$, 0.007 sccm for $(C_2H_5)_2S_2$ and 100 sccm for H_2, all of which were precisely regulated by individual mass-flow controllers and electronic pressure controllers. The chamber pressure and wafer temperature were maintained at 5.0 torr and 600 °C, respectively, during the growth process. We used KI as an additive to improve adatom diffusion, placing it upstream in the reactor. Growth time was controlled from 12 min to 2 h to control the layer number.

Fabrication of 200-mm-wafer-scale FETs. First, we started device fabrication with a 200-mm silicon wafer and created a 100-nm SiO_2 layer through thermal oxidation. Next, we pattern the bottom-gate electrode using photolithography with an i-line stepper. At this stage, the negative process using the image reversal photoresist AZ5214 is utilized, followed by a lift-off process. For the bottom-gate metal, 5 nm of titanium and 20 nm of gold are used. The creation of the bottom-gate structure is completed by depositing 10 nm of HfO_x by atomic layer deposition. Next, a MoS_2 film grown by MOCVD is transferred onto the substrate. As in our previous study[55], a semiautomatic transfer stage is utilized at this stage. After that, another photolithography process is carried out to pattern the active channel area of MoS_2. The exposed areas of MoS_2 are etched using O_2 reactive ion etching or a plasma asher. Next, we patterned fine source/drain electrodes for the short-channel device using electron-beam lithography. In this case, a 495,000 M_w PMMA A2/950,000 M_w PMMA A2 (PMMA, poly(methyl methacrylate)) bilayer is utilized as an electron-beam resist for smooth lift-off. In this case, 20-nm gold is used as the contact metal. Another round of photolithography, metal deposition and lift-off are carried out to create metal leads connecting the pads for subsequent measurements. It is important to perform electron-beam lithography first in this process, as photoresist residue can notably degrade the R_C of the resulting FETs. To facilitate the deposition of dielectric on top of the MoS_2 for the fabrication of the top-gate stack, an interlayer is deposited using a method known as the 'nanofog' technique[14,57]. Top-gate dielectric, 10-nm HfO_x, is deposited by atomic layer deposition. Then, similar to the bottom-gate process, patterning is carried out to form the top-gate metal, completing the device fabrication. See Supplementary Fig. 9 for a visualization of the fabrication processes.

Data availability

Source data are provided with this paper. Any additional data supporting the conclusions of this work can be obtained from the corresponding authors upon request.

Code availability

The Python code (v.3.8.5) used for the statistical analysis of FETs in this study is available from the corresponding authors upon request.

References

46. Mirabelli, G., Hurley, P. K. & Duffy, R. Physics-based modelling of MoS_2: the layered structure concept. *Semicond. Sci. Technol.* **34**, 055015 (2019).
47. Donetti, L. et al. Towards a DFT-based layered model for TCAD simulations of MoS_2. *Solid State Electron.* **197**, 108437 (2022).
48. Stanojević, Z. et al. Nano device simulator—a practical subband-BTE solver for path-finding and DTCO. *IEEE Trans. Electron. Devices* **68**, 5400–5406 (2021).
49. Park, H.-H. et al. Toward more realistic NEGF simulations of vertically stacked multiple SiNW FETs. In *2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)* 206–209 (IEEE, 2018); https://doi.org/10.1109/SISPAD.2018.8551692
50. Kim, K. Y. et al. Quantum transport through a constriction in nanosheet gate-all-around transistors. *Commun. Eng.* **4**, 92 (2025).
51. J. Park *et al*. First demonstration of 3-dimensional stacked FET with top/bottom source-drain isolation and stacked n/p metal gate. In *2023 International Electron Devices Meeting (IEDM)* 1–4 (IEEE, 2023); https://doi.org/10.1109/IEDM45741.2023.10413694
52. Kasamatsu, S., Watanabe, S. & Han, S. Orbital-separation approach for consideration of finite electric bias within density-functional total-energy formalism. *Phys. Rev. B* **84**, 085120 (2011).
53. Kasamatsu, S., Watanabe, S. & Han, S. First-principles calculation of charged capacitors under open-circuit conditions using the orbital-separation approach. *Phys. Rev. B* **92**, 115124 (2015).
54. Seol, M. et al. High-throughput growth of wafer-scale monolayer transition metal dichalcogenide via vertical Ostwald ripening. *Adv. Mater.* **32**, 2003542 (2020).
55. Kwon, J. et al. 200-mm-wafer-scale integration of polycrystalline molybdenum disulfide transistors. *Nat. Electron.* https://doi.org/10.1038/s41928-024-01158-4 (2024).
56. Nguyen, V. L. et al. Wafer-scale integration of transition metal dichalcogenide field-effect transistors using adhesion lithography. *Nat. Electron.* **6**, 146–153 (2023).
57. Kwak, I. et al. Low interface trap density in scaled bilayer gate oxides on 2D materials via nanofog low temperature atomic layer deposition. *Appl. Surf. Sci.* **463**, 758–766 (2019).
58. *International Technology Roadmap for Semiconductors (ITRS) 2007 Edition*. https://www.semiconductors.org/resources/2007-international-technology-roadmap-for-semiconductors-itrs/, (Semiconductor Industry Association, 2007).

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Author contributions

J. Kwon, K.Y.K., D.J., K.-E.B., M.S. and J. Kim conceived the project and defined the research strategy. J. Kwon designed, fabricated and measured all wafer-scale devices, performed the data analysis and drafted the paper. K.Y.K. carried out all TCAD/NEGF simulations, developed the device-level models, supervised the simulation work and contributed to paper preparation. D.J. interpreted the simulation results, helped shape the logical flow of the paper and participated in writing. M.S.Y. and A.J. were responsible for the wafer-scale growth of monolayer and bilayer MoS_2 films by MOCVD. D.-S.K. performed TEM imaging and analysis. Y.H. performed quantum-capacitance simulations. H.R. participated in the fabrication of low-*k* spacer devices. W.I.C. carried out DFT-based calculations of the MoS_2 electronic structure. Y.C. led the discussion on MoS_2 transport mechanisms. C.K. contributed to the discussion of the experimental results. E.Y. acquired the SEM images and assisted with structural characterization. E.K.L. analysed the electrical-measurement data and led the discussion of these results. C-S.L. and S.W.K. provided the overall direction of the research, gave technical guidance and reviewed the paper. U.K. and D.S.K. discussed the simulation strategy, guided its development and supervised K.Y.K. S.K.L. supervised D.J. and led the discussion on future logic technologies. K.-E.B., M.S. and J. Kim supervised J. Kwon, contributed to the interpretation of the results and co-wrote the paper. All authors discussed the results, contributed to the interpretation of the data and approved the final version of the paper.

Competing interests

The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to Kyoung Yeon Kim, Sung Kyu Lim, Kyung-Eun Byun, Minsu Seol or Jeehwan Kim.

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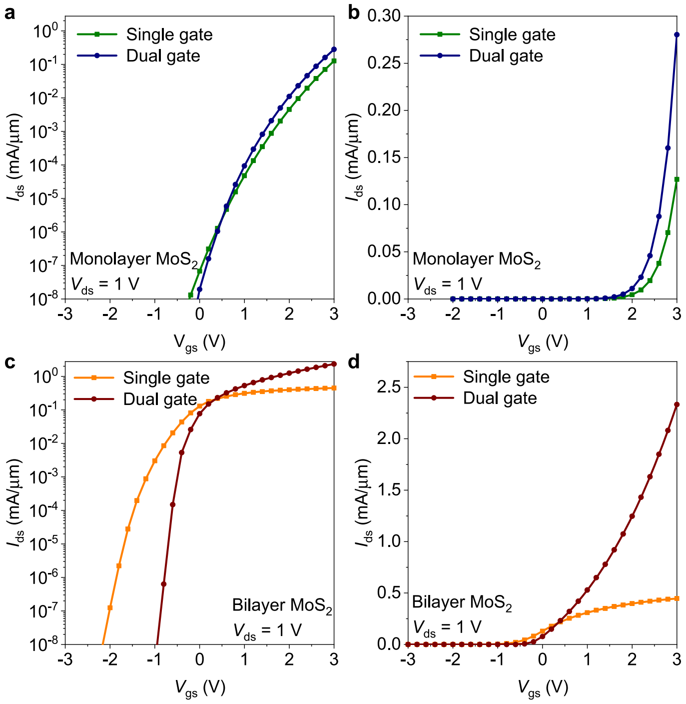
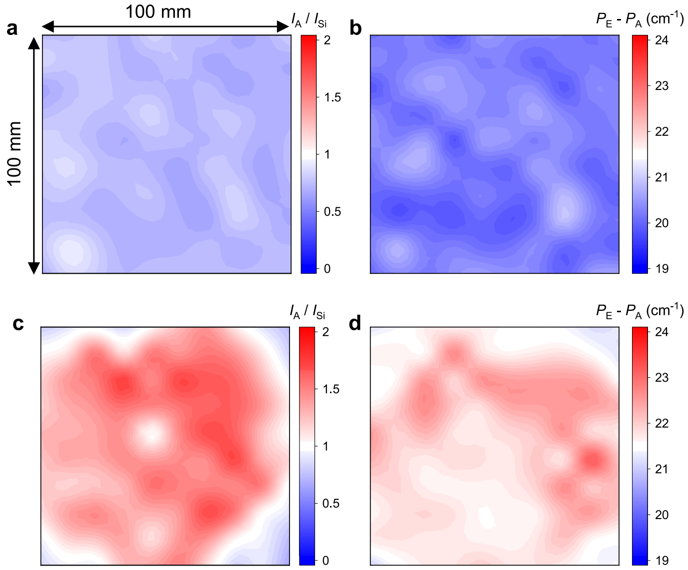


Extended Data Fig. 1 | Transfer curves (I_{ds} – V_{gs}) simulated using TCAD. a,b, Transfer curves of single gate (green) and dual gate (navy) monolayer MoS_2 FETs plotted on both semi-log (**a**) and linear (**b**) scales. **c,d**, Transfer curves of single gate (orange) and dual gate (wine) bilayer MoS_2 FETs plotted on both semi-log (**c**) and linear (**d**) scales.



Extended Data Fig. 2 | Raman map images of large area MoS_2 films. **a**, Image mapping the ratio of A peak intensity (I_A) of monolayer MoS_2 to Si peak intensity (I_{Si}). **b**, Image mapping the distance between the E peak position (P_E) and A peak position (P_A) of monolayer MoS_2. **c**, Image mapping the ratio of I_A of bilayer MoS_2 to I_{Si}. **d**, Image mapping the distance between the P_E and P_A of bilayer MoS_2. Only the 100 mm×100 mm region is mapped, as the device fabrication area was confined to the 100 mm centre region of the wafer.

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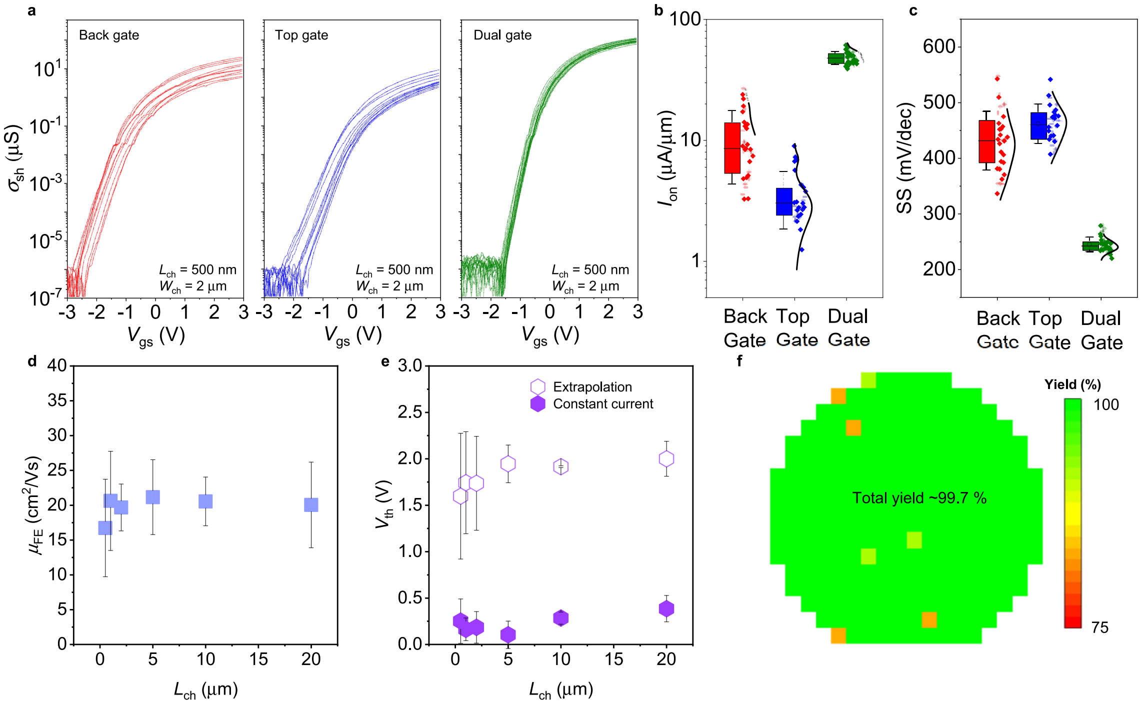
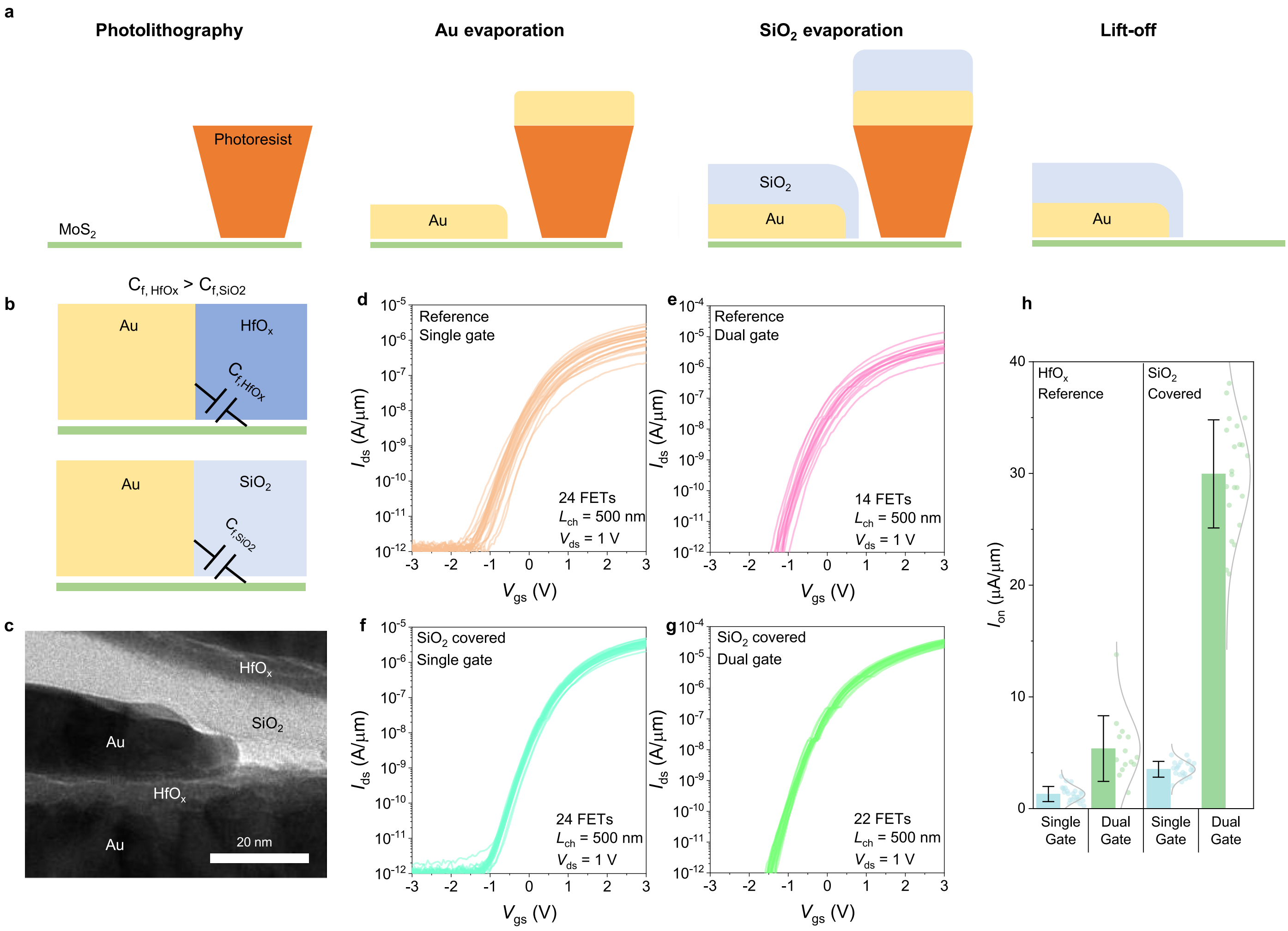
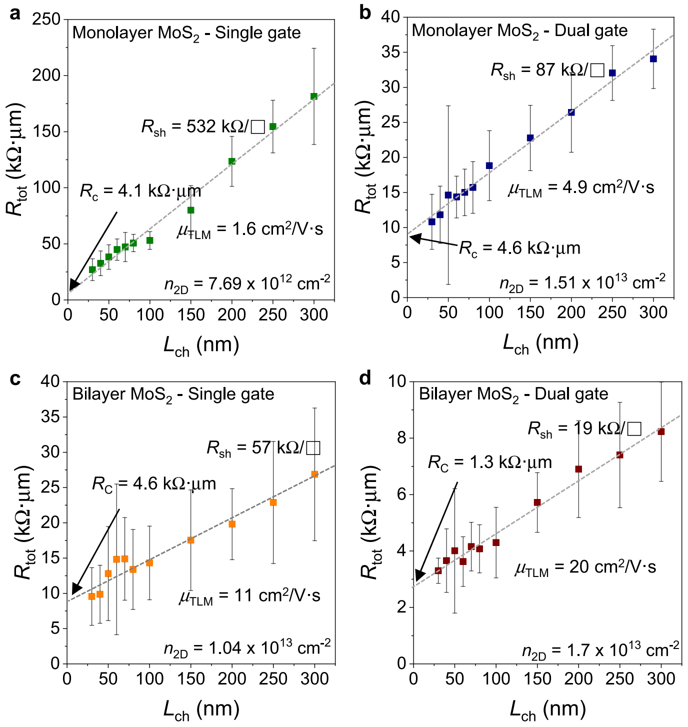


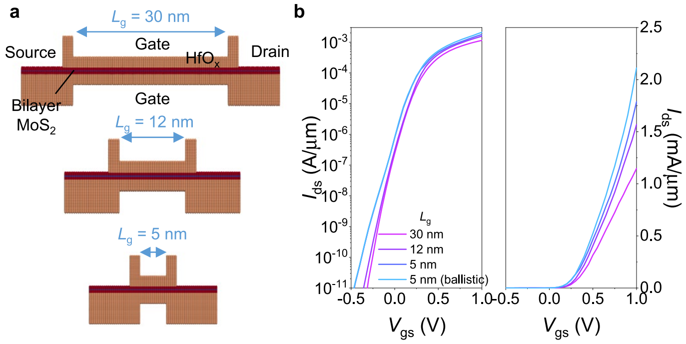
Extended Data Fig. 3 | Evaluation of 200-mm-wafer-scale long channel (L_{ch} > 500 nm) FETs based on bilayer MoS_2. **a**, Transfer curves ($\sigma_{sh} - V_{gs}$) of back gate (red), top gate (blue), and dual gate (green) MoS_2 FETs fabricated across the entire 200-mm wafer. **b**,**c**, Statistical distribution of I_{on} and subthreshold swing (SS) for back gate (red), top gate (blue), and dual gate (green) configurations. In dual gate configurations, not only I_{on} and SS have substantially improved, but the variance has also been greatly reduced. Here, the numbers of measured back-gate, top-gate, and dual-gate FETs are 40, 42, and 48, respectively. The box represents the 25 %–75 % range, the line in the middle indicates the median, and the circle denotes the mean value. **d**, Statistical analysis of field-effect (FE) mobility of dual-gate FETs as a function of L_{ch}. The consistent FE mobility values across different L_{ch} values indicate that the R_C has sufficiently decreased. **e**, Threshold voltage (V_{th}) of dual-gate FETs extracted using the linear extrapolation method (hollow hexagon) from the transfer curve and the V_{th} extracted using the constant current method (filled hexagon). The constant current value used was 50 nA. The number of devices for d and e by L_{ch} are: 115 devices for 500 nm, 60 for 1 μm, 34 for 2 μm, 35 for 5 μm, 36 for 10 μm, and 35 for 20 μm. Data in d, e are presented as mean values +/- standard deviation. **f.** A wafer map showing die-by-die device yield for the dual gate structure, demonstrating a high yield of 99.7%.



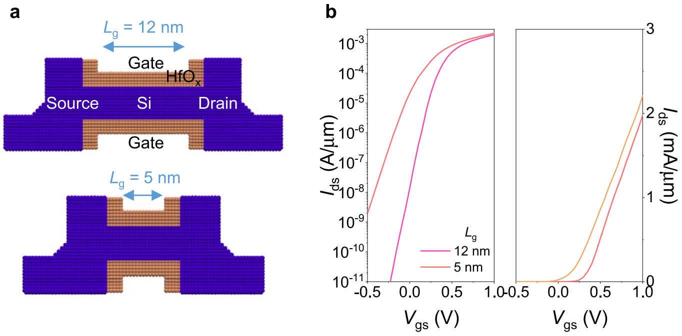
Extended Data Fig. 4 | SiO_2 spacer-based low-fringing-field FETs. a, Schematics showing SiO_2 spacer fabrication process. Source drain electrodes were fabricated by patterning a photoresist with a large undercut, followed by Au evaporation, subsequent SiO_2 evaporation, and a single lift off step, resulting in a SiO_2 spacer that covers the Au contacts. **b**, Comparison of the structure near the original contact (top) and the modified structure with an SiO_2 spacer (bottom). Because the dielectric constant of SiO_2 is lower than that of HfO_x, the fringing capacitance associated with the SiO_2 spacer ($C_{f,SiO2}$) is smaller than the fringing capacitance that arises from the HfO_x filled field ($C_{f,HfOx}$). **c**, Cross sectional TEM image of a fabricated MoS_2 FET that incorporates the SiO_2 spacer. **d,e**, Transfer curves of the reference structure without a spacer: back gate configuration (**d**) and dual gate configuration (**e**). **f,g**, Transfer curves of the FETs with a SiO_2 spacer: back gate configuration (**f**) and dual gate configuration (**g**). Insertion of the spacer reduces the fringing field, resulting in higher current and improved variation. **h**, Comparison of Ion at V_{gs} = 3 V extracted from the preceding transfer curves. After SiO_2 spacer insertion, both the back-gate and dual-gate configurations exhibit a pronounced increase in I_{on}. All data in this figure are presented as mean values +/- standard deviation.



Extended Data Fig. 5 | Transfer length method (TLM) of MoS$_2$ FETs. a, Total resistance (R_{tot}) as a function of channel length (L_{ch}) for single gate and monolayer MoS$_2$ FET at a planar carrier density (n_{2D}) of 7.69 ×10^{12} cm^{-2}. The number of devices for each L_{ch} is as follows: 10 devices for 30 nm, 52 for 40 nm, 67 for 50 nm, 16 each for 60, 70, 80, 150, 200, 250, and 300 nm, and 15 for 100 nm. **b**, Same plot for dual gate and monolayer MoS$_2$ FET at n_{2D} of 1.51 ×10^{13} cm^{-2}. 13 devices for 30 nm, 69 for 40 nm, 85 for 50 nm, and 18 each for 60, 70, 80, 100, 150, 200, 250, and 300 nm. **c**, Same plot for single gate and bilayer MoS$_2$ FET at n_{2D} of 1.04 ×10^{13} cm^{-2}. 5 devices for 30 nm, 32 for 40 nm, 55 for 50 nm, 14 for 60 nm, 15 for 70 nm, 14 for 80 nm, 14 for 100 nm, 16 for 150 nm, 16 for 200 nm, 16 for 250 nm, and 17 for 300 nm. **d**, Same plot for dual gate and bilayer MoS$_2$ FET at n_{2D} of 1.7 ×10^{13} cm^{-2}. 13 devices for 30 nm, 57 for 40 nm, 78 for 50 nm, 16 for 60 nm, 15 for 70 nm, 16 for 80 nm, 17 for 100 nm, 17 for 150 nm, 17 for 200 nm, 18 for 250 nm, and 17 for 300 nm. All data in this figure are presented as mean values +/- standard deviation.



Extended Data Fig. 6 | Variation in transfer curves of dual-gate MoS_2 FETs with L_g shrinkage. a, NEGF simulation models of bilayer MoS_2 dual-gate FETs with L_g = 30 nm, 12 nm, and 5 nm, from top to bottom. The bilayer MoS_2 was modelled with a vdW gap between the two MoS_2 layers. **b**, Transfer curves at V_{ds} = 0.7 V for L_g = 30 nm (pink), 12 nm (purple), and 5 nm (navy blue) calculated by quantum simulation. As L_g decreases to 5 nm, the transfer curve (navy blue) becomes increasingly similar to the ballistic transport-assumed transfer curve (light blue), indicating a higher proportion of ballistic transport under shorter L_g.



Extended Data Fig. 7 | Variation in transfer curves of Si FETs with L_g shrinkage. **a**, NEGF simulation models of Si GAAFETs with L_g = 12 nm and 5 nm, from top to bottom. The thickness of the Si channel is fixed to 4 nm. **b**, Transfer curves at V_{ds} = 0.7 V for 12 nm (pink), and 5 nm (orange) calculated by quantum simulation. Unlike MoS_2, Si exhibits a notable degradation in SS due to the short-channel effect as L_g is reduced to 5 nm.

Extended Data Table 1 | Parameters used in TCAD simulation

	Classical		**Quantum**	
Channel	Monolayer MoS_2	Bilayer MoS_2	Bilayer MoS_2	Silicon
Channel dielectric constant	23		15	11.7
vdW gap dielectric constant	2		4.4	-
Channel thickness (A)	8 for each layer		10	50
vdW gap thickness (A)	2		2	-
HfO_x dielectric constant	25		12	12
Effective mass (longitudinal)	0.342	0.386	0.648	0.98
Effective mass (transverse)	0.350	0.390	0.655	0.19
Doping concentration (cm^{-2} or cm^{-3})	8×10^{12} cm^{-2}	1.6×10^{13} cm^{-2}		1×10^{15} cm^{-3} for channel 3×10^{20} cm^{-3} for S/D
Band gap (eV)	1.6	1.2		1.12

The quantum simulation aimed to closely reflect the actual measured values for better fitting with experimental results, leading to differences in parameters compared to the classical simulation.

Extended Data Table 2 | Comparison of figure of merits between MoS_2 transistors and Si transistors[4,40,41,58]

Reference	This work Experiment	This work Simulation	This work Simulation	This work Simulation	This work Simulation	Ref. 40	Ref. 41	ITRS 2007	IRDS 2022	IRDS 2022
Channel	MoS_2				Si					
Technical node	Experiment	Simulation	Simulation	Simulation	Simulation	45 nm	45 nm	45 nm	3 nm	0.5 nm
Platform	Planar-DG	Planar-DG	Planar-DG	Planar-DG	GAAFET	Planar-SG	Planar-SG	Planar-SG	FinFET	GAAFET
L_g (nm)	40	12	5	5	12	35	35	25	16	12
μ_{eff} (cm^2/Vs)	20	13	5	5	14	-	-	-	125	40
SS (mV/dec)	290	88	98	85	71	90	-	90	82	70
I_{off} (µA/µm)	244	0.01	0.01	0.01	0.01	0.1	0.1	0.34	0.01	0.01
I_{on} (mA/µm)	1.55	0.538	0.487	1.09	1.09	1.36	1.2	1.211	0.874	0.753
V_{th} (V)	-1.4	-	-	-	-	0.15*	0.15*	0.134	0.156	0.154
V_{dd} (V)	1 (V_{ds})	0.7	0.7	0.7	0.7	1	1	1.1	0.7	0.6
V_{od} (V)	5.4	-	-	-	-	0.85*	0.85*	0.966	0.544	0.446
EOT or CET (nm)	3.3	1	1	0.5	1	1	1	1.1	1	0.9
R_{sd} (ohm·µm)	< 300	-	-	-	-	-	190	200	271	210

*The values marked with an asterisk are estimated based on other data from the manuscript and are not precise measurements.