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Methodology to determine the impact of linewidth variation on chip scale copper/low-*k* backend dielectric breakdown

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ABSTRACT

Low-*k* time-dependent dielectric breakdown (TDDB) has been found to be a function of metal linewidth, when the distance between the lines is constant. Modeling requires determining the relationship between TDDB and layout geometries. To determine this relationship, comb test structures have been design and implemented in 45 nm technology. In this work, low-*k* dielectric breakdown, low-*k* dielectric vulnerable areas, and linewidth variation are linked to full chip lifetimes.

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1. Introduction

Low-*k* time-dependent dielectric breakdown is an important reliability issue during Cu/low-*k* technology development and its qualification. With increasing porosity Cu/low-*k* interconnect systems are more vulnerable to breakdown, and reduced supply voltage scaling with respect to feature size had led to exponentially increasing electric fields among interconnects every technology generation, aggravating low-*k* dielectric breakdown.

Low-*k* dielectric breakdown is typically measured with comb test structures. The stress on the dielectric is created by applying a voltage difference to the comb, which creates lateral stress across the dielectric between the fingers of the comb, separated by the line space, *S*. A cross-section of the dielectric under stress is shown in Fig. 1. In our examples, we applied a voltage of 14 V and the current between the lines was monitored, with a current limit of 100 μA to detect dielectric breakdown.

The two dominant models of dielectric lifetime, the *E* model [1] and the $\sqrt{E}$ model [2–4], relate time-to-failure to electric field. In both models, besides temperature, the only factor that determines the time-to-failure is the electric field (*E*). Electric field in backend structures is a function of the distance between the interconnect lines, termed line space *S*, i.e. $E = V/S$ where *V* is the applied voltage.

In prior work, with 180 nm technology, experimental data indicated that time-to-breakdown was a function of linewidth [5,6]. In [5], variation is explained to be due to field enhancement, in combination with contamination and charging during processing, that more strongly impacts the narrow lines. We have performed finite element analysis on our structures and found no significant field enhancement [7]. However, analysis found that the difference in time-to-breakdown was due to a physical difference in the line space. The explanation that best matched the data was microloading in etch. The microloading effect was due to a sensitivity of etch rate to pattern density [8,9]. However, the test structures used to analyze the impact of metal linewidth confounded the impact of linewidth with pattern density, as can be seen in Fig. 2. Fig. 2 shows that whenever linewidth is increased, while keeping the line space constant, the pattern density also increases.

Hence, although the theory associates the time-to-breakdown difference with pattern density, it could not be conclusively verified that pattern density, rather than linewidth, produced the time-to-breakdown difference. This paper aims to distinguish between these two factors and to use the results to estimate full chip lifetimes.

This paper is organized as follows. Section 2 presents the test structures to measure the impact of linewidth and density on lifetimes, together with the analysis of the data. The modeling of characteristic lifetime is discussed in Section 3. In Section 4, we use models based on the data from the three uniform linewidth test structures to predict the lifetime of a 4th test structure with non-uniform linewidths. Section 5 provides the theory and examples of full chip analysis, and Section 6 concludes the paper.

2. Linewidth variation in test structures

2.1. Test structures and data

Test structures that vary metal linewidth were implemented with 45 nm technology, where linewidth is the width of the Cu interconnect lines. Our test structure set contains three test structures with fixed linespace, *S*. The test structure with minimum linewidth is referred to as 1*X*. The structure with linewidths that are *N* times the minimum linewidth is referred to as *NX*. In total, we have 1*X*, 3*X*, and 5*X* test structures. Note that these test

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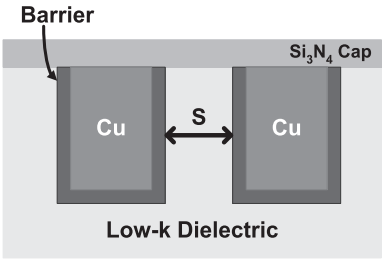

Fig. 1. Cross-section of an example copper/low-*k* interconnect system.

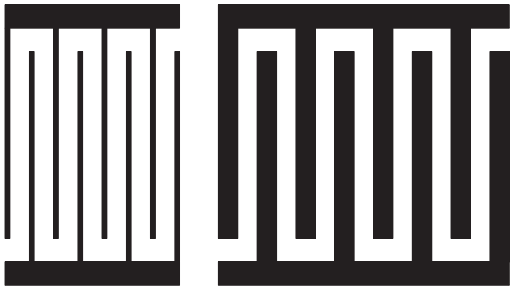

Fig. 2. Test structures that vary both linewidth and density concurrently (top view).

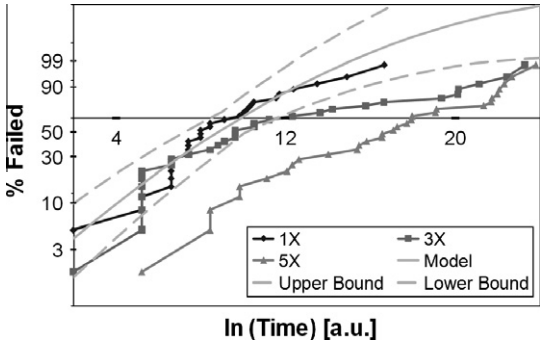

Fig. 3. Time-to-failure distributions for test structures with 1*X*, 3*X*, and 5*X* linewidths. 90% confidence bounds are for the 1*X* test structure, based on data in [10,11].

structures vary both linewidth and density concurrently, as illustrated in Fig. 2.

Experimental data indicates that time-to-breakdown is a function of linewidth. Fig. 3 shows the failure rate distribution for the test structures with 1*X*, 3*X*, and 5*X* linewidths. The confidence bounds on the 1*X* test structure show that the increase in lifetime for test structures with wider lines is statistically significant.

Let's suppose that the lifetime is modeled with a Weibull distribution with two parameters: the characteristic lifetime, η, and the shape parameter, β. The characteristic lifetime is the intercept of the $\ln(t)$ axis. It increases with linewidth. The shape parameter, β, is the slope. It cannot be extracted directly, since the Weibull curves are impacted by die-to-die linewidth variation. The die-to-die variation was extracted in [10,11], by accounting for the difference between β (extracted by area scaling) and the slope of the Weibull curves. Assuming the same die-to-die variation, β was extracted by curve fitting. β decreases for the test structures with wider lines.

Because the 1*X*, 3*X*, and 5*X* test structures confound area and density, a non-uniform test structure was implemented to decouple the impact of linewidth and density. This test structure is labeled as 1*X*/5*X*, since it matches the linewidths of the 1*X* and 5*X* structures. It matches the density of the 3*X* structure, as seen in Fig. 4.

Fig. 5 compares data from the non-uniform 1*X*/5*X* structure with the 3*X* structure, which matches its density. The failure rate curves do not match. Density does not appear to be the cause of the difference in lifetime.

2.2. Modeling variation in line space

Manufactured geometries were collected for the test structures using scanning electron microscopy. The data is shown in Fig. 6. In the graph, the linewidth difference is $\Delta W = W_{ACTUAL} - W_{DRAWN}$. The graph indicates that the narrow lines are wider than drawn, and the wide lines are narrower than drawn. The shift in linewidth as a function of drawn linewidth is statistically significant at a 10%

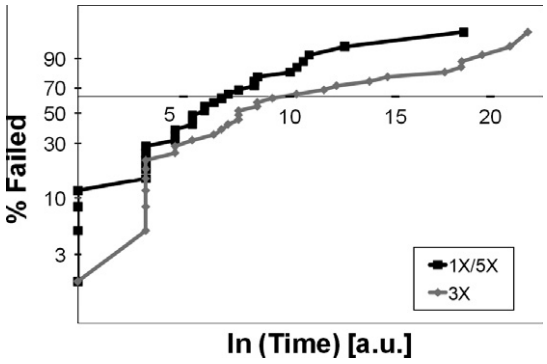

Fig. 5. Failure rate distribution for equal density structures (in Fig. 4).

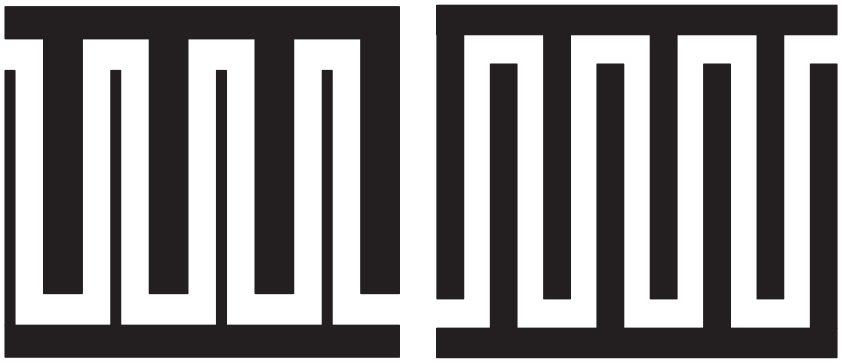

Fig. 4. A test structure pair that can distinguish between the impact of density and linewidth (top view).

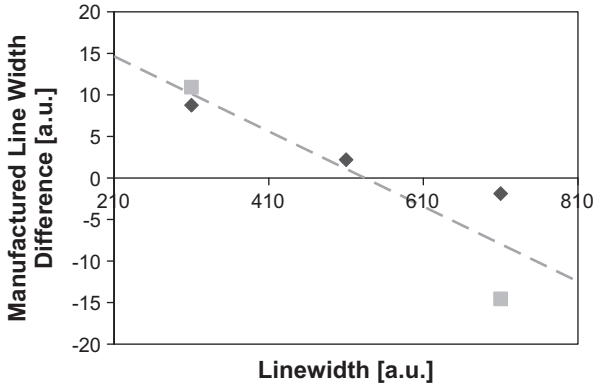

Fig. 6. The manufactured shift in linewidth as a function of linewidth on the mask. The black and grey dots correspond to the uniform and non-uniform test structures, respectively. The model is computed with regression.

level of significance. Therefore, even with this small sample size, variation in linewidth cannot be attributed to random variation (line edge roughness) only.

The data shows a correlation between linewidth and line height, because the process uses a timed etch, rather than an etch stop layer. Line height is assumed to be proportional to the etch rate, and a model was computed for etch rate as a function of aspect ratio in Fig. 7.

Aspect ratio dependent etching (ARDE) manifests itself in submicron features having high aspect ratios (feature height/feature width). In the presence of ARDE, higher aspect ratio trenches etch slower [12,13]. When the etch rate increases with trench size, this indicates that the process is chemically-controlled. Ion bombardment is not controlling the etch. Instead the concentration of etchant species entering the trenches increases with increasing trench width. Therefore, as the trench width increases, more etchant enters the trench, thereby increasing the etch rate.

It appears that the etch rate is composed of two different etch rate components, the lateral etch rate and the vertical etch rate, both of which depend on aspect ratio. The impact of the lateral component on linewidth as a function of aspect ratio is illustrated in Fig. 8. The lateral etch rate decreases with increasing aspect ratio.

There is asymmetry in lateral etch. We partition the shift into right and left sides of the trench. Fig. 9 shows the overall shift in width, ΔW, as a function of the widths on each side of the dielectric. This is the sum of the shift on the right and the left of the dielectric. The contour is based on the five measured linewidths.

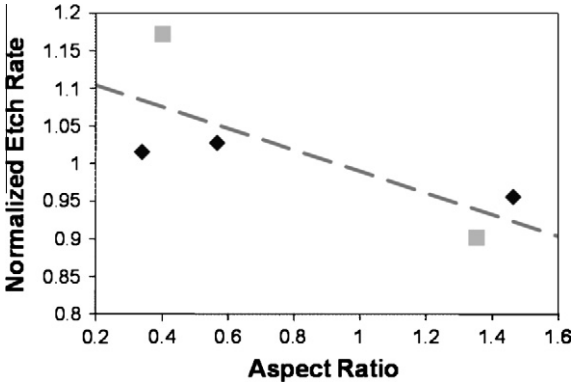

Fig. 7. The etch rates for test structures as a function of aspect ratio, showing ARDE. The aspect ratio is computed using measured data. The black dots and grey dots correspond to the uniform and non-uniform structures, respectively. The model is computed with regression.

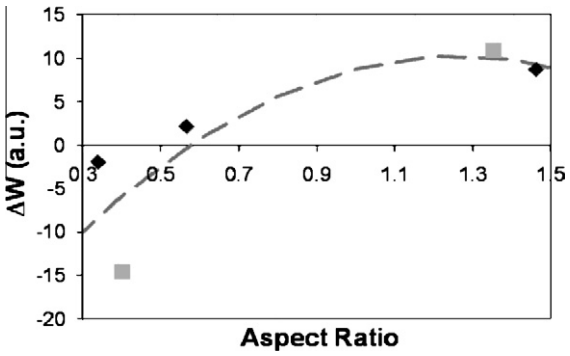

Fig. 8. Variation in linewidth as a function of aspect ratio. The black and grey dots correspond to the uniform and non-uniform test structures, respectively. The model is fit with regression.

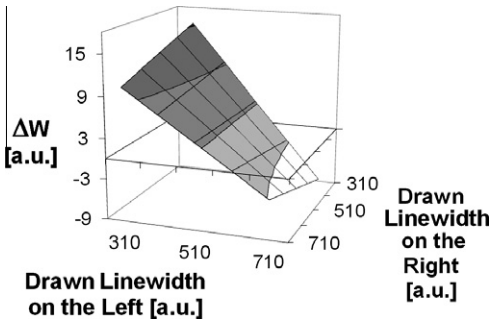

Fig. 9. Variation in line space as a function of the width of the lines on either side of the dielectric. The model is fit to the five data points.

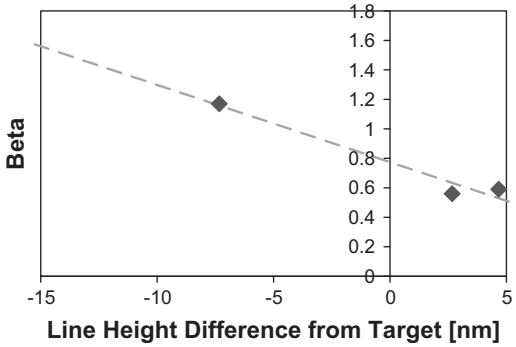

Fig. 10. Variation in beta as a function of line height. The model is fit with regression.

To compute lifetime for an arbitrary vulnerable area in the layout, one determines the widths of lines on each side of the vulnerable area, and then looks up the shift in line space from Fig. 9 to find the printed line space.

It turns out that β is also a function of the height of the lines, as shown in Fig. 10. Therefore, to compute the beta for an arbitrary vulnerable area in the layout, one finds the aspect ratio of the lines on each side. From Fig. 7, the etch rate is determined and converted to a line height difference from the target. Beta is then estimated from Fig. 10. If a vulnerable area is surrounded by two lines of different widths and aspect ratios, the beta is the average for the two lines.

3. Modeling characteristic lifetime

In accordance with the E or $\sqrt{E}$ model, characteristic lifetime is a function of the electric field in the dielectric. The electric field is a function of distance between the lines. For a pitch, P, the line space, S_{ACTUAL}, is

$$S_{ACTUAL} = P - W_{ACTUAL} \text{ or } S_{ACTUAL} = S_{DRAWN} - \Delta W. \quad (1)$$

Fig. 9 shows ΔW for any segment of dielectric.

The electric field is proportional to $1/S_{ACTUAL}$. For the $\sqrt{E}$ model, we have

$$\eta = A + B/\sqrt{S_{DRAWN} - \Delta W}, \quad (2)$$

where A and B are constants.

It has been noted that the characteristic lifetime is dependent on line edge roughness (LER) [4,5,14–16]. LER reduces the effective line space, i.e.

$$S_{EFF} = S_{ACTUAL} - \Delta S_{LER}(\sigma^2_{LER}), \quad (3)$$

where σ^2_{LER} is the variance of LER. The effective line space is reduced as the variance of LER increases. For the $\sqrt{E}$ model, $\eta = A + B/\sqrt{S_{EFF}}$.

The impact of LER is significant when line spaces are below 50 nm. In this case, $\Delta S_{LER}(\sigma^2_{LER})$ needs to be extracted from the dataset. However, our test structures have larger line spaces. The measured LER is less than 10% of the line space, and LER does not have a significant impact on our data.

4. Model verification

We now aim to predict the characteristic lifetime for the non-uniform test structure based on data from the uniform test structures. We do this by combining the Weibull cumulative probability density function of the time-to-failure (t) for a population $P(t) = 1 - \exp(-(t/\eta)^{\beta})$, and the Poisson defect distribution $P(t) = 1 - \exp(-\lambda(t)A)$ to get a time-dependent defect generation function $d(t) = \lambda(t)A = (t/\eta)^{\beta}$.

The 1X/5X test structure contains half of its vulnerable dielectric area with 1X linewidth on the left and 5X linewidth on the right, and it contains half of its vulnerable area with 5X linewidth on the left and 1X linewidth on the right. Therefore, its characteristic lifetime should be a combination of characteristic lifetimes of structures with these two vulnerable areas: $\eta_{1X,5X}$ and $\eta_{5X,1X}$. Let $\eta_{1X,5X}$ and $\eta_{5X,1X}$ correspond to defect densities, $\lambda_{1X,5X}(t)$ and $\lambda_{5X,1X}(t)$, respectively. The combined defect generation function, for test structure 1X/5X, is $d(t) = \lambda_{1X,5X}(t)A/2 + \lambda_{5X,1X}(t)A/2$, i.e.

$$d(t) = \frac{1}{2}\left(\left(\frac{t}{\eta_{1X,5X}}\right)^{\beta_{1X/5X}} + \left(\frac{t}{\eta_{5X,1X}}\right)^{\beta_{1X/5X}}\right), \quad (4)$$

where A is the vulnerable area of the uniform test structures and $\beta_{1X/5X}$ is the shape parameters.

Substituting (4) into the Poisson model, the cumulative probability density function for the non-uniform structure is

$$P(t) = 1 - \exp\left(-\frac{1}{2}\left(\left(\frac{t}{\eta_{1X,5X}}\right)^{\beta_{1X,5X}} + \left(\frac{t}{\eta_{5X,1X}}\right)^{\beta_{1X,5X}}\right)\right). \quad (5)$$

Since the characteristic lifetime, $\eta_{1X,5X}$, of the non-uniform structure corresponds to $P(t) = 0.625$:

$$\eta_{1X/5X} = \left(\frac{1}{2}\left(\frac{1}{\eta_{1X,5X}^{\beta_{1X/5X}}} + \frac{1}{\eta_{5X,1X}^{\beta_{1X/5X}}}\right)\right)^{-1/\beta_{1X/5X}}. \quad (6)$$

There are no test structures corresponding to $\eta_{1X,5X}$ and $\eta_{5X,1X}$. Therefore, $\eta_{1X,5X}$ and $\eta_{5X,1X}$ are evaluated with (2). The constants, A and B, are determined using data from the uniform test structures. The data in Fig. 9 determine ΔW. β is computed by estimating the normalized etch rate from Fig. 7, as a function of aspect ratio of the two lines. The normalized aspect ratio is converted to an estimated line height. The corresponding values of β are determined from Fig. 10. These are averaged. The estimate of β is 0.81. The value determined from the Weibull curve for the 1X/5X test structure is 0.83. Fig. 11 shows the predicted values of the characteristic lifetime. The model matches the data reasonably well.

5. Full chip analysis

5.1. Vulnerable area

The vulnerable area for a segment of dielectric is the dielectric area bordered by two lines. The feature that is extracted from the layout is the vulnerable length, L_i, associated with a line space, s_i. Line space, s_i, is a function of the widths of the two adjacent lines, W_L and W_R. The vulnerable length, L_i, for a dielectric surrounded by lines separated by line space, s_i, is illustrated in Fig. 12.

The layout is analyzed by determining the pairs ($s_i(W_L, W_R)$, L_i) for each layer, for all line spaces $s_i(W_L, W_R)$.

To find $s_i(W_L, W_R) = S_{ACTUAL}$ for a dielectric area, we first find the width of the lines on each side using the layout. We then use the data in Fig. 9 to find the shift in width, ΔW, for each line space, and S_{ACTUAL} is computed with (1).

5.2. Characteristic lifetime for a layer

Let's suppose that a test structure has a vulnerable length, L_{test}, corresponding to line spacing s_{test}. Let's suppose that the vulnerable length in a layer of the full chip layout corresponding to s_{test} is s_f. Let η_{test} be the measured characteristic lifetime of the test structure. Then, the characteristic lifetime of all features in the full chip layout corresponding to a line spacing of s_{test} is

$$\eta_f = \eta_{test}\left(L_{test}/L_f\right)^{1/\beta_f}, \quad (7)$$

where β_f corresponds to the target vulnerable area.

A full chip layout may have many line spacings not included in the test structure set. In this case, we estimate ΔW with Fig. 9 and η_{test} with (2).

A full chip layout has many different line spacing, s_f. To combine the failure rates for all line spacings, as was done for the non-uniform test structure, $d_f = (t/\eta_f)^{\beta_f}$ is computed for each line spacing

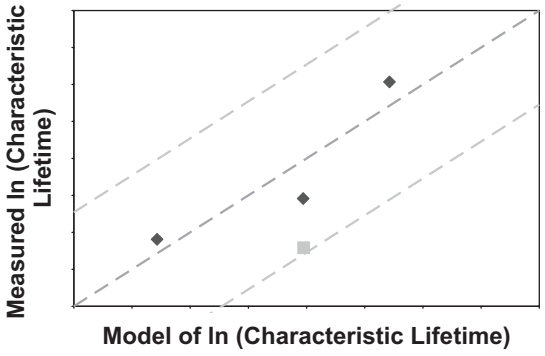

Fig. 11. Model vs. measured characteristic lifetime. The black dots correspond to the uniform test structure, from which the model was constructed. The 2σ confidence bounds for the model are shown. The grey dot corresponds to the non-uniform test structure.

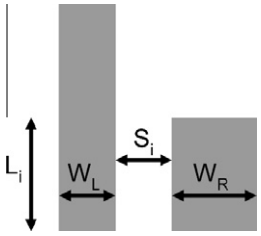

Fig. 12. The vulnerable length, L_i, is the length for which two lines run side by side, separated by line space, S_i.

in the layout. The total defect count at failure is the sum, $d = \sum_f d_f$. Then, the characteristic lifetime at the probability point $P = 0.625$ in the Weibull distribution is implicitly defined as the solution of

$$1 = \sum_f (\eta/\eta_f)^{\beta_f}. \tag{8}$$

In the limit, when β_f is constant, then

$$\eta = \left(\sum_f \eta_f^{-\beta}\right)^{-1/\beta}. \tag{9}$$

Fig. 13 shows the characteristic lifetime for each layer for an example JPEG encoder/decoder chip. The lifetime of layer 3 is shortest because it is the densest.

Fig. 14 shows the characteristic lifetime for each layer of another circuit example, a radix-2 pipelines FFT 8 chip. This graph compares the characteristic lifetime computed accounting for all geometries in a layer with two simplifications. One simplification uses only the most frequent line space (critical linespace), and the other includes only the smallest linespace. Significant errors result if lifetime is calculated based on only the vulnerable area associated with the smallest line space.

5.3. Failure statistics for the full chip

The full chip failure statistics are described by two parameters: the characteristic lifetime of the chip, η_{chip}, and the shape parameter for the chip, β_{chip}.

Let d_l be the defect density for each layer, $d_l = \sum_{f(l)} d_{f(l)}$, each composed of many feature line spaces, $f(l)$, corresponding to defect counts at failure, $d_{f(l)}$. Overall, for the chip, $d_{chip} = \sum_l d_l$.

Unlike for a single layer, multiple layers of a chip may have different process details. Therefore, data needs to be collected from test structures for each layer separately, i.e. $L_{test(l)}$, $\eta_{test(l)}$, and $\beta_{f(l)}$ are unique to each layer. $\eta_{f(l)}$ is computed for each feature in each layer with (7).

If β were common to all layers and all features, then it is possible to solve for the characteristic lifetime of the chip, η_{chip}:

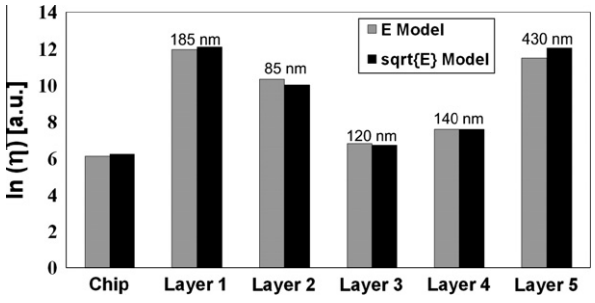

Fig. 13. Characteristic lifetime for individual layers and the complete chip for a JPEG decoder/encoder. The figure also shows the most frequent line spacing for each layer.

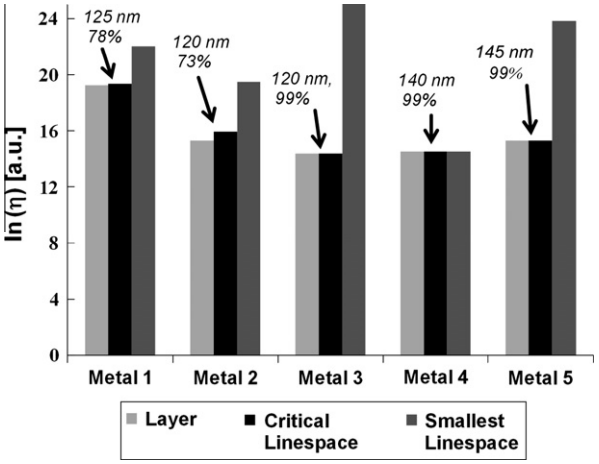

Fig. 14. Characteristic lifetime for individual layers for, a radix-2 pipelined FFT 8 chip. The figure also shows the most frequent line spacing for each layer and the percentage of vulnerable area covered by this most frequent line spacing. It compares the estimated lifetime including all vulnerable areas, the vulnerable area associated with only the most frequent vulnerable area (critical line space), and the vulnerable area associated with only the smallest line space.

$$\eta_{chip} = \left(\sum_l \sum_{f(l)} \eta_{f(l)}^{-\beta}\right)^{-1/\beta}. \tag{10}$$

Otherwise, η_{chip} is implicitly defined

$$1 = \sum_l \sum_{f(l)} (\eta_{chip}/\eta_{f(l)})^{\beta_{f(l)}}. \tag{11}$$

The characteristic lifetime for the JPEG encoder/decoder chip is shown in Fig. 13. It can be seen that the characteristic lifetime of the full chip is close to that of layer 3, the most dense layer.

Projection of time-to-failure at small probabilities, P, requires not just η_{chip}, but also β_{chip}, where β_{chip} is

$$\beta_{chip} = \left.\frac{\delta(ln(-ln(1-P)))}{\delta(ln(t))}\right|_{t=\eta_{chip}}. \tag{12}$$

P is the cumulative probability density function of failure for the chip. Solving,

$$\beta_{chip} = \sum_l \sum_{f(l)} \beta_{f(l)} \left(\eta_{chip}/\eta_{f(l)}\right)^{\beta_f(l)}. \tag{13}$$

To compute the lifetime at probability point, P, say, $P = 0.0001$, the lifetime, t, is

$$t = \eta_{chip}(-ln(1-P))^{1/\beta_{chip}}. \tag{14}$$

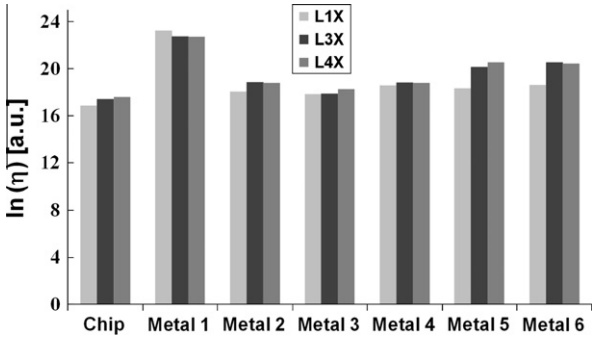

Fig. 15. Characteristic lifetime for different instantiations of the FFT8 chip. The metal 3 linewidth of L3*X* and L4*X* is three and four times the linewidth of L1*X*, respectively.

5.4. Impact of changes in linewidth on lifetime

According to the model in Fig. 9, changes in linewidth result in changes in line space. To assess how ARDE impacts characteristic lifetime, we generated three different instantiations of our example radix-2 pipelined FFT 8 chip. The reference layout is labeled L1*X*. L3*X* and L4*X* have metal 3 that is three and four times wider than the linewidth of metal 3 in L1*X*. Fig. 15 shows that the change in linewidth increases the characteristic lifetime for all of the layers, as well as for the chip. The increase in lifetime for all layers can be attributed to a change in the routing for all layers due to the smaller number of routing tracks in metal 3. Hence, the increase in vulnerable area due to re-routing has a greater impact by degrading lifetime, outweighing any improvement in lifetime due to the use of wider metal 3 lines.

6. Conclusions

This paper has analyzed data from test structures with varying linewidths, while holding line space constant. The data indicates a link between linewidth and lifetime. Analysis indicates that variation in lifetime is not due to variation in density, but rather due to ARDE. Using test structure data, a model was constructed linking the shift in line space to the widths of lines surrounding a vulnerable dielectric area.

The full chip lifetime is characterized with a characteristic lifetime and a shape parameter. These parameters are computed based of the vulnerable dielectric area for all geometries in a chip, together with parameters extracted from test structure data.

Future work aims to also take into account the impact of variations in temperature and detailed analysis of the electrical signals within a chip.

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