Signal Integrity Analysis and Optimization for 3D ICs

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***Abstract*— This paper studies the TSV-to-TSV coupling issues in 3D ICs and introduces a methodology for performing signal integrity (SI) analysis considering TSV-to-TSV coupling for 3D ICs. 3D SI analysis results show that TSV coupling has big impact on the SI in 3D ICs. A TSV-KOZ sizing methodology and a force-directed placement-refinement approach are proposed to alleviate the 3D SI problem. Experimental results show that using different larger KOZ sizes can achieve a 22%-55% total coupling-noise reduction and a 12%-39% critical path delay reduction. By using placement refinement approach, the total coupling-noise is reduced by 32% and the critical path delay is reduced by 10% while maintaining the same chip area. Therefore these two approaches are both effective in alleviating the TSV-caused SI problems in 3D ICs.**

I. Introduction

Through-Silicon-Via (TSV) and 3D stacking technology are currently being actively evaluated as a potential solution to alleviate the interconnect delay problems in giga-scale circuits and systems[1]. Some works have been done to show that 3D ICs have advantages in total wire length[2] and timing performance[3] compared to 2D ICs.

However, signal integrity (SI) is another key challenge caused by the advance nano-scale interconnect technologies due to the rising number of analog effects. Due to the big size of TSVs[3], it's highly possible that TSVs will introduce new coupling sources, which are bad to the circuit's SI performance. The potential coupling sources include TSV-to-device coupling, TSV-to-TSV coupling, landing-pad-to-metal coupling, landing-pad-to-landing-pad coupling, etc. Several works have been done to illustrate the impact of TSVs on SI in 3D ICs[4][5][6]. However, those studies only look at simple individual coupling cases in device level. To obtain a comprehensive understanding of SI issues in 3D ICs, we still need to answer the following two questions: 1) How much SI issues do the TSVs cause to the 3D IC design from a full-chip perspective? 2) If the impact of TSVs to the full-ship SI is non-negligible, how should we alleviate the TSV-caused problem from a designer's perspective?

This paper tries to answer these two questions. The main contribution of this work includes: 1) Studied the impact of TSV-coupling on SI in 3D ICs. 2) Proposed a 3D SI analysis flow considering the TSV coupling. 3) Proposed two approaches to alleviate the TSV-caused coupling problem. One is by using TSV keep-out zone (KOZ). The other is by using force-directed placement refinement framework.

II. Impact of TSV Coupling on Signal Integrity

TSVs introduce several new coupling sources to 3D ICs, as shown in Figure 1. The first coupling source is from the big TSV landing pad to the wires and devices. Considering the TSV landing pad is big (typically 100 μm^2) which occupies several standard cell rows, the metal running above or next to it will suffer from big coupling capacitance. Fortunately, this coupling source can be analyzed by existing SI tools easily[7], because it's essentially a traditional wire coupling problem.

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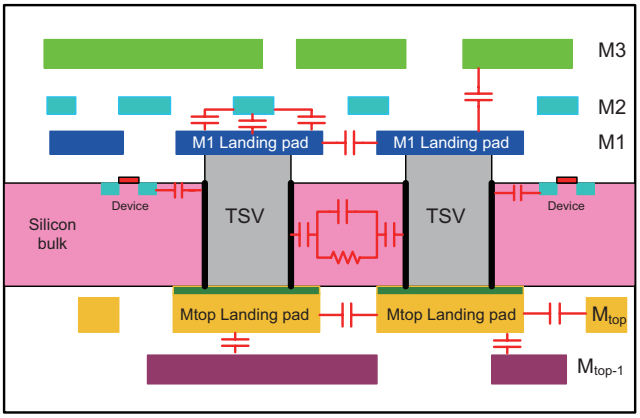

Fig. 1. An illustration of TSV related coupling

Another coupling source is from TSV-to-device coupling. This coupling happens between the TSV and the S/D region of the MOSFET through the substrate[8]. The coupling path is mainly on the silicon-bulk surface. Therefore, by adding sufficient substrate contact, the surface can be strongly tied to ground, thus alleviating TSV-to-device coupling.

The third coupling source is from TSV-to-TSV coupling. Different from TSV-to-device coupling, TSV-to-TSV coupling happens not only on the silicon-bulk surface, but also deep inside the substrate, because a TSV is a via that goes through the entire substrate. Therefore, simply adding substrate contact cannot guarantee to eliminate this coupling. Recently, there are several works done to investigate the TSV-to-TSV coupling on the device level[4][5][6][9]. [5] studies a specific case where 9 TSVs are placed as a 3×3 array. [9] analyzes the factors that contribute to TSV coupling from a process and device perspective. [6] gives an analytical model for the coupling capacitance between TSVs. Equation 1 shows the TSV coupling model used in this paper.

$$C_C = 0.4\alpha\beta\gamma \cdot \frac{\epsilon_{si}}{S}\pi DL \quad (1)$$

where α, β, γ are all fitting parameters, S is the distance between the TSVs, and D is the TSV diameter. This models implies that the TSV-to-TSV coupling capacitance is inversely proportional to the TSV distance.

All these studies explore the TSV-to-TSV couplings individually and show how much coupling TSVs cause in some simple cases. However, whether this TSV coupling will cause troubles in a real digital design containing many gates and TSVs still leaves a question. In this section, we try to answer this question by doing full-chip SI analysis considering TSV-related coupling. The TSV-related coupling we are dealing with in this paper is mainly TSV landing-pad related coupling and TSV-to-TSV coupling. The former can be handled by existing tools (CeltIC, Primetime etc). We use the coupling model in Equation 1 to calculate TSV-to-TSV coupling. Notice that all the

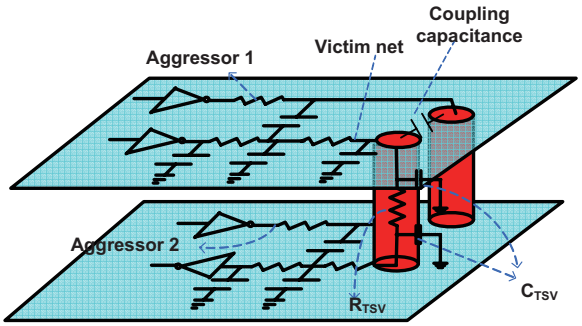

Fig. 2. An illustration of 3D victim net

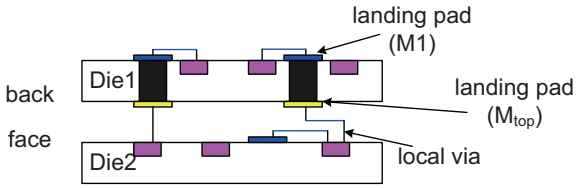

Fig. 3. An illustration of 3D structure

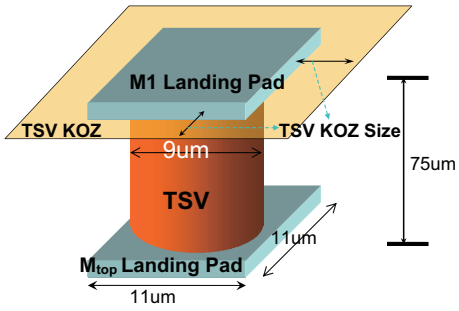

Fig. 4. An illustration of TSV structure

analysis and optimization methodologies proposed in this paper are flexible with models and not limited to Equation 1. Considering these TSV coupling sources, this section studies the impact of TSVs on 3D SI from a full-chip perspective.

A. Full chip 3D SI analysis flow considering TSV-to-TSV coupling

Currently, there is no SI analysis tool designed for 3D circuits. A 3D SI analysis tool must consider all nets and all TSVs in all the tiers simultaneously, because the total noise experienced by a 3D net may come from coupling within the same tier as well as neighboring tiers. Figure 2 shows a 3D net whose aggressors come from both tiers.

We designed our 3D SI flow, which utilizes our own scripts in combination with the existing commercial SI (= CeltIC) and timing analysis (= PrimeTime) tools. First, we use RC extraction tool to obtain the SPEF files containing the interconnect RC information for each die. Then by using Equation 1, we made a script which inserts the TSV parasitics and TSV-to-TSV coupling capacitances automatically based on the locations of TSVs, and writes the TSV-coupling information into a top-level SPEF file.

Once these files are ready, we use PrimeTime to read in verilog files and SPEF files in incremental mode, and generate a new stitched SPEF file containing the RC information of all the dies and the TSVs. With this stitched SPEF file, we use CeltIC to perform signal integrity analysis.

B. Analysis results and comparisons

We use VM64, which is a 64-bit multiplier as a test circuit. The circuit has 61K gates and 435 TSVs. The design is a 2-layer 3D IC based on 45nm technology. The 3D structure used in this design is shown in Figure 3. In this 3D structure, the TSVs, which are all located on the top die, go through the substrate and contact with the top metal landing pad of the bottom die. Figure 4 shows a TSV cell structure, which consists of a TSV pillar and two landing pads. The TSV is $9\mu m$ in diameter and $75\mu m$ in height. The TSV landing pad is a $11\times11\mu m^2$ square in metal 1 which occupies 4 standard-cell rows. Usually a TSV cell has a keep-out zone (KOZ), where no other devices and TSVs can be placed inside. We define the distance between the M1 landing-pad and the keep-out zone edge as the TSV KOZ size. From Figure 4, we can see that the actual area a TSV cell occupies is determined by the sum of landing pad size and the KOZ size.

Figure 5(a) shows a 3D design flow. First a min-cut partitioner is used to partition the top level design into two dies. Each cut becomes a pin in each die, which corresponds to a TSV.

Next, we place TSVs and standard cells sequentially. We first convert the TSV pins to TSV standard cells which we define in the physical library (.LEF). Then we place the TSV cells and standard cells together in the first die using the predefined pin locations as constraints. After placement, we change TSV standard cells back to TSV pins so that we can do routing and optimization as the usual design flow.

For the second die, we first get the TSV landing pad locations from the previous die. With these locations as constraints, we do placement and routing. The following steps are the same as in the first die.

Figure 6 and Figure 7 show the glitch-analysis results and coupling-caused delay degradation results on VM64 design respectively. The analysis compares two cases where TSV-to-TSV coupling is considered, and is not considered. We can see that for both glitch and delay degradation analysis, TSV coupling has significant contributions to the total coupling noise and delay, especially in the high noise region. From Table I, we can see that TSVs contribute 50% more total glitch noise and 277% more total delay degradation compared to the case without considering TSV coupling.

III. SI Refinement by TSV KOZ sizing

After realizing that TSVs have significant contribution to the 3D SI performance, we need to find a way to reduce TSV coupling. There are several possible ways to reduce the TSV induced coupling. Shielding by using Power/Ground TSVs is an effective way to cut off the coupling path. However, many Power/Ground TSVs need to be inserted around the victim signal TSVs, which will increase the total area significantly. Buffer insertion is another effective way to reduce the coupling noise. However, the total power consumption will increase because of the inserted buffers. From a design perspective, the most intuitive way is to increase the distance between TSVs. Figure 8 shows the relationship between TSV distance and TSV coupling capacitance. We can see that as the TSV distance increases, the coupling between them decreases. According to Equation 1, the coupling capacitance is reversely proportional to the TSV distance. This relationship indicates that TSV spacing is most effective in reducing coupling when the TSV distance is small. After TSVs are separated with certain distance, keeping on increasing the TSV distance will not have much impact in reducing coupling.

TABLE I

DESIGN AND SI ANALYSIS COMPARISONS

	3D no TSV coupling	3D with TSV coupling
Footprint (μm^2)	455×455	455×455
Silicon Area (μm^2)	2×455×455	2×455×455
Wirelength (μm)	926000	926000
Total noise (V): nets with noise bigger than 10mV	1072	1613
Total delay degradation (ns)	122	460

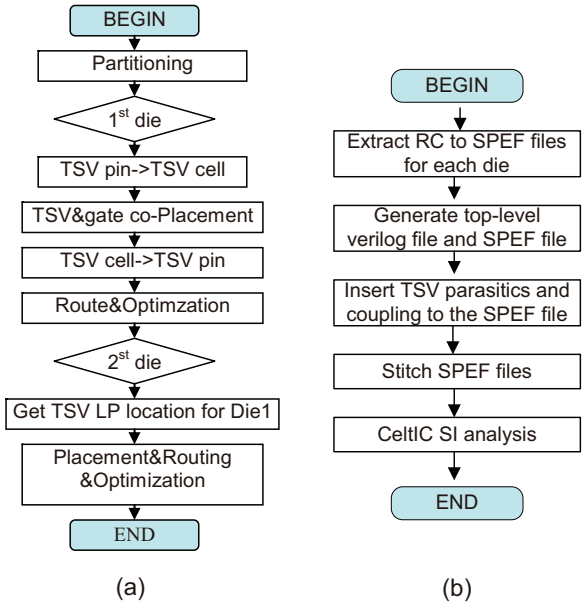

Fig. 5. (a) 3D design flow, (b) 3D SI analysis flow

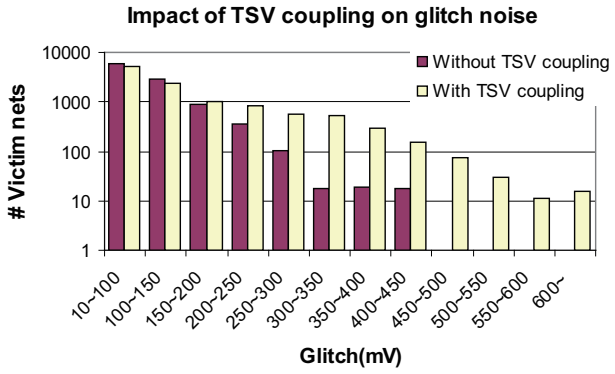

Fig. 6. Glitch analysis results comparison

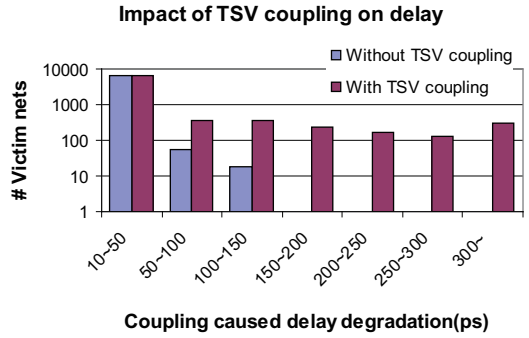

Fig. 7. Coupling-caused-delay-degradation analysis results comparison

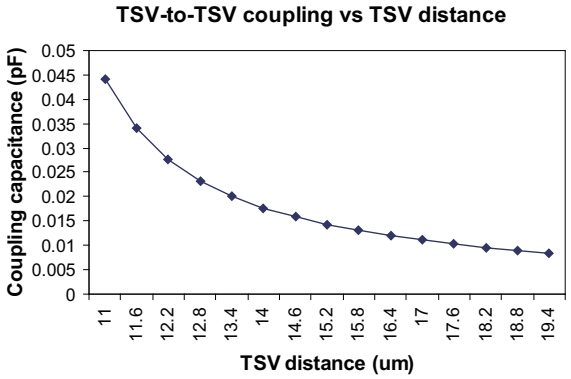

Fig. 8. TSV coupling with different TSV distances

The easiest approach to increase the TSV distance is to use a larger keep-out-zone (KOZ) for each TSV cell during placement in the physical design flow. In this study, we define the distance between landing pad edge and TSV cell edge as the TSV KOZ size (see Figure 4). If the KOZ size becomes larger, the distance between TSVs will naturally increase. Based on this phenomenon, we redo the design by increasing the KOZ size gradually.

The original TSV KOZ size is 0.7um. The TSV KOZ size we use for optimization is from 1um to 3.5um, as shown in Figure 9. Figure 14 shows a layout comparison between the original design and the design with 2um KOZ size. We first compute the total TSV coupling capacitance in these designs, as shown in Figure 10. We also draw a curve showing the total die area increase of these designs (also see Figure 10). We can see that the total TSV coupling capacitance decreases, while the footprint increases as we increase the TSV KOZ size. Depending on the KOZ size we use, the total TSV-coupling capacitance reduction is 28%-76%, while the total area increase is 4%-31%.

We also performed sign-off SI analysis with these designs based on the routed GDSII layout. The analysis contains glitch noise results and coupling-caused delay degradation results, as shown in Figure 11. We can see the same over-all trend: SI performance gets better as we increase the TSV KOZ size. With different KOZ sizes, we can achieve a 22%-35% total noise reduction.

3D timing analysis is also performed in these designs. Figure 12 shows the critical path delay and total wire length under different TSV KOZ sizes. We can see that the wire length increase is about 29% when we use the maximum KOZ. We can also see that although a larger TSV KOZ may result in a bigger area and total wirelength, which potentially harms the timing, the critical path delay is still

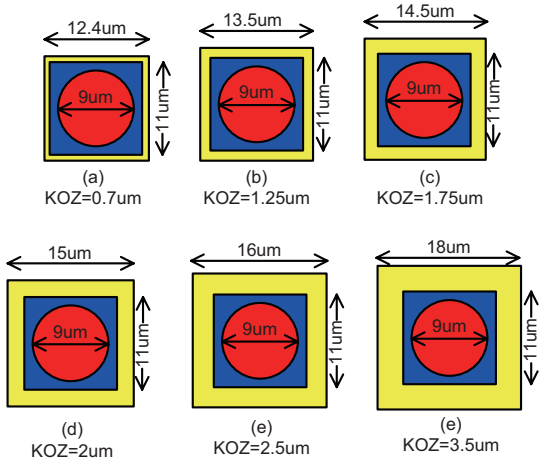

Fig. 9. TSV cells with different TSV KOZ size

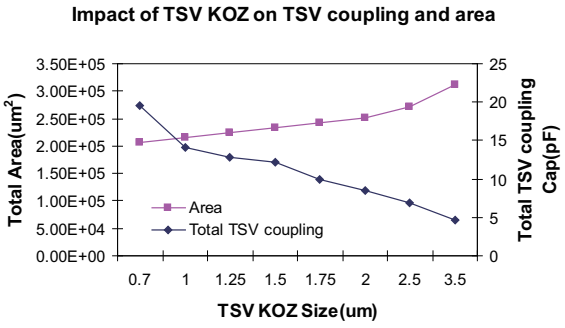

Fig. 10. The impact of KOZ size on total TSV coupling and chip area

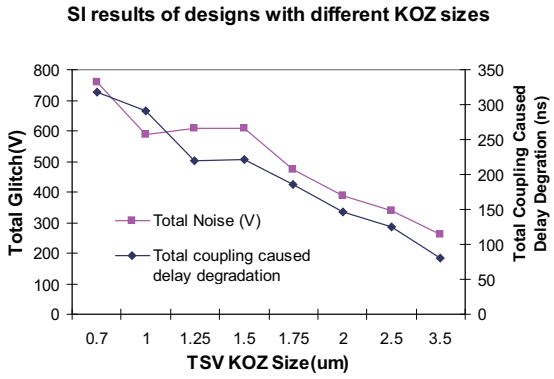

Fig. 11. The impact of KOZ size on SI results (glitch and delay degradation)

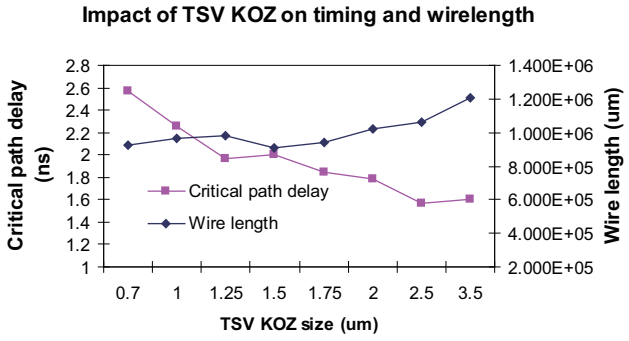

Fig. 12. Timing analysis results under different TSV KOZ sizes

better as we increase the TSV KOZ size before TSV KOZ size reaches 3.5um. By increasing TSV KOZ size, we obtain a 12%-39% critical path delay reduction. This is because in this region, the TSV coupling plays a dominant role on path delay compared to the wirelength. Thus a bigger TSV distance helps to alleviate the delay degradation caused by TSV-coupling, which in turn improves overall timing. We also notice that when TSV KOZ size reaches 3.5um, the timing result begins to degrade. This is because the increasing wirelength begin to play a dominant role in the critical path delay at this point.

IV. TSV Coupling Aware Placement Refinement

Although increasing the TSV KOZ is effective in alleviating SI problems in 3D ICs, keeping a fixed KOZ is still not the most optimized way to reduce coupling. One reason is that a larger KOZ requires a larger chip area, which may not be desired when the area constraint is very strict. And a larger area will cause a higher possibility of longer wirelength, which is not desired because of timing issues. Another reason is that using a fixed KOZ for every TSV is too arbitrary. Since the coupling environment for each TSV is different, a fixed keep-out distance may not be enough for some cases (see the victim TSV in Figure 13(a), or may be overcompensated for other cases (see the victim TSV in Figure 13(b).

To overcome the above problems and better optimize the design, we propose a placement refinement algorithm to reduce the coupling between TSVs. Our refinement framework is based on a force-directed placement approach[10], where a new force called "coupling force" is added to separate TSVs thus alleviating the TSV-to-TSV coupling problem. This refinement framework has the following merits:

- Since the noise force applied to a TSV is computed based on the coupling level on it, the framework is capable of handling different coupling environment. Thus the problem in Figure 13 will not happen.
- This approach doesn't necessarily require larger chip area, because it doesn't need a larger TSV cell.
- This approach considers wirelength, density, and coupling simultaneously by using different forces and weights. Therefore it's a multi-objective optimization framework where we can tune the objective function freely based on our interest.

A. Brief Review of Force-Directed Placement

Kraftwerk2 is a fast force-directed quadratic placement approach proposed in [10]. It formulates the placement problem as a global electrostatic problem and applies three different forces to the cells: net force, move force and hold force. The net force is coming from the quadratic placement methodology, which is targeting at minimizing total wirelength. Since the squared Euclidean distance between two movable cells i and j is:

$$(x_i - x_j)^2 + (y_i - y_j)^2 \tag{2}$$

The quadratic cost function in x direction can be written in matrix-vector notation, as shown in Equation (3)

$$\Gamma = \frac{1}{2} x^T C_x x + x^T d_x + const \tag{3}$$

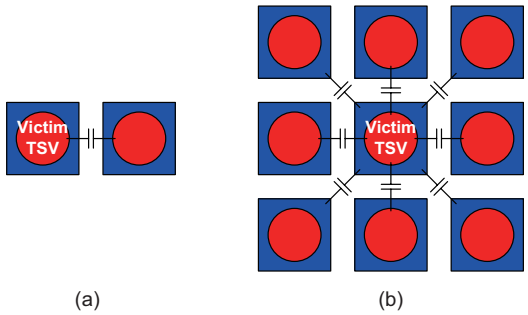

Fig. 13. Limitation of fixed KOZ approach. (a) KOZ is overcompensated, (b) KOZ is not enough

Minimizing the total wirelength requires the solution of Equation (4).

$$F_x^{net} = C_x x + d_x = 0 \tag{4}$$

If we consider it as a spring system, $C_x x + d_x$ can be regarded as net force.

The move force is proposed to remove the overlaps among cells. Therefore it's a cell density force in nature. The basic idea is to consider the placement area as a electrostatic field. Each module has positive charge and the chip area has negative charge. These charge form a charge density D, which is dependent on the overlap among cells. The charge creates a potential Φ. By solving Poisson equation, we can calculate a target point:

$$\dot{x_i} = {x_i}' - \frac{\partial}{\partial x}\Phi|_{({x_i}', {y_i}')} \tag{5}$$

The move force can be calculated by Equation (6).

$$F_x^{move} = \dot{C_x}(x - \dot{x}) \tag{6}$$

The hold force $F_{x,hold}$ is defined by the negative net force, as shown in Equation (7). Therefore the sum of net force and the hold force is zero.

$$F_x^{hold} = -(C_x x' + d_x) \tag{7}$$

The total force is expressed in Equation (8). We set it to zero and solve it iteratively to get a placement with minimal wire length and some overlap reduction.

$$F_x = F_x^{net} + F_x^{move} + F_x^{hold} = 0 \tag{8}$$

B. Coupling Force

To implement a TSV coupling aware placer, we introduce a new force called "coupling force" into the force-directed placement approach. This force is similar to the move force. The major difference is that in the Poisson equation, we replace the density function $D(x, y)$ with coupling function $C(x, y)$, and the coupling force is only applied to TSVs. Using this coupling force, the TSVs that are too close to each other can be spread.

We still use Equation (1) to calculate the TSV coupling force on each TSVs. The placement can be represented as supply and demand system D. The demand of one TSV is proportional to its coupling noise number. To better describe it, we use a square function R.

$$R(x, y, x_u, y_u, w, h) = \begin{cases} 1 & \text{if } 0 < x - x_u < w \\ & \text{and } 0 < y - y_u < h \\ 0 & \text{if else} \end{cases}$$

The demand function of one TSV cell located at (x_i', y_i') with a width w_i and height h_i is

$$C_{TSV,i}^{dem}(x, y) = \frac{c_i}{A_i} \cdot R(x, y, x_i' - \frac{w_i}{2}, y_u - \frac{h_i}{2}, w_i, h_i) \tag{9}$$

where C_i is the coupling capacitance on this TSV, which can be calculated using Equation (1). A_i equals $w_i h_i$, which is the area of the TSV. The demand function of all the TSV cells is the sum of all the single TSV cells, as shown in Equation (10):

$$C^{dem}(x, y) = \sum_{i=1}^{N} C_{TSV,i}^{dem}(x, y) \tag{10}$$

In order to keep the supply and demand function balanced, we define the supply function as in Equation (11)

$$C^{sup}(x, y) = C_{sup} \cdot R(x, y; x_{chip}, y_{chip}, w_{chip}, h_{chip}) \tag{11}$$

where C_{sup} is defined as the total TSV coupling capacitance divided by the total chip area, as show in Equation (12):

$$C_{sup} = \frac{\sum_{i=1}^{N} C_i}{A_{chip}} \tag{12}$$

Thus, the coupling function can be represented in Equation (13)

$$C(x, y) = C^{dem}(x, y) - C^{sup}(x, y) \tag{13}$$

Using this coupling function, we can formulate the Poisson equation for the coupling force exactly the same way as the move force, as shown in Equation (14).

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2})\Phi_c(x, y) = -C(x, y) \tag{14}$$

Similar to the move force, the coupling force can be calculated in Equation (15)

$$F_i^{coupling} = w_i(x_i - \dot{x_i}) \tag{15}$$

where

$$\dot{x_i} = {x_i}' - \frac{\partial}{\partial x}\Phi_c(x, y)|_{(x_i', y_i')} \tag{16}$$

C. Dynamic Force Balancing

Adding up those four forces, we obtain the total force expression, as shown in Equation (17).

$$F_{total} = F_{net} + F_{hold} + \lambda_1 F_{move} + \lambda_2 F_{coupling} \tag{17}$$

where λ_1 and λ_2 are used for dynamically adjusting the weight of move force and coupling force. The reason we need these two coefficients is because we start from an existing layout where all cells are already spread enough. In this case, the initial move force tends to be very small. On the other hand, TSV-to-TSV coupling is significant at the beginning. Therefore the strong coupling force will move the crowded TSV away at the first iteration, which will create some overlaps. At the second iteration, due to the overlap created by the TSV movement, the move force tends to move the TSVs back to their original location, which is not desired. Thus we use λ_1 and λ_2 to give the coupling force a larger weight, and the move force a smaller weight at the first few iterations. After that, we gradually increase λ_1 and decrease λ_2, to gradually remove the overlaps created by the TSV movement.

Replacing F_{hold}, F_{move}, F_{net} and $F_{coupling}$ with their expression, we obtain the final equation for the computer to solve, as shown in Equation (18)

$$(C_x + \lambda_1 C_x^m + \lambda_2 C_x^c)\Delta x = -\lambda_1 C_x^m \Phi_x^m - \lambda_2 C_x^c \Phi_x^c \tag{18}$$

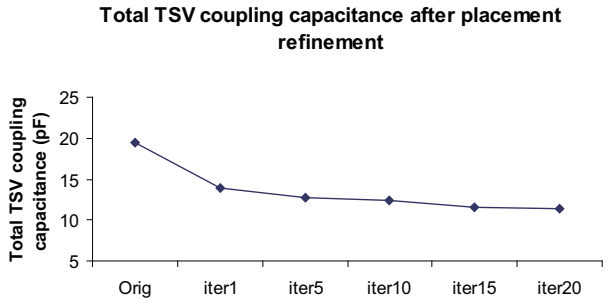

Fig. 16. TSV coupling capacitance after every 5 iterations

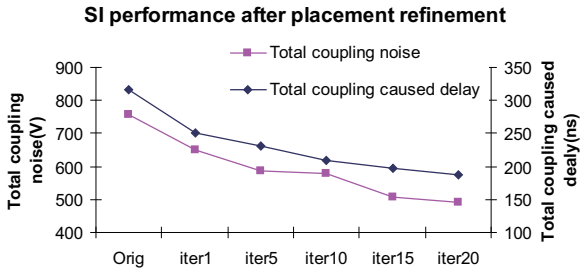

Fig. 17. SI analysis results after every 5 iterations

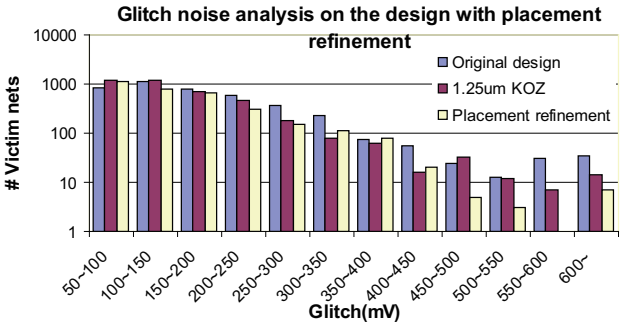

Fig. 18. Glitch distribution comparison among the three designs

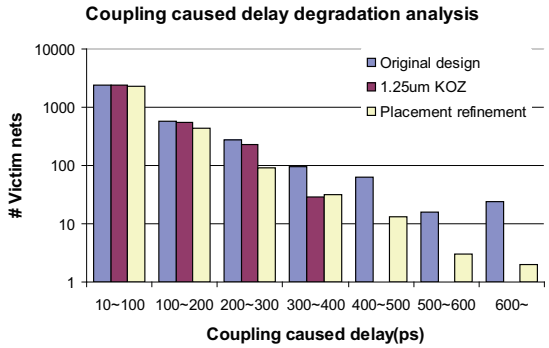

Fig. 19. Coupling-caused-Delay-degradation distribution comparison among the three designs

D. Experimental results

We apply the forced-directed placement refinement framework to the original VM64 design using the same area. We run 25 iterations with the placer. After every 5 iterations we do the routing and SI analysis. Figure 14 shows the layout after routing. Compared to the original design, the TSVs are more spread. Figure 15 shows zoom-in shots of various placement results.

The total TSV coupling capacitance and total wirelengh after each 5 iterations are shown in Figure 16. We can see that the total TSV coupling capacitance decreases by 41% at the 15th iteration, which means that the TSVs are spread. After several iterations, the total TSV coupling reduction rate becomes slower, which means that the placement refinement should stop at this point.

We did sign-off SI analysis on both glitch noise and coupling-caused delay degradation on the routed designs. Figure 17 shows the SI analysis results. Similar to the total TSV coupling capacitance, The same trend happens. As the TSVs get more and more spread, the total coupling noise and coupling-caused delay naturally decrease. Finally a 32% noise reduction is obtained. Figure 18 and Figure 19 show the detailed SI analysis results which contain the glitch and coupling-caused-delay distributions for the final placement. We can see that especially in high noise region, placement refinement is effective in reducing the glitch noise.

We are also interested in the over-all timing performance after placement refinement. Figure 20 shows the sign-off 3D timing analysis results on the routed designs including the critical-path delay and total negative slack (TNS). We can see that after placement refinement, the critical path delay reduces from 2.57ns to 2.3ns. This again shows that TSV-to-TSV coupling caused delay is a big bottleneck for timing performance in the original design. Notice that the total wire-length variation is very small after each iteration. This is because in most cases, the TSV movement is small. If the new TSV location is still in the original bounding-box of the 3D net, the TSV movement doesn't necessarily increase wirelength. Therefore we conclude that the TSV spreading using placement refinement helps to improve both SI and timing performance.

Then we compare the SI results of the four designs: original design, design with 1um KOZ, design with 2.5um KOZ and design with placement refinement. The over-all comparison results are show in Figure 21. We can see that the SI performance of all the three optimized designs are better than the original one. If we compare the three optimized designs, the design with 2.5um KOZ has the best over-all performance. However, the cost is a 31% area increase. In contrast, the design with 1um KOZ achieves a similar over-all performance improvement as the placement-refinement design, while the area overhead is only 4.4%. Therefore, by paying some area cost, we can achieve a much better performance. On the other hand, if the area requirement is very strict, then the placement refinement is the best approach, because it increases the SI and timing performance while maintaining the same area. Table II and Table III lists the detailed experimental results for both approaches.

V. Conclusions

This paper studied the impact of TSV-to-TSV coupling on SI from a full-chip perspective in 3D ICs. A 3D SI analysis flow is proposed to perform SI analysis in 3D ICs, where TSV coupling is considered. The 3D SI results show that the TSV-to-TSV coupling has a big contribution to the total glitch noise and coupling-caused delay degradation. Two approaches are proposed to alleviate the TSV coupling induced SI problem. Both TSV-KOZ sizing and placement refinement approaches help to improve SI as well as timing

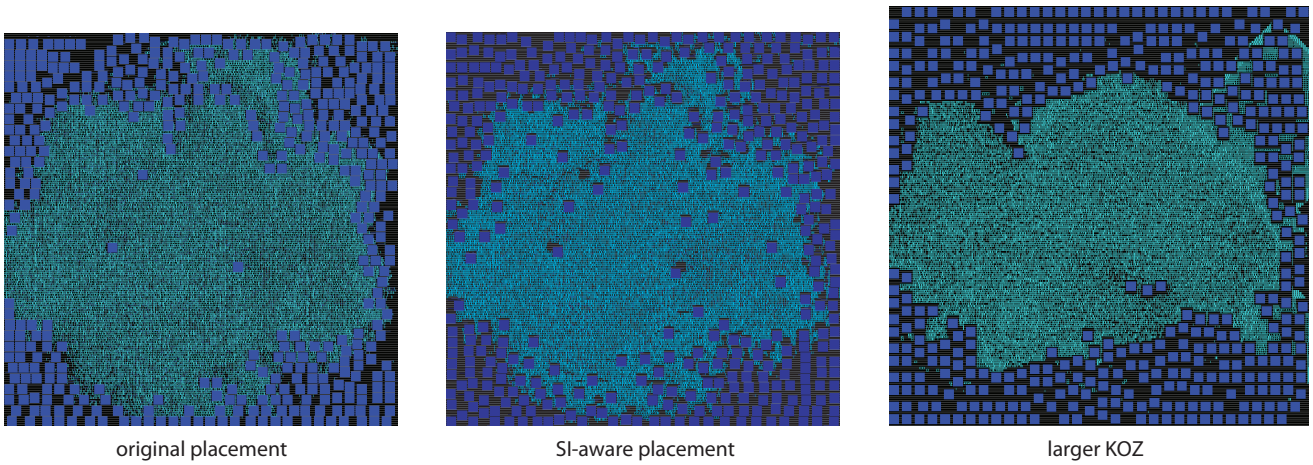

Fig. 14. Various full die shots using Cadence Encounter

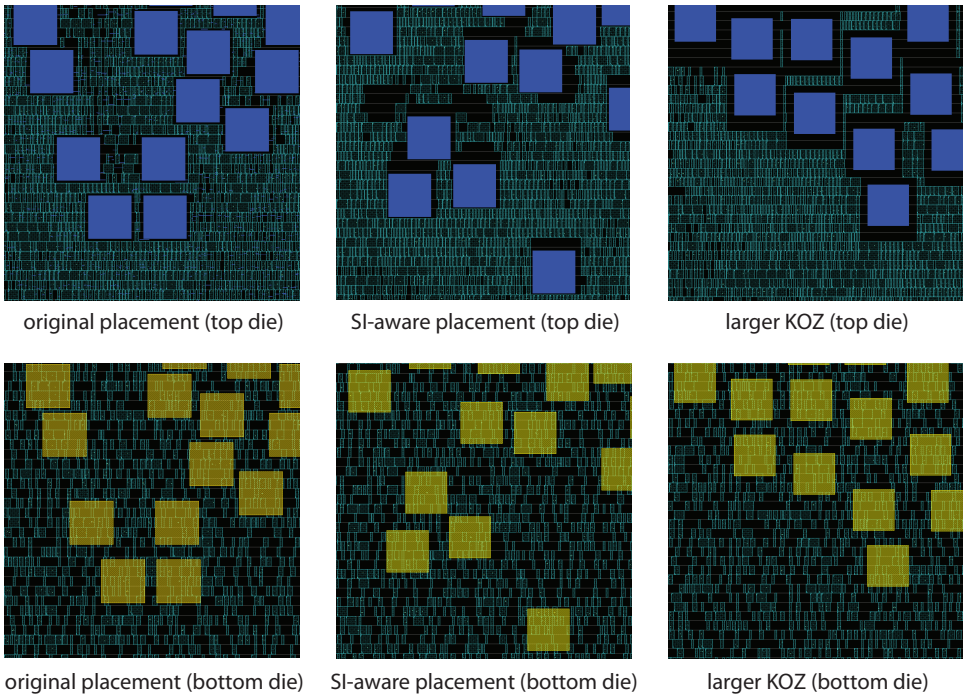

Fig. 15. Various zoom-in die shots using Cadence Encounter. Blue squares denote M1 TSV landing pads in the top die, and yellow squares denote Mtop TSV landing pads in the bottom die. Mtop TSV landing pads do not interfere with gates in the bottom die.

TABLE II
DESIGN AND OPTIMIZATION SUMMARY FOR KOZ SIZING

Design	Original	1um KOZ	1.25um KOZ	1.5um KOZ	1.75um KOZ	2um KOZ	2.5um KOZ	3.5um KOZ
TSV number	435	435	435	435	435	435	435	435
KOZ (μm)	0.7	1	1.25	1.5	1.75	2	2.5	3.5
Total TSV coupling capacitance (pF)	19.495	14.033	12.863	12.105	9.979	8.516	6.892	4.649
Footprint (μm^2)	2.067×10^5	2.16×10^5	2.25×10^5	2.33×10^5	2.42×10^5	2.52×10^5	2.71×10^5	3.13×10^5
Wire length (μm)	9.267×10^5	9.677×10^5	9.772×10^5	9.114×10^5	9.409×10^5	1.023×10^6	1.062×10^6	1.203×10^6
Total noise (V): nets>50mV	757.438	588.771	606.213	609.628	473.123	388.366	340.056	262.177
Total coupling-caused delay (ns): nets>10ps	317.137	290.277	219.905	222.281	185.294	147.158	124.896	80.044
Critical path delay (ns)	2.57	2.26	1.95	1.91	1.84	1.78	1.57	1.61
Total negative slack (ns)	725.809	238.272	157.787	63.736	45.089	37.842	3.387	5.290

performance. Using KOZ sizing, an extremely good SI and timing performance can be obtained, where total coupling noise is reduced by 55% and critical path delay is reduced by 39%. However, the total area has to be sacrificed by 31%. Therefore, the size of KOZ should be carefully chosen. On the other hand, by using placement refinement, we obtained a 32% total coupling-noise improvement and

TABLE III

DESIGN AND OPTIMIZATION SUMMARY FOR PLACEMENT REFINEMENT

Design	Original	iter1	iter5	iter10	iter15	iter20
TSV number	435	435	435	435	435	435
KOZ (μm)	0.7	0.7	0.7	0.7	0.7	0.7
Total TSV coupling capacitance (pF)	19.495	13.922	12.802	12.317	11.623	11.439
Footprint (μm^2)	2.067×10^5	2.067×10^5	2.067×10^5	2.067×10^5	2.067×10^5	2.067×10^5
Wire length (μm)	9.267×10^5	9.226×10^5	9.266×10^5	9.229×10^5	9.235×10^5	9.236×10^5
Total noise (V): nets>50mV	757.438	648.744	586.691	579.974	506.869	492.820
Total coupling caused delay (ns): nets>10ps	317.137	250.345	230.422	208.860	196.440	187.209
Critical path delay (ns)	2.57	2.42	2.50	2.44	2.30	2.32
Total negative slack (ns)	725.809	519.932	509.921	497.287	479.68	458.57

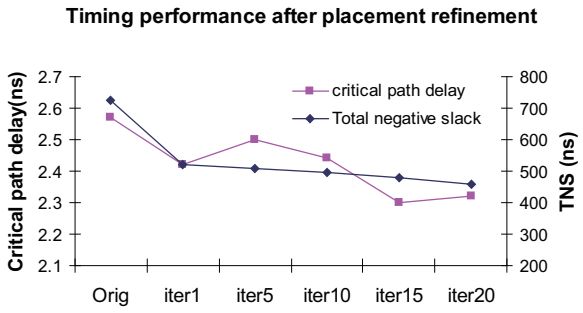

Fig. 20. Timing analysis results after every 5 iterations

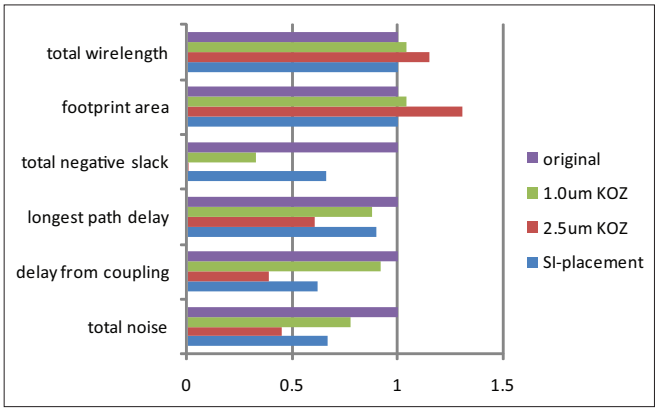

Fig. 21. Comparison of the original design and the three optimized designs

a 10% timing improvement without increasing the total area.

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