Novel Crack Sensor for TSV-based 3D Integrated Circuits: Design and Deployment Perspectives

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Abstract—The CTE mismatch-induced stress in 3D ICs may initiate cracks from the interface between a TSV and its dielectric liner, and propagates them on the silicon substrate surface. If a crack grows beyond the keep-out-zone (KOZ) of a TSV, it will jeopardize the reliability of the devices along its propagation path. While such threat can be eliminated by a sufficiently large KOZ, significant area overhead will be incurred. Given the low probability of crack occurrence, we argue that a much more economical approach is to keep KOZ small and filter out bad chips with cracks growing beyond the KOZ during testing. However, traditional microscope or X-ray diffraction based crack detection techniques are cost-prohibitive for massive productions. To address this issue, this paper proposes a novel crack sensor design with very little design or testing overhead. It is simply formed by doping the area surrounding a suspicious TSV. By measuring its DC resistances during testing, cracks that grow beyond the doped area can be easily detected. In addition, through empirical studies on crack dynamics in various TSV configurations, we provide deployment guidelines to minimize the number of sensors needed. To the best of our knowledge, this is the first work to propose a macro-scale crack detection technique.

Fig. 1. SEM image [3] of: (a) TSV; (b) zoom-in of the up-left corner of the TSV with radial crack

I. INTRODUCTION

Despite various advantages, TSV-based 3D ICs are subject to severe thermo-mechanical reliability hazards due to the coefficients of thermal expansion (CTE) mismatch between TSV and silicon substrate. Under normal operations, the 3D IC experiences heavy thermal cycles and thus induces large thermo-mechanical stress. Consequently, the stress may initiate micro cracks from the interface between a TSV and its dielectric liner, and further propagates them on the silicon substrate surface. Several studies have shown the existence of radial cracks adjacent to TSVs [13] [2] [3] due to thermo-mechanical stress. For example, Fig. 1(a) shows the scanning electron microscopy (SEM) image of a TSV [3], where a radial micro crack can be clearly observed by zooming in its up-left corner as shown in Fig. 1(b).

Not all cracks lead to troubles, but when a crack appears on the silicon substrate surface and reaches beyond the keep-out-zone (KOZ) of the originating TSV, it may jeopardize devices such as transistors along its propagation path and thus causing various circuit reliability issues [10]. For example, as will be shown in section II-A, if the surface crack cuts through the channel of a MOS transistor, it can degrade or even fail the entire transistor. In this paper, we define cracks on the silicon substrate surface that grow beyond the TSV KOZ as *critical cracks*.

To eliminate critical cracks, the simplest solution would be to make the KOZ of TSVs large enough to cover the maximal possible length any crack might grow. However, as will be shown in Sections II-B and III, the length a crack can grow from an originating TSV depends heavily on the locations of the nearby TSVs due to the superposition of thermo-mechanical stress, and its value can be large or even difficult to calculate when complicated TSV placement structures present. On the other hand, as the probability of crack initiation is low, it would be a waste of chip area to set the KOZ to
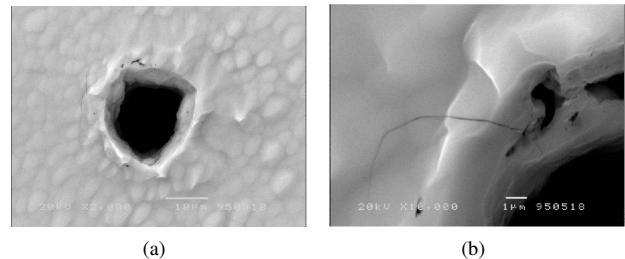
the extreme value for every TSV. Alternatively, it is more economical to make the TSV KOZ reasonably small and filter out those chips with critical cracks during testing. As will be shown in Section II-B, the saving of chip area from reduced KOZ can be huge: an estimation using 3D-MAPS processor [7] suggests that up to $8.0mm^2$ area can be saved, which is equivalent to that of 3.6M gates in $45nm$ technology.

One possible testing technique to indirectly detect critical cracks would be to check for various device and circuit level faults such as timing violations, stuck-at faults, etc. caused by the critical cracks. However, with limited testing coverage, large number of TSVs, and various possible crack propagation directions, conventional chip testing techniques may fail to identify every chip with critical cracks. In other words, a direct critical crack detection technique is imperative to guarantee shipping only critical-crack-free chips. An extra motivation to develop such a technique is to help silicon debugging and provide the necessary information for future technology improvement.

Although various studies have been carried out to model and simulate cracks in 3D ICs (e.g. [6]), their direct detection has primarily been based on the microscope [3] or X-ray diffraction [12]. Unfortunately, these techniques are too expensive to be employed for individual chip testing. The lack of efficient yet economical "macro-scale" solutions for crack detection has puzzled the 3D IC community for many years.

In this paper, we perform detailed studies on the TSV crack growth patterns under different TSV placement structures using finite element analysis (FEA). Based on that, we propose a novel crack sensor design using an extra doping surrounding each suspicious TSV. It is so simple that little overhead is induced at design time and a single DC measurement is required during testing for all TSVs being sensed. Yet, based on detailed device-level simulations, we show that it is very effective to detect critical cracks. Furthermore, general deployment guidelines are provided on where to place the sensors and how to decide the sizing of the doped area. To the best of our knowledge, this is the first work to propose a macro-scale crack detection technique based on in-depth studies of crack dynamics.
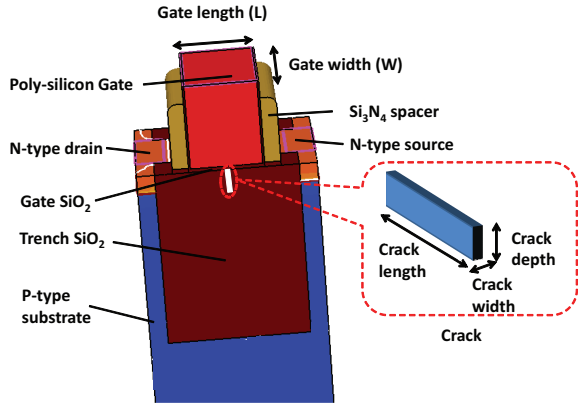
Fig. 2. NMOS transistor structure used in simulation

TABLE I. NMOS TRANSISTOR PARAMETERS USED IN SIMULATION

Parameter	Value
P-type substrate doping density	$1e17\ cm^{-3}$
N-type Poly-Si gate doping density	$1e20\ cm^{-3}$
N-type source/drain doping density	$1e19{\sim}1e17\ cm^{-3}$
Source/drain doping depth	$10\ nm$
Gate length (L)	$40\ nm$
Gate width (W)	$40\ nm$
Crack depth	$10\ nm$
Crack width	$1\ nm$
Crack length	$40\ nm$

II. FUNDAMENTAL MODELING

A. Impact of Crack on Transistors

As mentioned in Section I, critical cracks may grow beyond the TSV KOZ and reach nearby MOS transistors. When such crack appears on the silicon substrate surface and cuts through the channel (i.e., strong inversion layer) of a transistor, there will be less or even no conduction current flowing between the source and the drain even when the transistor is turned on. This is because the channel is usually shallow in advanced technologies (e.g., less than $10nm$). Consequently, the transistor tends to experience longer transition delays or to be entirely broken in the worst case.

To verify the negative impact of critical cracks on MOS transistors, we perform the device-level simulation using the Sentaurus technology CAD (TCAD) tool. Fig. 2 shows the detailed NMOS structure under study, with parameters illustrated in Table I following typical settings in $45nm$ technology [1][1]. The crack is modeled as a three-dimensional cuboid with properties of air, which cuts through the middle of the entire conduction channel underneath the gate to show its maximal impact.

Fig. 3(a) and 3(b) illustrate the simulated $I_D - V_{DS}$ curves at different gate voltages with and without cracks in the channel, respectively. Clearly, when the crack exists, the source/drain current I_D deteriorates severely and becomes five orders of magnitude smaller than the normal conduction current. Note that the current is not completely zero although the crack cuts off the channel, which is due to the combined effects of the tunneling current through the crack and the leakage current through the reverse-biased PN junction between source/drain and silicon substrate. Nonetheless, as the current is extremely small, the MOS transistor can be regarded as being in

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[1]The source/drain doping density decreases gradually from surface to $10nm$ deep following the Gaussian distribution.
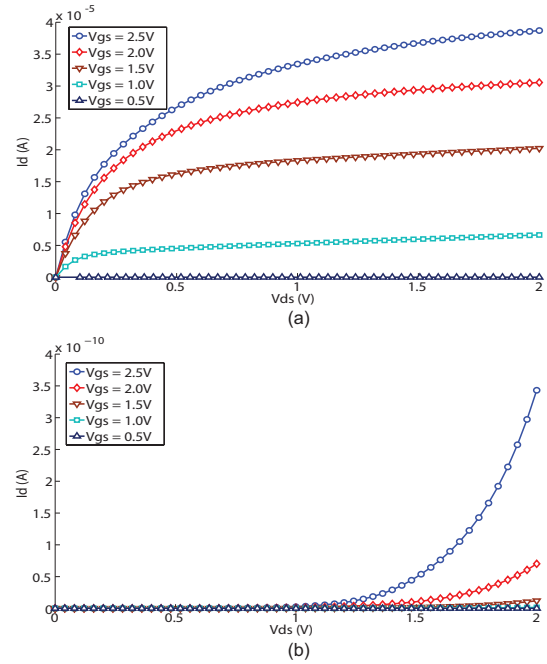

(a)

(b)

Fig. 3. Simulated $I_D - V_{DS}$ curve of NMOS transistor: (a) without crack in the channel; (b) with crack in the channel

TABLE II. I_D CHANGE WITH NMOS CONDUCTION CHANNEL CUT PARTIALLY BY THE CRACK

Crack length (nm)	$I_D\ (\mu A)$	Ratio
40 (100%)	1.81e-7	$0\times$
30 (75%)	2.98	$0.56\times$
20 (50%)	4.11	$0.78\times$
10 (25%)	4.92	$0.93\times$
0 (0%)	5.30	$1\times$

OFF status constantly regardless of the gate control voltage, which could lead to circuit malfunctioning.

In real situations, the critical crack may not always be long enough to completely cut through the channel of a transistor. Table II illustrates the corresponding simulation results when the NMOS transistor conduction channel is only partially cut by the critical crack, with $V_{GS} = V_{DS} = 1.0V$. Note the value in the parentheses of the first column is the percentage of channel that is cut by the crack in the channel width direction. Interestingly, the result shows that the I_D changes non-linearly with different crack lengths. In addition, even if only half of the channel is cut by the crack, there is still considerable I_D degradation (i.e., 22%) which will lead to increased transistor transition delay and cause potential timing violations.

Note that in the above studies we only considered cracks on the silicon substrate surface (i.e., surface crack) as active devices are fabricated there. Since the channel of a MOS transistor tends to be extremely shallow in advanced technologies, the cracks away from the silicon substrate surface will have negligible impact on transistor behavior.

To verify this, we perform the third group of Sentaurus simulations for the NMOS transistor with cracks underneath the silicon substrate surface as shown in Table III. The first column denotes the distance between the silicon substrate surface and the top surface of crack as shown in Fig. 4, i.e., zero distance means the crack reaches the surface of silicon substrate. Not surprisingly, even when the crack
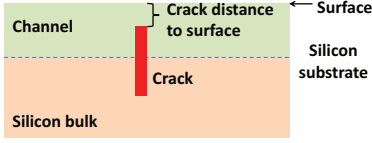
Fig. 4. Non-surface crack

TABLE III. IMPACT OF THE NON-SURFACE CRACK ON I_D

Crack distance to surface (nm)	I_D (μA)	Ratio
0	1.81e-7	$0\times$
1	5.03	$0.95\times$
2	5.19	$0.98\times$
3	5.24	$0.99\times$
no crack	5.30	$1\times$

is only $1nm$ underneath the silicon substrate surface, 95% of the channel conduction current is maintained compared to the crack-free case, which means the transistor can work almost normally. As such, we only consider surface cracks in the rest of this paper.

B. Impact of TSV Keep-Out-Zone

It might seem effective to simply set up a large enough TSV KOZ to eliminate all critical cracks. However, as will be shown in Section III with details, the maximal possible length a crack can grow from an originating TSV depends heavily on the nearby TSV placement patterns due to the superposition of stress. For example, Table IV shows that the maximal possible crack length becomes longer with the increased TSV array size (with constant TSV pitch of $10\mu m$). With heavy utilization of the vertical interconnections, larger TSV arrays are becoming popular (e.g. wide IO or for power/ground delivery) [7] [11], which leads to even larger TSV KOZ needed. In addition, it would be difficult to estimate the crack length in the case of non-uniform TSV placement structures. In other words, the TSV KOZ must leave additional margins in such situations. Consequently, if we only use TSV KOZ to eliminate cracks, significant chip area will be wasted because of the over estimation.

As the probability of crack occurrence is low, we believe it would be much more economical to make the TSV KOZ reasonably small and use crack sensors to filter out chips with critical cracks during testing. The saving of chip area can be huge: For example, the 3D-MAPS processor used 50K TSVs [7]. Assuming we reduce the radius of the KOZ[2] of each TSV from $7\mu m$ (safe for up to 5×5 TSV array) down to $4\mu m$ (safe only for single TSV), a total area of 8.0 mm^2 can be saved, equivalent to that of 3.6M gates in $45nm$ technology. Such analysis does not consider area overhead induced by techniques to detect cracks. However, as will be shown in Section IV, our novel sensors can be mostly embedded in the KOZ of TSVs and little area overhead is induced.

III. CRACK PROPAGATION MODELING

We observe that critical cracks can degrade transistor performance significantly in Section II. In this section, we examine the crack propagation behavior under different scenarios such as an isolated TSV and TSV array. Such structures are critical to guide crack sensor deployment with objectives of reducing the number of sensors needed given the KOZ size.

Before discussing detailed crack modeling, we introduce two terminologies: (1) **Victim TSV**: TSV with an initial crack. (2) **Aggressor TSV**: TSV located nearby a victim TSV and affecting crack growth of the victim TSV.

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[2]The KOZ radius is measured from the TSV/liner interface.

TABLE IV. IMPACT OF TSV ARRAY SIZE ON MAXIMAL POSSIBLE CRACK LENGTH

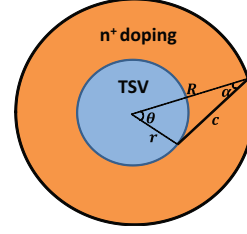| TSV array size	Crack length (μm)
1×1	4
3×3	5
5×5	7

Fig. 5. Top view of a crack (c) initiated from TSV/liner interface and reaching the n^+ doped region in arbitrary direction.

A. Energy Release Rate

Energy release rate (ERR) [5] is defined as the energy dissipated during fracture, i.e., crack, per newly created fracture surface area. In other words, ERR is the measure of the amount of energy available for fracture. The crack front will mostly likely grow in the direction with largest ERR. The crack will not grow when ERR is zero.

Since the loading in our simulation structure is solely due to thermal expansion from fabrication process with no work done by external loads, ERR can be determined as the rate of change in strain energy with crack extension [8]. In TSV-based 3D ICs, this strain energy is mostly generated from the thermo-mechanical stress induced by TSVs. Based on this, two 3D FEA models are created for strain energy analysis, one with a crack length of d, and another with a crack length of $d + \Delta d$. We obtain ERR for a crack using a forward difference approach as follows:

$$ERR = \frac{\partial U}{\partial A} = -\frac{U_{d+\Delta d} - U_d}{\Delta A} \tag{1}$$

where U is strain energy, A is area and ΔA is a newly created crack surface area.

B. Isolated TSV Case

The simplest case to start with is an isolated TSV. We would be interested to know how a crack will propagate in this case (in what direction and for how long). Such study will provide information on whether a crack sensor is needed given a particular KOZ radius.

We first study the direction of crack propagation, and show that a crack is most likely to grow along the radial direction, which justifies the settings in our motivation. Towards this, we need to prove that ERR attains maximum along the radial direction. It is known that ERR is related to the stress intensity factor K_I as

$$ERR = \frac{K_I{}^2}{E} \tag{2}$$

where E is the Young's modulus of material in which the crack propagates. So we only need to show that K_I attains maximum along the radial direction.

Consider the crack with given orientation as shown in Fig 5. The stress intensity factor K_I at the tip of the crack can be calculated as follows [9].

$$K_I = r^2 B \Delta\alpha\Delta T \sqrt{\frac{\pi c}{8Rr^3}} \cos(\frac{\alpha}{2} + \frac{3(\alpha + \theta)}{2}) \tag{3}$$

where r is the TSV radius, B is the Young's modulus of the silicon substrate, $\Delta\alpha$ is the CTE mismatch between TSV and silicon
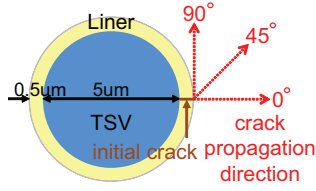
Fig. 6. Top view of a crack simulation structure of a single TSV with different crack propagation directions. Initial crack length is $0.5\mu m$ from TSV/liner interface.
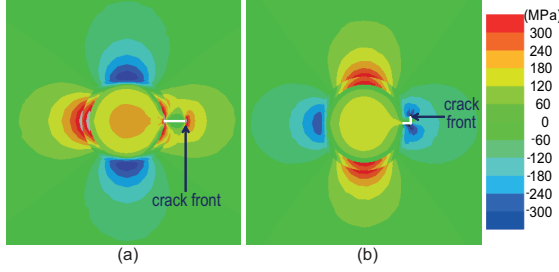

Fig. 7. Stress maps around a crack front in an isolated TSV. (a) σ_{yy} map with crack propagating with $0°$ angle. (b) σ_{xx} map with crack propagating with $90°$ angle.

substrate, ΔT is the thermal load, c is the crack length, θ is the angle spanned by the crack from the center, and R is the outer radius of the n^+ doped region. Applying trigonometry laws, we obtain

$$\frac{r}{\sin \alpha} = \frac{c}{\sin\theta} = \frac{\sqrt{r^2 + R^2 - 2rR\cos\theta}}{\sin\theta} \quad (4)$$

In addition,

$$\cos(\frac{\alpha}{2} + \frac{3(\alpha + \theta)}{2})$$
$$= (1 - 2\sin^2\alpha)\cos\frac{3\theta}{2} - 2\sin\alpha\cos\alpha\sin\frac{3\theta}{2} \quad (5)$$

Substituting (4) and (5) into (3), we obtain

$$K_I = \frac{\cos\frac{\theta}{2}(4a\beta^2\cos^2\frac{\theta}{2} - 3a\beta^2 - 2\beta + 1)}{(\beta^2 + 1 - 2\beta\cos\theta)^{3/4}\sqrt{\beta}} \quad (6)$$

where $a = \sqrt{r}B\Delta\alpha\Delta T\sqrt{\frac{\pi}{8}}$ and $\beta = R/r$. For $\theta \in [0, \arccos(\frac{r}{R})]$ (θ reaches maximum when the crack grows in the tangential direction of the TSV/liner interface circle) in (6), the denominator is increasing while the numerator is decreasing with the increase of θ. Thus, K_I monotonically decreases with θ, which leads to the following theorem.

Theorem 1: For an isolated TSV, the crack along the radial direction has maximal K_I and ERR, while the crack along the tangential direction has minimal K_I and ERR.

Since the crack tends to grow in the direction with maximal ERR, we have the following corollary.

Corollary 1: For an isolated TSV, the crack grows and propagates along the TSV radial direction.

To validate Theorem 1, we build FEA simulation structures as shown in Fig. 6. Our TSV diameter, height, and dielectric liner thickness are $5\mu m$, $30\mu m$, and $0.5\mu m$, respectively. Material properties used for our experiments are as follows: CTE (ppm/K) / Young's modulus (GPa) for Cu = (17/110), Si = (2.3/130), and SiO_2 = (0.5/71). We use the FEA simulation tool ABAQUS to perform simulations, and all materials are assumed to be linear elastic and isotropic [4]. The entire structure undergoes $\Delta T = +250°C$ of thermal load (Cu
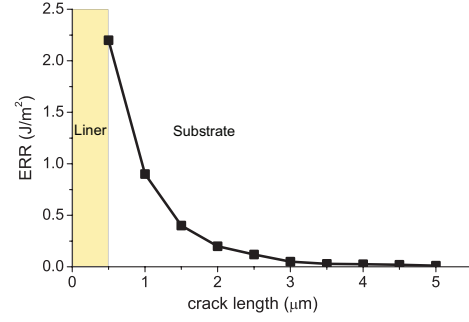

Fig. 8. ERR of the crack propagating along the radial direction of a single TSV.

electroplating $25°C \rightarrow$ annealing $275°C$) to represent a fabrication process.

The initial crack length and depth is assumed to be $0.5\mu m$ and $10nm$, respectively, and this crack spans from the TSV/liner interface to the liner/substrate interface. Then, we simulate three cases to examine in which direction this crack will further grow as shown in Fig. 6. ERR values from FEA simulations for these three cases are as follows: ERR (J/m^2) for $0°$ (radial direction): 2.2, $45°$: 0.6, and $90°$ (tangential direction): 0.4. This clearly shows that the crack will grow in the radial direction.

This preferred crack propagation direction, i.e., radial direction, can be explained with stress maps shown in Fig. 7. For the crack to grow further, tensile stress needs to be applied perpendicular to the plane of the crack. With a positive thermal load ($\Delta T = +250°C$), Cu TSV expands more than silicon substrate, and hence generates compressive stress along the radial direction from the TSV center.[3] On the other hand, tensile stress builds up along the tangential direction around the TSV.

Thus, in the σ_{yy} map (Fig. 7(a)), the tensile stress (red color) in the y-direction (tangential direction) opens the crack front that propagates in the radial direction ($0°$). On the other hand, when the crack propagates in the tangential direction ($90°$), the compressive stress (blue color) in x-direction (radial direction) closes the crack as shown in σ_{xx} map (Fig. 7(b)).

Now that we know the crack always grow in the radial direction, the next question is the maximum length it can grow. Fig. 8 shows that ERR monotonically decreases as the crack grows. This is because stress magnitude decreases rapidly as the crack front moves away from the TSV, and hence the strain energy available for crack growth becomes smaller. Beyond $4\mu m$ away from the TSV/liner edge, the ERR is almost zero, and hence the maximum length of the crack is around $4\mu m$.

C. Single-Aggressor Case

In this section, we further investigate the crack growth behavior in the existence of a single aggressor TSV. Especially, we study the impact of the TSV pitch (center-to-center distance) and location of the aggressor TSV with respect to the victim TSV. Fig. 9 shows the simulation structure. We grow the crack along the x-direction (radial direction) and obtain ERR values from FEA simulations. We first place the aggressor with $10\mu m$ pitch and then moves it away from the victim TSV up to $20\mu m$ pitch with a $2.5\mu m$ step. Fig. 10 shows that as the crack propagates along the x-direction, the impact

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[3]With a negative thermal load (annealing $275°C \rightarrow$ room temperature $25°C$), tensile stress builds up around a TSV along the radial direction.
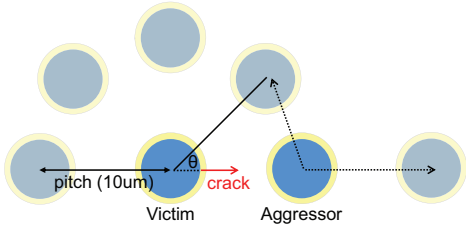
Fig. 9. Simulation structure with one aggressor TSV. A crack grows along the x-direction (radial direction). The aggressor TSV either rotates around a victim TSV or moves away from the victim TSV.
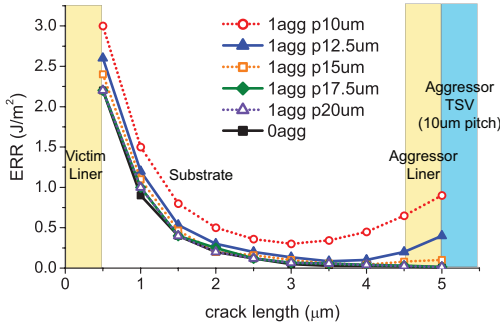

Fig. 10. ERR of the crack of a victim TSV with one aggressor at different pitches. Initial crack is $0.5\mu m$ (from victim TSV/liner interface to liner/substrate interface). Crack length is swept from the initial crack up to the TSV/liner interface of the aggressor with $10\mu m$ pitch.

of an aggressor TSV with a pitch greater than $15\mu m$ on the victim TSV crack's ERR is almost negligible (same as the case without an aggressor).

However, interestingly when the TSV pitch is small enough such as below $12.5\mu m$, ERR values first drop as expected, and then start to increase as the crack front becomes close to the aggressor location. This is because the higher stress from the aggressor TSV creates higher strain energy for the crack to grow further. Thus, it is possible that a crack can create a bridge between two TSVs (bridge crack). As the copper atoms may easily migrate along the cracks, the bridge may create short-circuit issues.

Now we rotate the aggressor at $10\mu m$ pitch around the victim TSV with a $45°$ angle step. We see that ERR is highest when the aggressor TSV is on the crack propagation direction ($0°$) as shown in Fig. 11. This is because the constructive stress interference between the victim and aggressor TSVs that generates higher tensile stress perpendicular to the crack propagation direction. Similar constructive stress occurs with an aggressor TSV at $135°$ and $180°$, but that impact is much smaller than the $0°$ case because the distance between the crack front and the aggressor TSV is much longer and hence stress magnitude is lower. On the other hand, when the aggressor TSV is at $45°$ and $90°$ (acute angle), ERR values are lower than the other cases. In short, in the single aggressor case, the crack will either bridge the victim and aggressor TSV, or the crack will stop growing at certain distance similar to the single-TSV case, depending on the initial crack direction.

D. Two-Aggressor Case

We now examine the crack propagation direction when two aggressor TSVs exist as shown in Fig. 12. If a crack can propagate in between aggressor TSVs, it is possible that this crack break the entire chip in the worst case. However, as shown in Fig. 12(b), compressive
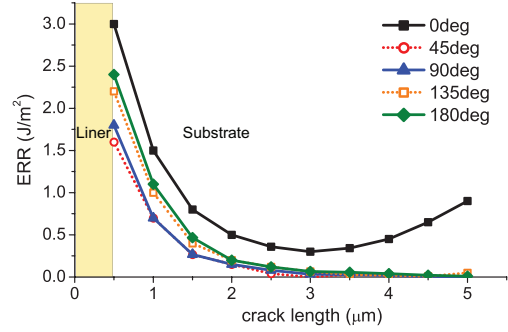

Fig. 11. ERR of the crack of a victim TSV with one aggressor at different angles. TSV pitch is $10\mu m$ for all cases.
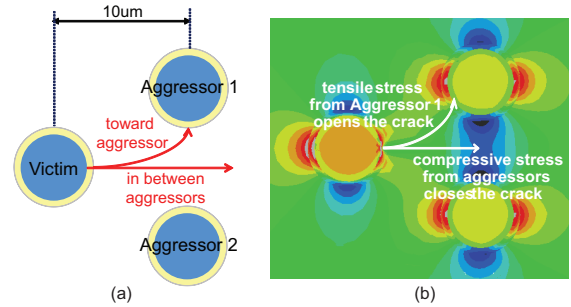

Fig. 12. Crack propagation with two aggressor TSVs. (a) Simulation structure to examine if the crack propagates toward one aggressor or in between aggressors. (b) σ_{yy} map of (a).

stress from aggressor TSVs close the crack, and ERR of $0 J/m^2$ is observed in FEA simulations. Thus, the scenario that a crack propagates across a chip is unlikely to happen. On the other hand, when the crack propagates towards one aggressor TSV, the tensile stress along the tangential direction around an aggressor TSV helps open the crack further (non-zero ERR). Therefore, we can infer from these simulations that a crack will grow towards the aggressor TSV rather than propagating in between TSVs, and as such, the radial direction is no longer always the most likely one.

E. TSV-Array Case

Up to this point, we have examined the crack growth behavior with up to two aggressor TSVs. In this section, we study the crack propagation in a general TSV array. We monitor ERR values of the crack of the victim TSV in three distinctive locations in a 5×5 TSV array as shown in Fig. 13: center, side, and corner locations. The pitch is still set as $10\mu m$. It can be easily inferred from stress maps that ERR values of cracks from any TSV other than these three locations will take intermediate values compared with these three cases. Since we observed that a crack growing toward an aggressor TSV has higher ERR in Section III-B, the crack propagation direction is assumed to be upward, downward, left, or right from the victim TSV to show the worst case. All these directions are radial direction from the victim TSV.

In addition, thanks to the symmetry in the array structure, we only need to monitor six cases. For example, as for the victim TSV in the center, ERR values for up, down, left, and right crack propagation directions are identical. Thus, we only monitor a crack that propagates to the left (ctr_L). As for the side location we monitor upward (side_U), left (side_L), and right (side_R) directions, and for
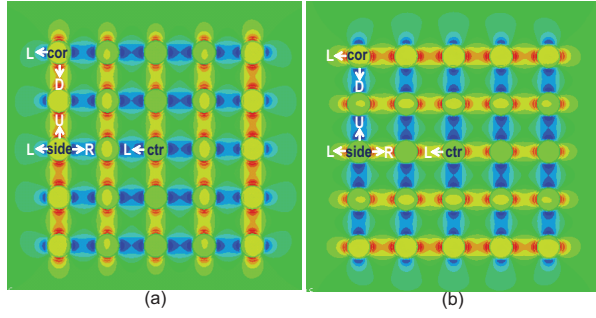
Fig. 13. Stress maps of a 5×5 TSV array. (a) σ_{xx} map. (b) σ_{yy} map.
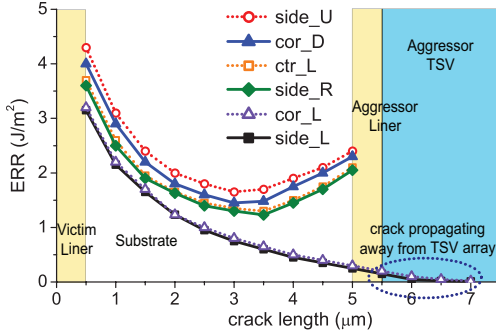

Fig. 14. ERR of the crack of a victim TSV in different locations of a 5×5 TSV array. side_L and ctr_L overlap. Naming convention: e.g., ctr_L = a crack propagates towards left from the victim TSV in the center of a TSV array.
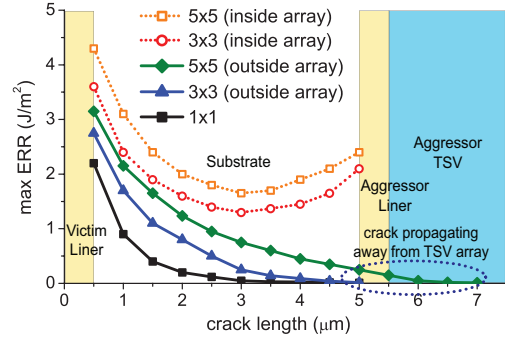

Fig. 15. Maximum ERR in different TSV array sizes. Inside array: a crack propagates inside a TSV array. Outside array: a crack propagates away from a TSV array.
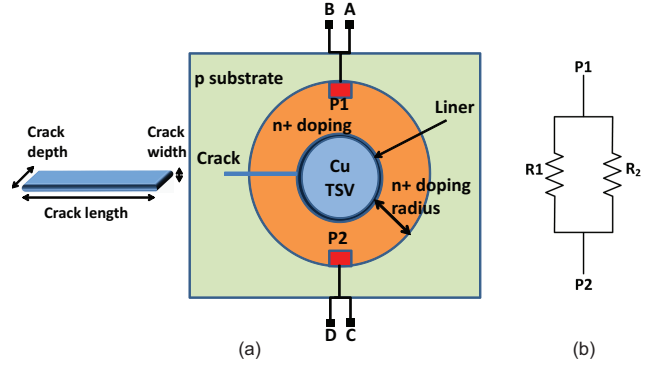

Fig. 16. Crack sensor: (a) top-view sensor structure; (b) equivalent circuit

the corner we track left (cor_L) and downward (cor_D) directions.

ERR curves for these six cases are shown in Fig. 14. Interestingly, the ERR is highest in the side_U case. As shown in Fig. 13(a), tensile stress in σ_{xx} map is highest around the side location along the upward and downward directions. Thus, this high tensile stress helps the crack to propagate in the upward direction. Although the victim TSV in the center is surrounded by more aggressor TSVs, the stress magnitude is lower than other locations because of the destructive stress interference between TSVs in vertical and horizontal directions. In all the cases, once a crack initiates from one TSV it is highly likely to grow and reach a neighbouring TSV. From this perspective, it is only necessary to place crack sensors every other TSV in a diamond pattern. On the other hand, for the crack growing away from the TSV array such as side_L and cor_L, the ERR decreases monotonically similar to the case without an aggressor, but decays much slower. If the KOZ of the TSVs is smaller than $7\mu m$, it is also necessary to place crack sensors on all the side and corner TSVs.

We also study the impact of TSV array size on the crack propagation: 1×1, 3×3, and 5×5 TSV arrays. We monitor maximum ERR values of these three cases for the crack that grows inside TSV array (side_U) as well as away from the array (cor_L). As Fig. 15 shows, larger TSV array generates higher ERR values. The conclusion here is that larger TSV array has higher probability of generating bridge cracks between two TSVs when they are growing inside the array, or cracks of longer length when they are growing away from the array. As such, it is more important to place sensors for larger arrays.

IV. CRACK SENSOR DESIGN AND VERIFICATION

While the crack growth patterns have been studied, it remains an open question on how a critical crack (i.e., the crack on the silicon substrate

surface that grows beyond the TSV KOZ) can be detected. The traditional microscope [3] or X-ray diffraction [12] based detection are too expensive to be employed for individual chip testing. In this section, we propose a novel crack sensor design that can easily detect critical cracks directly with very low area overhead.

A. Sensor Structure

Fig. 16(a) shows the top view of the proposed crack sensor design as well as the dimension definitions for the crack. Specifically, assuming the silicon substrate is p-type, the sensor is composed of a circular n^+ doped area surrounding a suspicious TSV and two Ohmic contacts, $P1$ and $P2$ symmetrically located at the boundary of the n^+ doped region. Note the n^+ doping radius is measured from the TSV liner instead of the TSV center. Four nodes A, B, C and D, two from each contacts, are wired out for measurement (details to be explained later). The actual fabrication is done by first doping the solid round area before etching the TSV.

The sensor's working mechanism can be explained using the equivalent circuit shown in Fig. 16(b), where R_1 and R_2 model the left- and right-hand-side resistance in the n^+ doped region, respectively. Note that it is not possible to conduct through any path in the substrate (i.e., $n^+ \rightarrow p \rightarrow n^+$), because any such path will encounter two diodes connected back-to-back. Also, we do not include the contact resistance in the model since it is common knowledge that such resistance is orders of magnitude smaller than the doped area resistance (R_1 and R_2). Denote the current and voltage between $P1$ and $P2$ as I and V, we have

$$V = \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot I$$

TABLE V. VOLTAGE CHANGE WITH MULTIPLE CRACKS

Crack locations	Left	right	Left and right
ΔV from nominal value	2×	2×	∞

TABLE VI. CRACK SENSOR PARAMETERS USED IN SIMULATION

Parameter	Value
Cu TSV diameter	5 (μm)
SiO$_2$ liner thickness	0.5 (μm)
N$^+$ doped region radius	5 (μm)
N$^+$ doped region depth	10 (nm)
N$^+$ doping density	1e19 (cm^{-3})
P-type substrate doping density	1e17 (cm^{-3})

In the crack-free situation, we have $R_1 = R_2 = R$ with R being small due to the existence of the highly conductive n^+ doped circle. In this case, $V = 0.5IR$, which we define as the nominal value. When a crack as shown in Fig. 16(a) with depth larger than that of the n^+ doped region (5-10nm with ultra shallow injection [1]) occurs and completely cuts through the doped area, the conduction path is broken - note that it is impossible to conduct through any path in the p-type substrate. Accordingly, $R_1 \to \infty$, which leads to $V = IR$, or 2× larger than the nominal value.

Practically, five issues need to be considered: 1) To measure the voltage V across $P1$ and $P2$, any metal wires used to connect the contacts have significant parasitic resistance, which will affect the measured resistance. 2) Our sensor should still work even if multiple critical cracks originates from the same TSV. 3) Due to process variation, the resistance will deviate from the design values. We need to make sure that the voltage change induced by a crack is much larger than that from process variation. 4) We need to minimize the number of external pads needed for measurement for massive TSVs and 5) We need to make sure that the crack we have detected is a critical one, i.e., the surface crack growing beyond the TSV KOZ that can potentially affect nearby transistors.

For the first issue, we can address it through the classical four-point Kelvin measurement (this is also the reason why we need four nodes A, B, C and D). By injecting current I through A and C and measuring the voltage V across B and D, we are able to exclude any impact from the wires. In addition, since the resistances of the contacts $P1$ and $P2$ are smaller than those of $R1$ and $R2$, they do not affect the final measurement results. For the second issue, some simple analysis leads us to the result listed in Table V when multiple cracks occur in different regions. When the crack appears in either left- or right-hand-side of the n^+ doped region, V becomes 2× larger compared to the nominal value. When cracks appear in both left and right hand side, we have $R_1 \to \infty$ and $R_2 \to \infty$, which leads to $V \to \infty$ (a very large value).

For the third issue, we perform quick estimation to see how much impact process variation can have on V. Assuming a maximal of 20% variation on R_1 and R_2, it is easy to see that V can increase up to $0.6IR$, i.e., 1.2× increase from the nominal value. As shown in Table V, in all cases the voltage change is much more significant than what could be potentially caused by process variation. It is thus clear that our sensor can still work properly in the presence of multiple cracks.

For the fourth issue, since many suspicious TSVs exist on chip, using four I/O pads for each TSV is impossible. Accordingly, we propose the testing structure by connecting A and C of each crack sensor to an adjacent Wilson current mirror, which uses an on-chip reference current shared by all TSVs. In addition, B and D are connected to an adjacent voltage comparator with a reference voltage of 1.5× of the nominal value, which can come from on-chip DC-DC converter or external power pad. The output of these voltage comparators are connected together using logic OR to generate a final Boolean signal to an output pad, which can then be measured to tell if there is any critical crack at any TSV. As such, at most two pads are needed to cover all TSVs.

For the last issue, assuming that dramatic resistance change will only occur for cracks that grow beyond the doped area and are deeper than the doping depth, we can set the n^+ doping depth the same as

the depth of the typical MOS transistor channel (less than 10nm that can be achieved through ultra shallow injection). This guarantees only cracks really affecting the MOS transistors will be detected. In addition, we design the radius of the n^+ doping region the same as the KOZ of TSVs. As such, only critical cracks (i.e., those grow beyond the TSV KOZ) will cause dramatic resistance change by entirely cutting through half of the conduction path in n^+ doped region, which will thus be observed by the crack sensor. The assumption will be verified in Section IV-B.

Finally, we would like to point out that since the doped area is set to be the same as the KOZ, it will not incur any area overhead. The only area overhead comes from the voltage comparator, the current source, and the associated interconnects, which is relatively small.

B. Verification Results

To verify the proposed sensor design, we set up the crack sensor structure shown in Fig. 16(a) and perform Sentaurus simulations with parameters listed in Table VI. The conduction current is defined as the current $I_{P_1 P_2}$ through $P1$ and $P2$ by applying $V_{P1} = 2.0V$ and $V_{P2} = 0.0V$.

We first study the impact of different crack widths (see Fig. 16(a) for definition) on conduction current when the crack fully cuts through the n^+ doped region (i.e., with crack length 5μm and crack depth of 10nm). This experiment is to verify the impact of potential tunneling current through the crack. However, the results indicate that even the crack width is down to 0.1nm (i.e., one angstrom), the tunneling current observed is still four orders of magnitude smaller than the normal conduction current in the crack-free case. As such, we conclude that the tunneling current due to small crack width will have negligible impact on the crack sensing results. In the following simulations, we set crack width as 1nm constantly.

Fig. 17 demonstrates the impact of different crack lengths (see Fig. 16(a) for definition) on the conduction current $I_{P_1 P_2}$ and the corresponding change in resistance $R_{P_1 P_2}$, where the crack depth is set to be 10nm (i.e., spans the entire n^+ doped region in the vertical direction). We observe a sharp decrease (increase) in $I_{P_1 P_2}$ ($R_{P_1 P_2}$) only when the crack reaches the boundary of the n^+ doped region (i.e., it starts to become a critical crack). This is actually desirable, since by designing the n^+ doped region radius, the designer can customize the length of the crack to be detected, i.e., cracks with length smaller than the n^+ doped region radius will not cause enough change in resistance and will thus not be observed. **For our application, we will set it equal to the radius of the KOZ**. The 2X resistance change in the case of critical crack also matches well with the theoretical analysis shown in Table V, as the contact resistance is much smaller than that of the n^+ doped area.

Similarly, Fig. 18 shows the impact of different crack depths on the $I_{P_1 P_2}$ and $R_{P_1 P_2}$, where the crack length is set to be 5um (i.e., spans the entire n^+ doped region in the radial direction). We also observe a sharp decrease (increase) in $I_{P_1 P_2}$ ($R_{P_1 P_2}$) only when the crack has a depth close to that of the n^+ doped region. This is desirable as designers are able to customize the depth of the crack they would like to detect by simply controlling the depth of the n^+
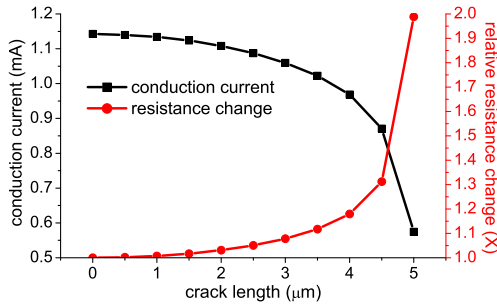
377

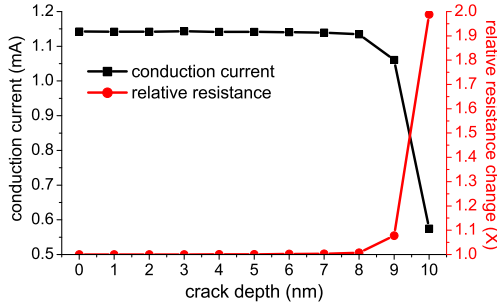Fig. 17.   Impact of crack length on crack sensing result

Fig. 18.   Impact of crack depth on crack sensing result

doped region. **For our application, we will set it equal to the depth of the channel of the transistors.**

V.   CRACK SENSOR DEPLOYMENT GUIDELINES

To guide the crack sensor deployment, we first summarize our crack propagation modeling results from Section III as follows. All the numbers are based on our TSV geometries[4].

1) In the case of an isolated TSV, a crack would most likely grow along the radial direction, and stops at a maximum length of around $4\mu m$.

2) Any aggressor TSV that is more than $15\mu m$ away from the victim TSV has no impact on the crack growth.

3) The aggressor TSV on the crack propagation direction has the maximum impact on further growing the crack. In addition, a crack tends to terminate at a nearby aggressor TSV (bridge crack) rather than propagate in between aggressors.

4) In TSV arrays, once a crack is initiated from one TSV, it is highly likely to bridge a neighbouring TSV if its direction is inside the array, or to grow much longer than in the isolated TSV case if its direction is away from the array. The likelihood of a bridge crack inside the array or the maximum length of the crack growing away from the array increases with the array size. As such, TSVs in larger arrays need larger KOZ.

Based on the above results and the proposed crack sensor design, we provide the following deployment guidelines to reduce the number of crack sensors needed.

1) For an isolated TSV, since a crack may not grow beyond $4\mu m$, if the TSV KOZ is more than $4\mu m$, there is no need to deploy a sensor. Otherwise, we put a sensor with doped radius equal to the actual KOZ size.

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[4]It can be anticipated that similar conclusions can be obtained from different TSV geometries although the numbers may be different.

2) The existence of an aggressor TSV can help the crack propagate if it is in the direction of crack propagation and is within $12.5\mu m$ from the originating TSV. In this case, a bridge crack is most likely to occur. If the TSV KOZ is less than $6.25\mu m$, we only need to deploy a single sensor (either for the aggressor TSV or for the victim TSV), with doped radius equal to the KOZ size.

3) In a TSV array, if the maximum crack length exceeds the KOZ size, sensors need to be deployed in a diamond pattern (one every other TSV) inside the array, and for all the side and corner TSVs. Sensors are more important for larger arrays.

VI.   CONCLUSIONS AND DISCUSSIONS

In this paper, detailed studies on the crack propagation patterns under different scenarios are performed. In addition, we propose and verify through device-level simulations the concept of a novel low-cost on-chip crack sensor design for critical crack detection. Based on these results, we provide general crack sensor deployment guidelines considering local TSV placement structures. Many interesting questions can be inspired from it. For example, 1) What if we use other shape (e.g. rectangular) to implement the doped area? 2) What if we use more than two contacts in the doped area? 3) How to alter the sensor to detect interfacial delamination, another major type of crack in 3D ICs? We hope that our idea presented here shall point out a new research direction in the on-chip crack sensor designs for 3D ICs.

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