Enabling 3D Integration Through Optimal Topography

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Abstract— In a 3D stacked IC, *through-silicon vias* (TSVs) are utilized to interconnect dies vertically. In one common TSV practice, via-first TSVs directly connect the first metal layer of a die and the top metal layer of the die above it. However, the landing pads on the first metal layer, due to their large area and presence of features with widely varying sizes, may result in serious topographic errors after chemical-mechanical polishing. These errors result in cumulative effects in up interconnect layer processing steps, thereby causing yield and performance problems. In this paper, we analyze the impact of TSV landing pads on topography and present a technique to minimize it. We first show that traditional fill methodology is inefficient due to large metal density variations. After selecting best fill possible through conducting *design of experiments* (DOEs), we run CMP simulations on another DOE to find the impact of TSV to TSV pitch on final topography. Finding a minimum pitch from this experiment, we apply force-directed TSV separation during placement. We achieve $24\% \sim 36\%$ improvement in topography variation with only $0.5\% \sim 2.0\%$ wirelength increase. The improvements presented herein will enable manufacturability of 3D circuits with reduced topographic variations.

I. Introduction

Recently, *three-dimensional integrated circuits* (3D ICs) have emerged as a promising candidate to improve die-to-die latency of 2D (traditional) ICs. In a 3D IC, the dies are stacked vertically and connected with *through-silicon vias* (TSVs) as shown in Figure 1. Therefore, for the same logic design, the footprint area of a 3D IC implementation is smaller than a 2D IC. Several recent works ([1] and [2]) have shown that smaller footprint area of a 3D IC leads to shorter total wirelength, which in turn leads to better chip performance [3].

3D IC is enabled by the fabrication of TSVs and die-to-die bonding. In a via-first TSV process, TSVs are etched through the silicon and filled with copper or tungsten. The topmost interconnect layer of one die is connected to the *lowest interconnect layer* ($M1$) of another die. TSV landing pads are used in $M1$ and $Mtop$ layers to make the connection. TSV landing pads are laid out in the standard routing metal layer, hence a direct connection to the metal wires and eventually to transistors is possible.

TSV landing pads are designed to be larger than TSVs to prevent overlay error [4]. In practice, a TSV landing pad can be many times wider than the minimum $M1$ feature size. For example, a typical TSV diameter in demonstration is about 3 to $5\mu m$, whereas the minimum $M1$ wire width is $65nm$ in $45nm$ technology. Such a wide range of metal features increases the feature density mismatch significantly, thereby resulting in topographic non-uniformities and large density gradients due to *chemical-mechanical polishing* (CMP) which is highly dependent on the underlying metal feature density [5], [6].

Fill synthesis has been widely used as a post-route process to achieve the uniform feature density and also to meet the target feature
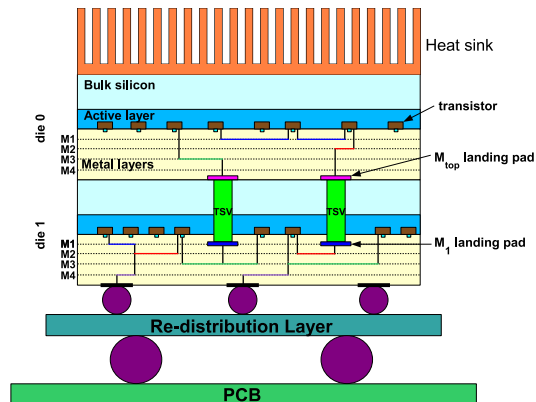
Fig. 1. Via-first TSVs and face-to-back bonding in 3D ICs (side-view). Rectangles (metals) that are attached to the TSVs are TSV landing pads.

density [7]–[9], [11]. During fill synthesis, floating or grounded metal fills are inserted into layouts so that the feature density in any layout window satisfies the feature density constraints.

When a layer contains widely varying feature sizes and metal densities, however, dummy fill insertion alone cannot mitigate the topography variation entirely. Moreover, the cumulative effect of the topographic variations for the rest of the eight to twelve interconnect layers signifies the importance of perfect uniformity at the lowest interconnect layer [10]. In this paper we study the impact of TSV landing pads on topography variation, and propose techniques to help minimize the topography variation.

II. Finding Optimal Fill Pattern

Accurate estimation of post-CMP topography requires a time-consuming full-chip CMP simulation because simple mathematical CMP models are inaccurate or simply not available [13]. In addition, $M1$ feature densities and patterns of 3D ICs are very different from those of 2D ICs. Consequently, it is hard to find the optimal fill pattern for each window when TSVs exist in the layout. Therefore, we conduct a DOE similar to the DOE shown in [12] to find the optimal fill pattern to minimize the topography variation in 3D ICs. We target selecting a topography-optimal fill using traditional fill methodology. For CMP simulation, we use *Calibre CMPAnalyzer* [15] with $45nm$ CMP model provided by *Mentor Graphics*. The parameters and assumptions used for device process and TSVs are shown in Table I.

In this DOE, we create a three-pass fill insertion algorithm, which starts from the largest fill pattern to the smallest fill pattern based on the fill practice in industry [17]. Figure 2 shows an example of three-pass filling, where W_i and L_i are the fill pattern width and length of i-th pass filling respectively. In each experiment, we choose a fill pattern with the following four parameters: (1) Fill pattern width, (2)

Parameter (Assumption)	Value
TSV shape	square
TSV type	via-first
Die bonding	face-to-back
TSV width	$6.0um$
TSV landing pad width	$10.0\mu m$
TSV-to-device keep-off distance	$3.175\mu m$
TSV-to-TSV keep-off distance	$6.35\mu m$
Device technology	NCSU $45nm$
M1 min. width	$65nm$
M1 min. pitch	$120nm$
M1 thickness	$130nm$
Max. tolerance of M1 thickness variation [16]	$13nm$

TABLE II

DOE TO FIND THE OPTIMAL THREE-PASS FILL PATTERN. VAR: AVERAGE
OF THE METAL HEIGHT GRADIENT.

Fill Style				Topography(Å)			
AR	ST	W_3	WR	MAX	MIN	MAX-MIN	VAR
2	0.2	2×	{1:3:5}	1533.37	1463.60	69.77	5.72
			{1:5:10}	1532.58	1463.16	69.42	5.65
		4×	{1:3:5}	1500.04	1427.31	72.73	6.35
			{1:5:10}	1500.44	1427.43	73.01	6.36
	0.4	2×	{1:3:5}	1527.15	1456.25	70.90	5.75
			{1:5:10}	**1527.94**	**1458.61**	**69.33**	**5.59**
		4×	{1:3:5}	1497.86	1424.87	72.99	6.20
			{1:5:10}	1497.94	1424.96	72.98	6.21
4	0.2	2×	{1:3:5}	1528.39	1457.24	71.15	5.89
			{1:5:10}	1527.88	1457.09	70.79	5.86
		4×	{1:3:5}	1495.35	1420.81	74.54	6.20
			{1:5:10}	1495.64	1421.05	74.59	6.20
	0.4	2×	{1:3:5}	1525.25	1453.72	71.53	5.78
			{1:5:10}	1524.74	1453.59	71.15	5.75
		4×	{1:3:5}	1494.04	1418.68	75.36	6.04
			{1:5:10}	1494.18	1418.84	75.34	6.04

Aspect ratio (AR) = L_i/W_i, (3) Width ratio (WR) = W_{i+2}:W_{i+1}:W_i, (4) Stagger amount.

Fill pattern width is defined as the width used in the third pass filling, i.e., W_3 in Figure 2. We also apply staggering in the x and y directions as offsets between the previous and the current fill patterns. In Figure 2, the two first-pass fills have y-direction staggering, while the two second-pass fills have x-direction staggering. In this experiment, we use both x- and y-direction staggering. The target feature density is 60% and we regulate the spacing between two fill patterns to meet the target density. The set of fill parameters we use in this DOE is listed as:

- **Fill pattern width:** 2× or 4× the minimum $M1$ width
- **AR:** 2 or 4
- **WR:** {1:3:5} or {1:5:10}
- **Staggering:** 0.2× or 0.4× fill pattern width

Table II shows the CMP simulation results of this DOE set. Based on the simulation results, we choose the following parameters: (1) fill pattern width = 2× the minimum $M1$ width, (2) AR = 2, (3) WR = 1:5:10, and (4) staggering = 0.4× fill pattern width, to perform the fill synthesis. Figure 2 shows a layout example after our three-pass fill insertion algorithm is applied.

III. DOEs FOR CMP-FRIENDLY 3D IC LAYOUTS

CMP is a complicated process and there is no accurate simple way for quick estimation of post-CMP final topography. Moreover, the big effective length of CMP process (e.g. $200\mu m$) makes it even harder to predict the final topography when TSVs are spread out over the entire layout. In this section, therefore, we generate many test layouts having TSVs, run CMP simulation on them, and find out
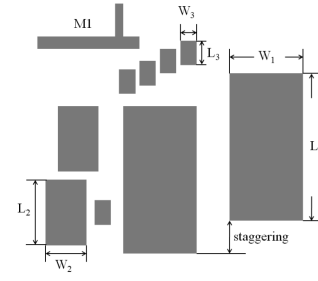

Fig. 2. Multi-pass fill insertion. We insert fills of size $W_1 \times L_1$ in the first pass, fills of size $W_2 \times L_2$ in the second pass, and fills of size $W_3 \times L_3$ in the third pass.

general trends of CMP-friendly 3D IC layouts. We use the optimal fill algorithm from previous section, and see whether TSV placement would have an impact on topography that traditional fill cannot fix.

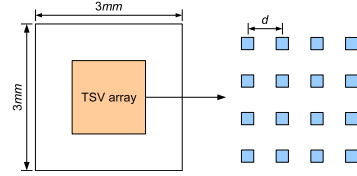### A. TSV Arrays without Standard Cells (DOE1)

Fig. 3. Left: DOE1 test layout floorplan. Right: TSV array and the definition of d.

As fill synthesis has been widely used to achieve uniform feature density in 2D ICs, we place TSVs only in this DOE and insert metal fills to see if fill alone can fix topography. The reason we place TSVs only is because having no obstacles (local $M1$ wires inside standard cells) in between TSVs can give the highest degree of freedom to the fill synthesizer. Figure 3 shows the TSV structure for this DOE study. There are 100 (or 400) TSVs forming a 10×10 (or 20×20) array, and the distance between two adjacent TSVs is d. Two variables exist in this DOE; d and the target metal density for fill synthesis. Changing d shows the impact of densely-placed or sparsely-placed TSVs on final topography while changing the metal density shows the optimal density for better final topography. Table III shows the full range of d and the target metal density.

Table IV shows the final topography when the metal density changes from 30% to 60% and the TSV-to-TSV distance changes from $12\mu m$ to $42\mu m$. As the table shows, layouts in which TSVs are placed densely have higher topography range (MAX-MIN) and also higher topography variation (STD). For example, the topography range and variation of a layout whose metal density is 40% and TSV-to-TSV distance is $12\mu m$ are respectively 62.85Å and 3.90Å when the TSV count is 400. However, when the TSV-to-TSV distance is $22\mu m$, the topography range becomes 16.72Å and the topography variation becomes 1.10Å. In addition, higher metal density has lower topography ranges and variations as expected. As the metal density increases and the TSV-to-TSV distance increases, the topography range and variation decreases. Therefore, we can conclude that TSVs need to be placed sparsely for a CMP-friendly 3D IC design when the TSVs are not surrounded by standard cells.

B. TSV Arrays with Standard Cells (DOE2)

In this DOE study, we investigate the relationship between the placement pattern of TSVs and its CMP simulation results when

TABLE IV

DOE1: FINAL TOPOGRAPHY (Å) WHEN THE METAL DENSITY AND THE TSV-TO-TSV DISTANCE CHANGE.

		Metal density							
		30%		40%		50%		60%	
	Distance (μm)	MAX − MIN	STD	MAX − MIN	STD	MAX − MIN	STD	MAX − MIN	STD
# TSVs = 100	12	63.90	2.17	49.65	1.69	36.04	1.15	22.69	0.64
	16	30.14	1.34	20.76	1.02	21.84	0.65	15.17	0.39
	22	17.44	0.88	16.65	0.96	13.19	0.63	9.24	0.37
	30	18.58	0.94	14.86	0.98	11.70	0.66	9.05	0.38
	42	16.55	0.96	15.60	0.98	9.67	0.67	7.71	0.37
# TSVs = 400	12	82.96	5.44	62.85	3.90	44.60	2.65	26.46	1.38
	16	40.27	3.05	22.20	1.46	22.30	0.87	15.94	0.52
	22	17.45	1.21	16.72	1.10	14.60	0.74	9.52	0.43
	30	20.88	1.45	17.35	1.21	15.25	0.84	11.65	0.54
	42	17.70	1.45	15.43	1.12	10.44	0.77	7.80	0.45

TABLE III

PARAMETERS FOR DOE1 AND DOE2

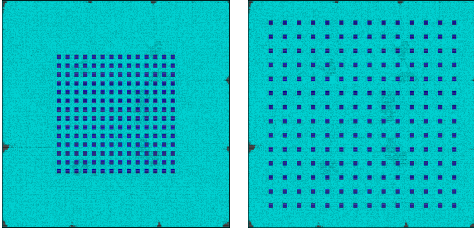| Parameter	Value
Target metal density in DOE1	30%, 40%, 50%, 60%
TSV-to-TSV distance in DOE1 (d)	12, 16, 22, 30, 42 (μm)
TSV-to-TSV pitch in DOE2 (P_T)	12.35, 22.23, 34.58, 46.93 (μm)

Fig. 4. DOE2 - varying TSV-to-TSV pitch in a TSV array. TSV landing pad width is $10\mu m$. Left: pitch = $20\mu m$. Right: pitch = $50\mu m$. (dark squares: TSV landing pads, light lines: standard cells)

TSVs are surrounded by standard cells in realistic circuits. The test case generation step is as follows: (1) we first insert TSVs on a 2D layout, (2) we place standard cells without violating the keep-off distance rule by putting placement obstacles on the TSVs, and (3) we route the circuit and insert fills using the optimal fill pattern described in Section II. The target fill density is 60%. The circuit used in this DOE is FFT1 as shown in Table V. Its 2D layout size is $1.3mm \times 1.3mm$.

For this DOE, we construct an $N_1 \times N_2$ TSV array where $N_1 = 25$ and $N_2 = 20$. The variable of this DOE is the TSV-to-TSV pitch (P_T). Figure 4 shows two examples when the TSV-to-TSV pitch is small vs. large , and Table III shows the full range of P_T.

Figure 5 shows the topography range (MAX-MIN) of DOE2.[1] When the TSV-to-TSV pitch (P_T) is small (e.g. $12.35\mu m$), the topography range is very high (~ 95Å) even after fill synthesis. As P_T increases, however, the topography range decreases rapidly and then becomes flat when P_T becomes bigger than about $20\mu m$. Table VI also shows the topography variation (STD) of DOE2. When P_T is small, the variation decreases rapidly as P_T increases. The decrement, however, becomes small when P_T is large. Therefore, the TSV-to-TSV pitch needs to be sufficiently large in order to obtain better topography results.

[1]The topography range predicted is relatively small. However, this is in part due to the models not having been optimized to our technology in particular. The proposed method is more general and is applicable to many BEOL stacks with improved CMP models.
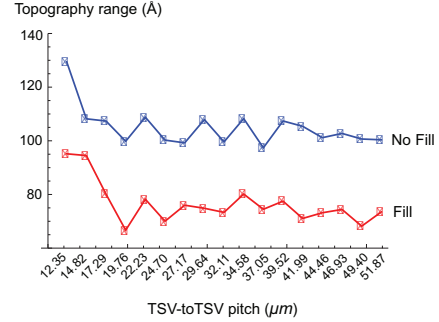

Fig. 5. Results of DOE2. The topography decreases rapidly as the pitch increases when TSVs are too close to each other. After $20\mu m$ separation between TSVs, however, the impact of the pitch on topography saturates. We use this value in our TSV replacement algorithm.

TABLE V

BENCHMARK CIRCUITS

Circuit	2D		3D			
			die0		die1	
	# gates	# nets	# gates	# nets	# gates	# nets
FFT1	324, 490	327, 843	152, 938	154, 809	171, 552	173, 460
FFT2	708, 148	711, 944	354, 556	356, 484	353, 592	355, 786

IV. APPLICATION TO TOPOGRAPHY-AWARE GLOBAL PLACEMENT

The DOE studies in the previous section show that TSVs need to be spread out for better final topography. In this section, therefore, we use the global and detailed placement package presented in [2], which is based on a quadratic force-directed algorithm, and add a repulsive force to separate TSVs for minimization of topography variation.

Topography: Table VII shows the final topography range (MAX-MIN) and the topography variation (STD) for FFT1 and FFT2 circuits. The variation decreases significantly from 15.97Å to 12.19Å when d_m is $40\mu m$ for FFT1. Similarly, the variation decreases from 8.10Å to 5.18Å when d_m is $50\mu m$ for FFT2. Therefore, we observe that topography variation is improved by separating TSVs.

TABLE VI

DOE2

P_T	Topography (Å)		Gradient (Å)	
	MAX - MIN	STD	MAX - MIN	STD
12.35	95.15	18.91	59.42	7.99
22.23	78.21	14.18	59.97	5.39
34.58	80.15	12.95	58.24	8.44
46.93	74.42	11.81	58.71	8.97

TABLE VII

COMPARISON OF WIRELENGTH, WIRELENGTH INCREASE, AND FINAL TOPOGRAPHY WITH AND WITHOUT SEPARATING TSVS DURING GLOBAL PLACEMENT. # DIES: 2. IF THE DISTANCE BETWEEN TWO TSVS IS LESS THAN d_m, WE SEPARATE THE TWO TSVS BY REPULSIVE FORCE.

| Circuit			w/o separating TSVs	d_m			
				$20\mu m$	$30\mu m$	$40\mu m$	$50\mu m$
FFT1 (428 TSVs)	Wirelength (μm)	die0	5,058,723	5,206,121	5,260,133	5,292,694	5,321,305
		die1	6,392,682	6,356,774	6,353,760	6,321,801	6,377,740
		Total	11,451,405	11,562,895	11,613,893	11,614,495	11,699,045
	Wirelength increase			+0.97%	+1.42%	+1.42%	+2.16%
	Final topography (Å)	MAX - MIN	79.76	81.39	79.19	77.61	78.25
		STD	15.97	15.75	15.33	12.19	12.72
FFT2 (328 TSVs)	Wirelength (μm)	die0	14,980,111	15,046,439	15,058,336	15,100,252	15,131,167
		die1	15,112,783	15,114,237	15,120,571	15,117,200	15,127,313
		Total	30,092,894	30,160,676	30,178,907	30,217,452	30,258,480
	Wirelength increase			+0.23%	+0.29%	+0.41%	+0.55%
	Final topography (Å)	MAX - MIN	80.57	72.86	71.96	73.54	73.16
		STD	8.10	5.85	5.79	6.64	5.18
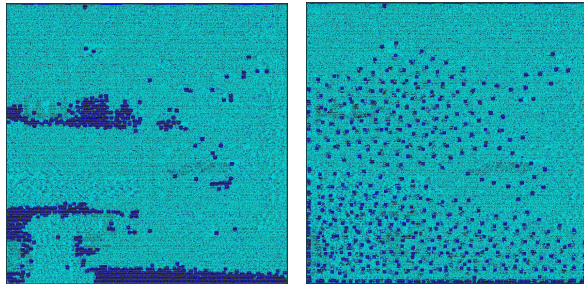
Fig. 6. Placement results (circuit: FFT1). Left: without optimization. Right: with optimization ($d_\mathrm{m} = 40\mu m$). (dark squares: TSV landing pads, light lines: standard cells)

Wirelength overhead: Since we intentionally separate TSVs to increase the distance between two close TSVs, separating TSVs is expected to result in wirelength increase. Table VII also shows the wirelength increase after global and detailed routing.

In both FFT1 and FFT2 cases, the total wirelength monotonically increases as d_m increases. However, wirelength of a single die may not increase monotonically as we optimize locations of cells and TSVs in both dies simultaneously to minimize the overall wirelength.

However, the wirelength overhead for all the cases in our placement remains less than 2.2%. Therefore, separating TSVs does not cause serious wirelength overhead while decreasing the topography variation significantly.

V. CONCLUSIONS

In this paper, we address the manufacturability problem of 3D ICs. The large landing pads of through-silicon vias (TSVs) cause topographic variations for which traditional metal fill is not sufficient. After devising a multi-pass fill pattern using a DOE to minimize the topography variation of 3D ICs, we find a CMP-friendly TSV-to-TSV pitch value using a DOE. We find that by placing TSVs sparsely, we can improve topography. Therefore we apply a repulsive force between TSVs during global placement. Our experimental results show that we achieve we achieve up to 10.69% improvement in topography range and 36.05% improvement in standard deviation with only $0.5\% \sim 2.0\%$ wirelength increase. The proposed method enables manufacturability of TSVs with reduced topography errors.

VI. ACKNOWLEDGMENTS

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