Optical Routing for 3D System-On-Package

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***Abstract*— Optical interconnects enable faster signal propagation with virtually no crosstalk. In addition, wavelength division multiplexing allows a single waveguide to be shared among multiple interconnects. This paper proposes efficient algorithms for the construction of timing and congestion-driven waveguides considering the optical resource constraints. We develop the first optical router for System-on-Packages (SOPs), which reduce electrical wirelength by 11% and improve performance by 23%, when a single optical layer is introduced for every placement layer.**

I. Introduction

The System-on-Chip (SOC) paradigm is a new system integration approach, where not only more and more transistors but various mixed-signal active and passive components are also integrated into a single chip. However, the systems community is beginning to realize that SOC presents fundamental, engineering, and investment limits [1]. This led to the 3D System-On-Package (SOP), where the package not the chip becomes the medium for system integration. Optoelectronics, which today finds use primarily in the back planes and in high-speed board interconnects, is fast moving onto SOP as chip-to-chip for high I/O and high-speed interconnections. Optical interconnects are replacing copper ones and thus addressing both the resistance and crosstalk issues of electronic ICs [2]. In addition, Wavelength Division Multiplexing (WDM) allows a single waveguide to be shared among multiple optical interconnects. Figure 1 illustrates the basic technologies required for a fully integrated digital-optical micro-system.

In this paper we present the first optical router for 3D System-On-Package. A recent work on placement for 2D SOP presented in [3] performs clock routing using optical waveguides. Our approach is to start with a pure electrical interconnect routing solution, build a set of customized waveguides, and convert a subset of electrical wires into optical interconnects by rerouting multiple nets to use these waveguides. Thus, our optimization goal is to minimize the total wirelength and delays under various layout capacity constraints due to optical devices and waveguides.

II. Problem Formulation

Given a 3D SOP placement, a set of nets N and number of placement layers L_p, the *3D SOP Optical Routing Problem* can be defined formally as follows: generate a routing topology for each net $n \in N$, assign n to *optical* or *electrical* routing layer or both, and assign all pins of n to legal locations, while minimizing the critical net performance D_{max}. All conflicting nets are assigned to a different routing layer. The number of optical layers are fixed to *one* per routing interval.

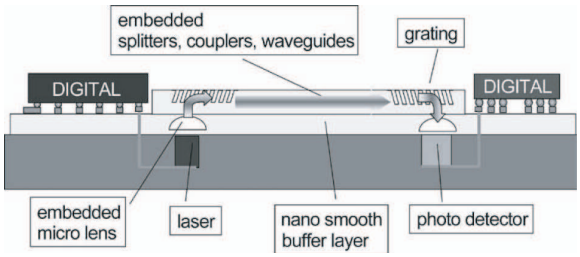

Fig. 1. Optical routing in System-On-Package.

The nets containing optical interconnects are modeled as buffered interconnects. The internal delay of this buffer model depends linearly on the optical interconnect length. Elmore delay model is used to estimate the performance of the nets.

III. Algorithms Overview

SOP optical routing is done in three phases: (i) construction of optical waveguides based on performance and congestion consideration, (ii) optimum net-to-waveguide mapping using maximum-flow minimum-cost network flow model, (iii) ripping and rerouting of existing nets to relieve congestion and maximize utilization of the waveguides. We integrated optical routing in a SOP global router [4] for this work.

The waveguides can be constructed (customized) to primarily reduce *timing* or *congestion*. Additionally, a *standard* waveguide pattern can also be pre-fabricated on the optical routing layer. The timing criticality of a net is defined as the ratio between the net delay and the worst delay among all nets in the routing layer.A net is said to be a critical net if its criticality exceeds a predefined *criticality level*. The algorithm starts with the set of pre-selected timing critical nets, which are sorted by their criticalities. The paths for each of the critical sinks (sinks with delays above a threshold) of the net are computed. These paths are segmented at its branch points. The set B contains a set of no-branch segments. The cost of waveguide insertion at each of the locations of the segments in B is computed. The waveguide is constructed at the location with the minimum cost. In *customized waveguide construction*, heavily used edges are noted in each routing interval and planar waveguides are constructed in these areas to reduce the number of electrical nets using these edges and thus reduce congestion.

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TABLE I

COMPARISON BETWEEN ELECTRICAL, CONGESTION-DRIVEN, STANDARD WAVEGUIDES AND TIMING-DRIVEN OPTICAL ROUTING WITH NO VIOLATIONS. WE REPORT THE TOTAL WIRELENGTH, ROUTING LAYER (XY) USAGE, AND MAXIMUM NET DELAY (NS).

	Electrical			Congestion Optical			Standard Optical			Timing Optical		
ckt	WL	lyrs	D_{max}	WL	lyrs	D_{max}	WL	lyrs	D_{max}	WL	lyrs	D_{max}
n30	0.619	3.5	2.609	0.561	3.5	2.609	0.601	3.5	2.609	0.592	3.5	2.083
n50	0.899	5	2.722	0.799	4.5	2.722	0.843	5	2.721	0.857	4.5	2.079
n100	1.458	7.5	2.666	1.349	7.5	2.666	1.439	7.5	2.503	1.399	7.5	2.036
n200	2.710	16	2.553	2.524	13	2.553	2.582	16	2.553	2.650	16	2.143
n300	4.098	13	3.237	3.781	12.5	3.059	3.956	13	3.037	4.041	12.5	2.837
TIME	20			108			33			52		

TABLE II

TIMING-DRIVEN OPTICAL ROUTING WITH DIFFERENT CRITICALITY LEVELS. WE REPORT THE TOTAL WIRELENGTH, ROUTING LAYER (XY) USAGE, MAXIMUM NET DELAY (NS), AND MAXIMUM VIOLATIONS.

	cLevel=0.90				cLevel=0.85				cLevel=0.80			
ckt	WL	lyrs	D_{max}	viol	WL	lyrs	D_{max}	viol	WL	lyrs	D_{max}	viol
n30	0.606	3.5	2.261	0	0.604	3.5	2.134	0	0.592	3.5	2.083	0
n50	0.884	5	2.283	0	0.872	4.5	2.234	0	0.857	4.5	2.079	0
n100	1.442	7.5	2.356	0	1.426	7.5	2.212	0	1.399	7.5	2.036	0
n200	2.677	16	2.283	0	2.650	16	2.143	0	2.598	16	1.987	1
n300	4.041	12.5	2.837	0	3.979	12.5	2.638	4	3.934	12	2.453	6
TIME	27				48				57			

The next step is to select a optical set of nets and assign them to the waveguides we constructed using a minimum-cost maximum-flow network flow model. The source node connects to the net nodes (each net is assigned a node) and all waveguide nodes (each waveguide is assigned a node) are connected to a sink node. A net node is connected to a particular waveguide node if all the routing edges in that waveguide are contained in the net. Each edge in this flow graph is assigned a capacity and cost value, depending on the waveguide utilization. Finally, the flow analysis provides flow values for each edge that tells us how useful it is to retain that edge in our final model.

After routing the net through the optical waveguides, it is desirable for the electrical part of the net *not* to go through these optical regions,thereby reducing overall electrical routing congestion. The electrical routes are ripped and rerouted using weights on the routing graph. The net is converted back to electrical if the delay exceeds the budget.

IV. EXPERIMENTAL RESULTS

We implemented our algorithms in C++/STL and ran our experiments on Linux Beowulf clusters. For our experiments we used the standard GSRC floorplanning benchmarks. The blocks are placed into four-layer SOPs using our SOP floorplanner [4].

The technology parameters for 0.13μ process was used for Elmore delay computation. Specifically, the driver resistance (R_d) of $29.4k\Omega$, input capacitance (C_L) of $0.050fF$, unit-length resistance (r) of $0.82\Omega/\mu m$ and unit-length capacitance (c) of $0.24fF/\mu m$ are used. For calculating the optical delay, v_w was chosen to be $1.936 \times 10^8 m/s$ and t_d was assigned $200ps$ [2]. The values of optical buffer parameters R_w and C_w was chosen to be the same as R_d and C_L. The wirelengths reported have been scaled down by $10^5 \mu m$. The runtimes reported are in seconds.

Table I compares pure electrical routing with congestion-driven optical routing, optical routing using standard waveguides, and timing-driven optical routing. An average wirelength saving of 8.5% was achieved using customized waveguides. The maximum wirelength improvement was 11% for $n50$. The amount of wirelength saved is less with the standard waveguides (3.7%). The wirelength saving in timing-driven optical routing is 3.6% and the performance enhancement is 19% on the average.

Table II compares timing-driven optical routing with different *criticality levels*. The wirelength savings using criticality levels of 0.90, 0.85, 0.80, are 1.5%, 2.6% and 4.3%. The performance improvements are 13%, 17.6% and 22.8% respectively. A maximum of 23.7% delay improvement without resource violations is achieved with a criticality level of 0.80 for $n50$ and $n100$.

V. CONCLUSIONS

In this paper we presented the first optical router for 3D System-On-Package. We developed algorithms for the construction and optimization of optical waveguides based on performance and congestion objectives.

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