Glass Interposer Integration of Logic and Memory Chiplets: PPA and Power/Signal Integrity Benefits

Pruek Vanna-Iampikul[1], Lingjun Zhu[1], Serhat Erdogan[1], Mohanalingam Kathaperumal[1], Ravi Agarwal[2], Ram Gupta[2], Kevin Rinebold[3] and Sung Kyu Lim[1]
[1]School of ECE, Georgia Institute of Technology, Atlanta, USA; [2]Meta Platforms, Inc., Menlo Park, CA, USA
[3]Siemens Industry Software, Inc., Plano, TX, USA
{v.pruek, lingjun, serhat.erdogan}@gatech.edu; {kmohan, limsk}@ece.gatech.edu
{ravisagarwal, rngupta}@meta.com; kevin.rinebold@siemens.com

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***Abstract*—Glass interposers enable 3D stacking between the chiplets embedded into the substrate and the ones stacked directly on top, which is not possible in silicon. In this work, we demonstrate the benefits of such stacking in glass interposers over silicon in terms of key system-level metrics including area, wirelength, signal, power, and thermal integrity. We achieve this goal with GDS layouts of both chiplets and interposers and sign-off simulations. Our experiments show that glass offers 2.6X area, 21X wirelength, 17.72% full-chip power, 64.7% signal integrity, and 10X power integrity improvement over silicon at the cost of 15% increase in temperature.**

I. Introduction

One promising approach to improve the yield of highly complex systems today and tomorrow is partitioning a system into "chiplets" [1]. These chiplets are to be integrated to form the overall system. Depending on the physical configuration, there exist two types of chiplet integration: 2.5-D interposers and 3D stacking. The 2.5-D integration has become an appealing option as it allows the integration of multiple off-the-shelf chiplets or intellectual properties (IPs) reuse on an interposer with different technology nodes (Heterogeneous integration). In 2.5-D, chiplets are placed side-by-side as flip-chip on top of the interposer packaging as in Figure 1(a). Moreover, they are connected through the redistribution layer (RDL), metal layers on passive interposer substrate, which provide lateral connections between chiplet and distribute the power from an external source. Common interposer packaging materials are silicon, organic, and glass.

In 3D integration, multiple chiplets are stacked on top of each others and connected through through-silicon-via (TSV) with micro bumps. Both Silicon and organic interposers require TSV-based, resulting in low bandwidth and significant overhead due to large TSV size. However, The glass is the only material that allows the chiplet to be placed within the substrate, naturally providing 3D stacking capability between the embedded die and the conventional flip-chip die on the top. Also, the Glass interposer offers low-cost options to embed chiplets directly inside the substrate itself. This embed capability enables 3D stacking configuration between the embedded dies and the conventional flip-chip dies mounted directly on top. Furthermore, the interconnect pitch and through-glass-via (TGV) diameter in glass are becoming comparable to their counterparts in Silicon, making glass a compelling option for 2.5D heterogeneous integration compared with Silicon.

Previous work has studied the process and performance comparison between glass and silicon interposers [2]. However, the analysis was only carried out for the packaging level without a full-chip design. Therefore, the high-density connection impact has yet to be considered. Another related study has performed the system-level comparison between Silicon and organic interposer [3]. However, the system-level comparison of glass interposer and other state-of-the-art interposers has yet to be performed with 3D stacking where glass interposer enables the capabilities to embed the chiplet inside the substrate.

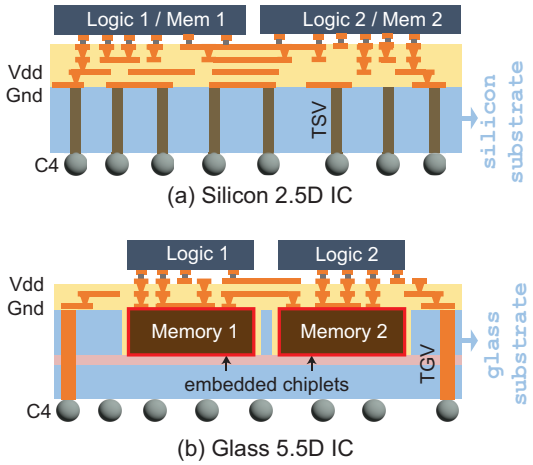

Fig. 1. Cross-sectional view of logic and memory chiplet integration. (a) "2.5D" silicon interposer using through-silicon-via (TSV), (b) "5.5D" glass interposer using die embedding and through-glass-via (TGV).

In this paper, we explore the potential chiplet integration of glass interposers in non-TSV based "5.5D" stacking as in Figure 1(b), where there consists of both vertical and lateral connection among chiplets. And we perform a detailed comparison with state-of-the-art (SOTA) interposers, such as Silicon and organic interposers, as these are common interposer choices in the industry. Our contribution is as follows:

1) We co-designed the chiplets and interposer of RISC-V processor design with commercial quality using glass interposer in 5.5D stacking fashion.
2) We perform detail analysis of power, performance, area (PPA) , signal integrity (SI), power integrity (PI), and thermal integrity (TI) on our final design to highlight the benefits of glass interposers compared to SOTA interposers.
3) We quantify the cost analysis from PPA and interposer analysis to help estimate manufacturing cost with sign-off quality design and accurate simulation for the first time for glass interposer in 5.5D stacking.

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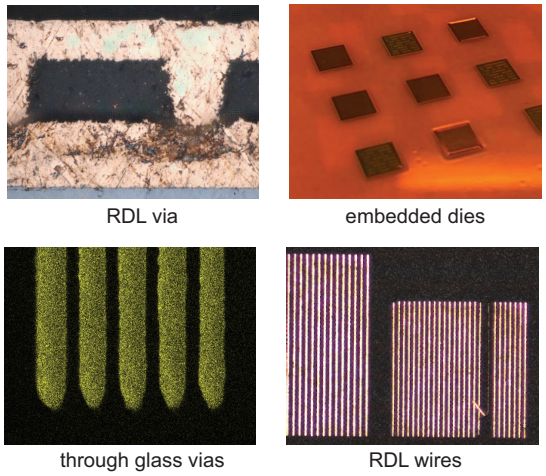

Fig. 2. Our manufactured samples of key elements in the glass interposer technology. Dimensions are reported in Table I.

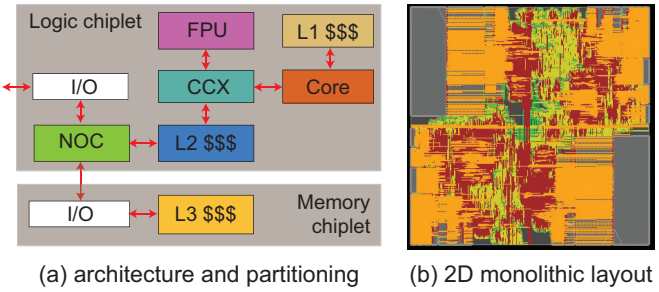

Fig. 3. (a) Single tile architecture of OpenPiton RISC-V [7] and our logic/memory chiplet partitioning, (b) single chip design using TSMC 28nm.

II. Glass Interposer Manufacturing

Glass has been extensively studied in recent years as an interposer substrate due to its favorable mechanical, electrical, and thermal properties [4]. The ability to process glass as large panels presents a major benefit when building systems consisting of a large number of chiplets. A smooth surface of glass enables high-density wiring similar to silicon interposers on large panels at a lower cost. The lowest line/space demonstrated on glass interposer with embedded dies in literature is 2µm [5].

Our proposed "5.5D" interposer architecture shown in Figure 1 relies on the ability to embed chips into glass cavities to form short chip-to-chip "microvia" interconnects through RDL. Blind or through cavities in glass can be drilled using wet etching or laser drilling steps, where the cavity depth can be controlled by optimizing the etch rate or the laser focus. Surface non-planarities in the RDL due to the embedded dies can be mitigated by applying surface planarization. The minimum diameter of the microvias on RDL is usually limited by the dielectric layer thickness. The width-to-depth aspect ratio of the microvias drilled with UV laser on the polymer is typically 1:1 [6]. The semi-additive patterning process is used for fabricating the RDL, where a 50nm thickness Ti layer was used to improve the adhesion between the copper wiring and the dielectric. Figure 2 illustrates various fabrication results such as RDL vias, embedded dies, TGVs, and RDL wires.

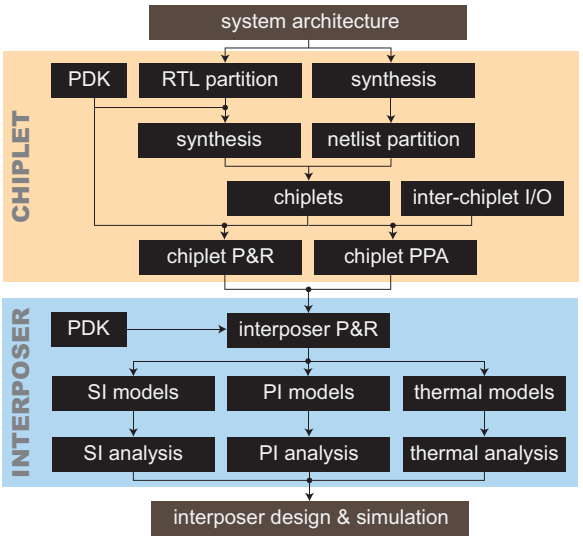

Fig. 4. Our chiplet/interposer co-design flow. Our chiplet tools are from Cadence, Synopsys, and in-house, while the interposer designs and simulations are done with tools from Siemens and Ansys. SI and PI respectively denotes signal and power integrity.

III. Design and Simulation Settings

A. Architecture Benchmark

We leverage the RISC-V OpenPiton architecture [7] as our benchmark, as shown in Figure 3. The OpenPiton chip design consists of 2 OpenPiton tiles. Each tile is connected via the NOC Router within each tile. Each OpenPiton tile consists of computational modules (Core, floating point unit (FPU), and CPU Cache-crossbar(CCX)), memory modules (L1 caches, L2 caches, and L3 caches), and a network-con-chip (NOC Router).

We chipletize each OpenPiton single tile into two parts by using the hierarchical-based partitioning. First, we group the L3 cache and its glue logics as memory chiplet, and treat the remaining modules as logic chiplet. With this grouping, we ensure the minimum cut-size between two chiplets such that the die size is minimum considering the bump pitch constraint for each I/O pins.

Since the connections between two OpenPiton tiles are relatively large with six 64-bit buses and 20 control signals, the I/O bumps can not fit into the chiplet due to the micro-bump pitch constraint in order to have practical cell utilization. Therefore, we insert the SerDes module to reduce the number of connections from 64-bit parallel wires to 8-bit serial wires. The control signal remains unchanged. The connections between OpenPiton tiles is 68, while the connections within a tile is 231.

B. Chiplet/Interposer Co-design Flow

Our design flow is shown in Figure 4, where we design both chiplet and interposer and perform the analysis, including PPA simulation, Interposer design analysis, SI, PI, and TI analysis. The design flow consists of two approaches of chipletization: hierarchical-based partitioning, flattening partitioning. In this study, we utilize the hierarchical-based partitioning (left branch). From the OpenPiton architecture in Section III-A, we first generate the register-transfer-level (RTL) of the OpenPiton chip design with two tiles setting. Next we partition modules based on Figure 3(a) and synthesize the netlist with process design kit (PDK) for a particular technology node. Each logic and memory chiplet netlist is reused for each

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TABLE I
INTERPOSER SPECIFICATIONS USED IN THIS PAPER.

	Glass	Silicon [8]	Shinko [9]	APX [10]
# Metal Layer	3	4	6	8
Metal thickness	4µm	1µm	2µm	6µm
Dielectric thickness	15µm	1µm	3µm	14µm
Dielectric constant	3.3	3.9	3.5	3.1
Min. Wire W / S	2µm/2µm	0.4µm/0.4µm	2µm/2µm	6µm/6µm
Via size	22µm	0.7µm	10µm	32µm
Bump size	16µm	20µm	25µm	32µm
Die-to-Die spacing	100µm	100µm	N/A	150µm
Micro-bump pitch	35µm	40µm	40 µm	50µm

OpenPiton tile. The connections between chiplets are considered off-chip connections, so the I/O drivers are mandatory to meet target timing. We design our inter-chip I/O driver to support the maximum interconnect length which is first obtained from the interposer design. And, We insert them into the chiplet netlist for each I/O pin and perform the chiplet design with Cadence Innovus. Finally, we analyze the chiplet PPA with Cadence Tempus.

In the interposer design step, we import in the chiplet footprint and interposer stack-up information such as metal layers, dielectrics, vias, and substrate. We insert the power delivery network (PDN) into the interposer and perform routing using Siemens Xpedition tool. Next, we analyze the SI, PI, and TI from interposer layout. Lastly, we verify all the design with simulation to ensure the performance, power, and thermal constraints are met.

C. Interposer Design Rules

We implement Glass, Silicon, and organic interposers using the design rule as defined in Table I. For glass interposer, we refer to the specification from the manufacturing capabilities of Georgia Tech's Packaging Research Center (PRC), where we are capable of manufacturing fine line 2um line and spacing. The micro-bump pitch supports with a minimum of 35um, which allows high-density I/O connections. The glass interposer allows the creation of a cavity and embeds the die inside. For the Silicon interposer, we leverage the Chip-on-Wafer-on-Substrate (CoWoS) technology [8], which provides 0.4 um line and spacing with 40um micro bump pitch. For Organic interposers, we have two types of organic interposers: Shinko [9] and Advance Packaging X (APX) [10]. The Shinko interposer provides fine-line from an additional thin film layer on top of conventional organic build-up layer. The APX is the conventional organic interposer which has improved over the year to support high-density connections.

IV. CHIPLET DESIGN RESULTS

A. Chipletization Results

We group the RTL based on Figure 3(a) and synthesize the netlist of the logic and memory chiplet. Since the chiplet are to be connected via an interposer RDL, we utilize the I/O driver design from [3], which supports the maximum transmission length of $10mm$. The I/O driver is designed based on Intel's Advance Interface Bus (AIB) with pipe-lining for data transmission. Therefore, the connection between chiplets would take one clock cycle to transmit, accommodating more flexible timing closure. We insert the I/O driver into the chiplet netlist. For the inter-tile connection (Logic-to-Logic), we insert the serialized connection module before the I/O driver. The micro bumps are placed with the minimum pitch for each interposer design as defined in Table I. Finally, we implement the layout and generate the Liberty model library to be used as hard macros in the chiplet design.

We calculate and design the chiplet footprint as in Table II. The signal bump to power bump ratio is 2 to 1 to have a compact footprint

TABLE II
CHIPLET BUMP USAGE AND AREA COMPARISON. ALL CHIPLETS ARE SQUARE. SILICON AND SHINKO HAVE THE IDENTICAL RESULTS DUE TO THE SAME MICRO-BUMP PITCH.

	Glass		Silicon		APX	
	logic	mem	logic	mem	logic	mem
Micro-bump pitch	35µm		40µm		50µm	
Signal bump	299	231	299	231	299	231
P/G bump	165	121	165	130	150	116
Total bump	464	352	464	361	449	347
Width (mm)	0.82	0.82	0.94	0.82	1.15	1.0
Area (mm^2)	0.67	0.67	0.88	0.67	1.20	1.00
Area ratio	1.0	1.0	1.3	1.0	1.8	1.5

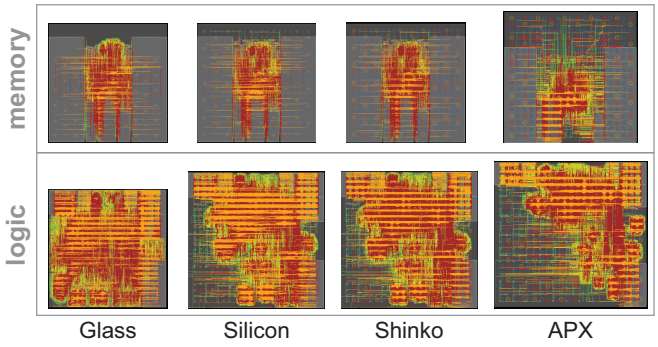

Fig. 5. GDS layout of chiplets used in our interposer designs. The dimensions are provided in Table II and power & performance in Table III.

with high density. The number of total bumps in the logic chiplet is higher than the memory chiplet because the logic chiplet contains the connection across the different OpenPiton tiles and the connection within the tile (to the memory chiplet).

For different interposer materials, glass interposer has the minimum footprint width and height since the micro bump pitch in the design rules of glass interposer is 35um which is the minimum compared to other interposers. Since the bump pitch of the Silicon and Shinko interposer are the same, the footprint of both chiplet is equal in size, while the APX has the largest chiplet footprint due to the larger micro-bump pitch. Therefore, the Area ratio between logic and memory remains identical across different interposer materials. However, with the different footprint sizes among different interposers, the footprint density(%) varies.

B. Chiplet Power and Performance Comparison

We perform the chiplet place-and-route with the footprint information as in Table II with the commercial 28nm PDK using the Cadence Innovus as the physical design tool with selected protocol translator and I/O driver. We first place the I/O pins based on micro bump placement for both signal and P/G pins. Moreover, we place the I/O driver as hard macro at the micro bump location to minimize the wire delay from input to the micro bump pad location. We allow the serialization module to be placed by the auto-placement engine to optimize the location. The final layout for each chiplet is shown in Figure 5. In addition, the power and performance results for individual chiplets are provided in Table III. We set the target frequency at 700MHz for logic and memory chiplet in all design options.

From Table III, we observe that most of the chiplet can be closed at 700MHz. The glass interposer chiplet has the smallest footprint compared to the other interposer's chiplet because the bump pitch in

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TABLE III
POWER AND PERFORMANCE COMPARISON OF THE CHIPLETS USED IN OUR INTERPOSER DESIGNS. WE ALSO REPORT THE AREA AND POWER OVERHEAD OF INTEL AIB DRIVERS.

	Glass		Silicon	
	Logic	Memory	Logic	Memory
Fmax (MHz)	684	697	689	698
Power (mW)	141.73	45.9	138.76	45.6
AIB area (μm^2)	22,507	17,388	22,507	17,388
	(3.40%)	(2.90%)	(3.30%)	(2.90%)
AIB power (mW)	0.54	0.16	0.59	0.18
	(0.40%)	(0.30%)	(0.40%)	(0.40%)
	Shinko		**APX**	
	Logic	Memory	Logic	Memory
Fmax (MHz)	676	697	690	694
Power (mW)	141.9	45.85	141.93	47.29
AIB area (μm^2)	22,507	17,388	22,507	17,388
	(2.90%)	(2.80%)	(2.20%)	(1.70%)
AIB power (mW)	0.59	0.18	0.54	0.16
	(0.40%)	(0.40%)	(0.38%)	(0.34%)

the glass interposer is the smallest. From Figure 5, we observe that the size of the memory chip of Glass and Silicon are equal even if the bump pitch in Silicon is higher than in Glass. The main reason is that in memory chiplet, there are memory macros which is the limiting factor of the footprint; even all I/O pins can fit within a smaller area. Therefore, the power consumption of all chiplet is similar, and the I/O driver (AIB) power is considered small to the total power.

We observe that the micro-bump placement in Glass and Silicon is different. In Glass, we assign the location to align with the bump location of the logic chiplet, but in Silicon, we utilize all the footprint area to fit all pins. For Logic chiplet, Silicon has a larger footprint due to a larger micro-bump pitch. The APX has the largest chiplet size compared to other interposers, which results in lower cell utilization. The power consumption among all interposers is considered comparable with marginal differences. Moreover, the AIB I/O driver area and power are small compared to the overall area and power of the chiplet

V. INTERPOSER PLACE/ROUTE RESULTS

Once we obtained the chiplet GDSII layout for all interposers, we integrated them into the interposers using the Siemens Xpedition tool. Each chiplets contains footprint size and micro-bump location for all I/O and power/ground (P/G) pins.

A. Interposer Placement Method

Both signal and P/G bumps and the chiplet footprint represent the chiplet in the commercial tool. We assign the signal and P/G bumps from a unit pattern of a 2X4 grid array, where 6 out of 8 bumps are the signal bumps, while the remaining 2 are the P/G bumps. The pattern is repeated until all I/O pins are assigned. Next, we removed the floating micro bumps since they will be unused. Finally, we specify each micro-bump location with the net name from the top-level netlist to ensure that both inter-tile and intra-tile connections matches and represent the connection in the commercial tool.

After specifying net names for micro bumps on each chiplet, we place the die according to die spacing constraints for each interposer type. In the glass interposer, the memory chiplet is embedded underneath the logic chiplet at the same location, enabling connection through stacked vias in the RDL, saving metal layers and shortening interconnections. This unique arrangement takes advantage of the glass interposer's die-embedding capabilities. With two OpenPiton tiles, we place the second tile similarly, connecting logic chiplets

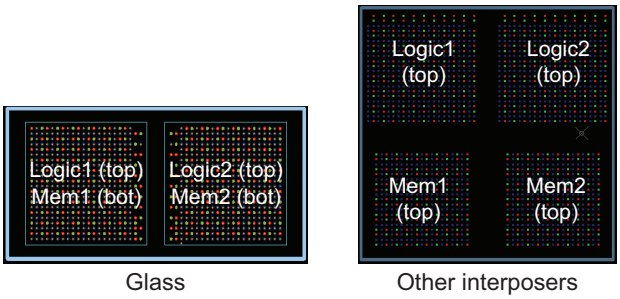

Fig. 6. Top-down view of the placement of the four chiplets, two logic and two memory. (a) logic and memory are stacked vertically in glass, (b) chiplets are placed side-by-side only in silicon, Shinko, and APX. See Figure 1 for cross-sectional view.

between tiles due to the NOC Router module's location in the logic chiplet after chipletization and module grouping. Figure 6(a) illustrates the glass interposer's die placement. For other interposers like Silicon, Shinko (organic), and APX (organic), chiplets are placed side-by-side, as shown in Figure 6(b), since the substrate doesn't support chiplet embedding.

B. Interposer Routing Method

We developed a sophisticated metal stack configuration based on interposer specifications for materials listed in Table I. Our approach features distinct routing strategies for glass, silicon, and organic interposers. Manhattan-style routing is employed for glass and silicon interposers to comply with manufacturing recommendations, while diagonal routing is introduced for organic interposers to accommodate their larger wire width and limited track space. This ensures the preservation of minimum micro bump spacing. We employ auto-routing with guided direction for a fair comparison. Furthermore, we have enhanced the power delivery network (PDN) by incorporating two additional metal layers, with the power metal layer positioned above the ground metal layer, to optimize signal-routing performance.

For the glass interposer, we insert the through-glass via (TGV) to support external power and ground connection as illustrated in Figure 7(a). The power and ground are implemented as a plane with vias to deliver the power to the chiplets. We use traditional through-silicon-via (TSV) for the Silicon interposer to connect the external power and ground from C4 bumps. The power and ground plane for silicon starts at metals 3 and 4 since the metal layer required to complete the signal routing in the silicon interposer is more than in the glass interposer. For organic interposers (Shinko and APX), we implement the PDN the same as the silicon interposer. The final layout of the interposer with PDN is shown in the Figure 8. The size of the layout reflects the relative relationship among all interposers.

C. Interposer Routing Comparison

From Table IV, we observe that the glass interposer utilizes the minimum metal layer with one metal layer for signal routing for lateral connections and the other two metal layers for PDN sharing with stacked vias for vertical connections. Silicon interposer requires an additional layer to complete the routing since all the connections have to connect horizontally. However, with thin line space, the silicon interposer does not require more metal layer to complete the routing compared to Shinko and APX, which requires more metal layer for signal routing. For total wirelength, the glass interposer obtains the shortest wirelength because the connection within the tile use stacked via to connect. For other interposers, the wirelength

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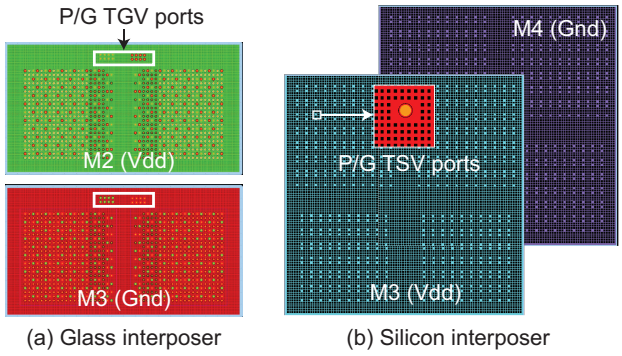

Fig. 7. Power delivery network of glass and silicon interposers.

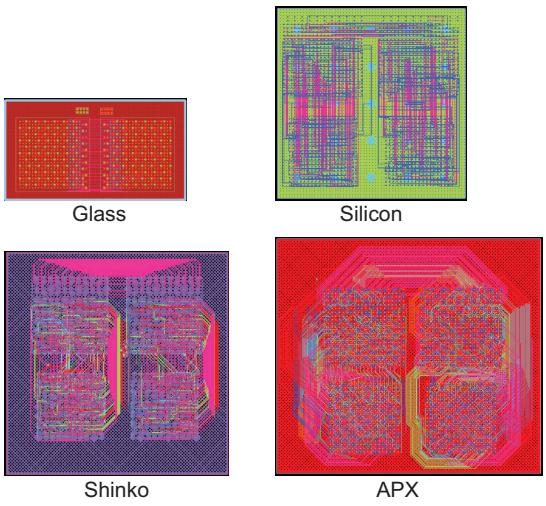

Fig. 8. Interposer routing layouts. All metals including signal and power/ground are superimposed in each design.

TABLE IV
INTERPOSER DESIGN RESULTS. ALL WIRE LENGTHS (WL) ARE REPORTED IN mm.

	2D mono	Glass	Silicon	Shinko	APX
Metals used	-	1+2	2+2	4 + 2	6+2
Total WL	-	29.69	772.9	803	881
Ave WL	-	0.43	1.5	1.4	1.6
Max WL	-	0.67	3.01	3.6	6.5
Via usage	-	21 + 924	1542	2190	3178
Footprint	1.6x1.6	1.8x1.0	2.2x2.2	2.5x2.5	3.2x2.7
Area (mm^2)	2.56	1.87	4.84	6.25	8.64
Power (mW)	330.92	399.75	417.47	437.81	506.33
PDN DC impd (Ω)	-	0.97	7.4	180	58
PI Settling Time (μs)	-	3.7	4.1	4.9	5.4
PI Voltage drop (mV)	-	17	27	23	17

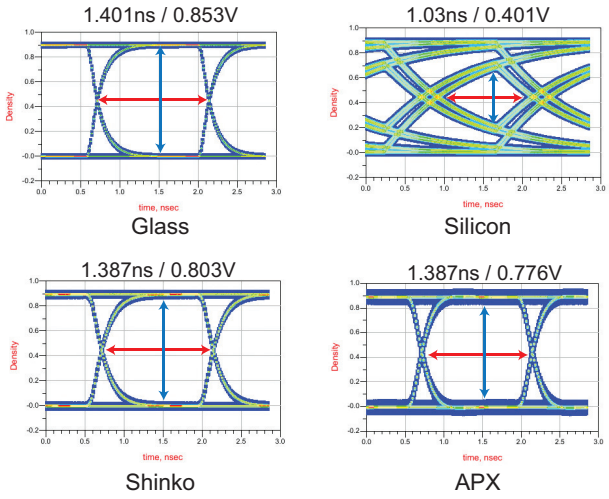

Fig. 9. Eye diagram comparison of the worst-case victim nets.

is comparable, whereas thicker line width increases wirelength due to detour routing and limited tracks. Glass's minimum, average and maximum wirelength is better due to the stacking benefit.

The interposer via usage correlates with the number of metals used. As a result, the APX has the most via usage. For footprint, the glass interposer obtains the smallest footprint die-to-die stacking. Other interposer footprint size depends on the metal thickness and die spacing. For Shinko and APX, the footprint is larger because the wire needs additional area since there is not enough track between the micro bumps pitch and via pads. As a result, glass interposer offers lower cost, shorter wirelength, and smaller footprint area.

VI. Interposer Reliability Results

A. Interposer Signal and Power Integrity Analysis Method

We model the transmission line of the interposer with the I/O driver for both driver and the receiver. First, we generate the inverting signal as an I/O driver to send the signal through the interposer wire and finally at the receiver end. The chosen I/O driver size is x128, same as [3] with the output impedance of 47.4Ω. The interposer transmission model is generated with HyperLynx Advance Solver and exported into spice netlist for the timing and power simulation. Next, we analyze the timing and power analysis with self-generated SPICE models, which include I/O drivers and interposer model spice circuits.

For signal integrity, we capture the longest net and the other two surrounding nets in the interposer design. The longest net will be treated as a victim net, while the other two surrounding nets are the aggressor. We cropped the interposer layout with three capture nets to generate the S-parameter model using the Siemens HyperLynx Advance solver tool. Then, we parse the S-parameter into Keysight ADS to generate the eye diagram. The results are simulated with the data rate of 0.7Gbps, I/O impedance of 50Ω, and receiver chiplet pad parasitics.

The power integrity of our design is simulated by generating the PDN impedance profile from the interposer layout using the HyperLynx Advance Solver tool. The frequency range of PDN Impedance simulation is from 10^6 to 10^9 Hz. Moreover, we simulate the power transient analysis by extracting the S-parameter of PDN and connecting them with the Integrated Voltage Regulator at 125MHz to measure the voltage drop and timing to settle for each interposer.

B. Interposer Signal and Power Integrity Comparison

We extract the S-Parameter from the longest net in the interposer layout and create the eye diagram for all interposers. From Figure 9, we observe that the glass interposer has the widest eye with 1.401ns and 0.853V due to the shortest wirelength. On the other hand, the silicon interposer has the narrowest eye because the wirelength is long, and the net detour across multiple layers. The long wirelength is due to the metal layer constraints since we use only two layers for the Silicon interposer. For APX and Shinko, the eye diagrams are

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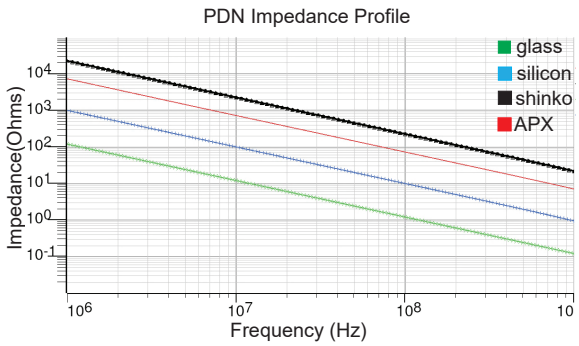

Fig. 10. PDN Impedance profile comparison for different type of interposers

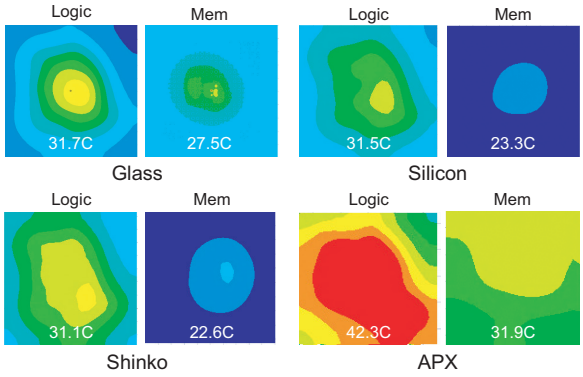

Fig. 11. Chiplet thermal distribution comparison. Our thermal analysis covers both the chiplets and the interposer for each interposer material choice.

wider than Silicon and considered comparable with slight differences in voltage level. In contrast, APX has a lower voltage level due to its longer wirelength.

We examined the PDN impedance impact across various interposer materials, maintaining a fixed PDN density with a plane-type PDN. Our analysis in Figure 10 reveals that glass interposers have the lowest impedance due to their higher metal-to-dielectric thickness ratio and thicker metal. Silicon interposers rank second, while APX and Shinko exhibit higher impedance. This impedance behaves similarly to capacitor impedances, with lower impedance at higher frequencies. For power transient and voltage drop analysis, we input 125MHz switching power to memory chiplets on all interposer materials. The glass interposer exhibits the fastest settling time and lowest voltage drop due to its superior PDN impedance profile. Glass also provides the minimum system power among all interposer materials, though it is higher than 2D monolithic ICs.

C. Interposer Thermal Reliability Results

To conduct interposer thermal analysis, we first create a Chip Thermal Model (CTM) for each chiplet using Ansys Redhawk, comprising tiled-based power and metal density maps. We then integrate a layer-based power map with the Ansys CPS tool to generate an 8x8 heat source power density map. Using coarse-grained tiles in Ansys IcePak, we model the interposer, including substrate, RDL, micro bumps, and chiplets. We assign the tile-based heat source to the bottom face of flip-chip dies and the top face of embedded dies, encompassing both packaging and chiplets in the thermal analysis. Lastly, we analyze the thermal performance with a minimum airspeed of 0.1 m/s, ensuring operation within the temperature range without requiring active cooling solutions like heatsinks.

We analyzed the thermal distribution across all interposer materials and found that the glass interposer's memory chiplet has a higher temperature range than others, except for the APX interposer, as shown in Figure 11. This is because the heat in the embedded die can only dissipate through TGV to the top RDL layer. The APX memory and logic chiplets have the highest temperatures due to the material properties absorbing the thermal energy. In the glass interposer, the logic chiplet has a lower temperature as heat dissipates through the air. Except for APX, all logic chiplets in other interposers have similar temperature ranges. The maximum temperatures of the glass interposer's logic and memory chiplets are 31.7°C and 27.5°C, respectively. For other interposers, the memory chiplet's temperature is around 23.3°C, while the Organic APX has the worst heat dissipation due to its dielectric material property.

VII. CONCLUSION

We introduce a 5.5D IC chiplet integration using a glass interposer, co-designing both chiplet and interposer and analyzing the results, including chiplet PPA, interposer routing, signal and power integrity, and thermal distribution in comparison to leading silicon and organic interposer alternatives. The glass interposer offers advantages such as shorter wirelength, smaller footprint, and superior signal and power integrity compared to 2.5D interposers. Additionally, we suggest partitioning the chiplet to maintain the embedded die's thermal condition within the operating range.

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