

Thermal Characterization of Interlayer Microfluidic Cooling of Three-Dimensional Integrated Circuits With Nonuniform Heat Flux

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It is now widely recognized that the three-dimensional (3D) system integration is a key enabling technology to achieve the performance needs of future microprocessor integrated circuits (ICs). To provide modular thermal management in 3D-stacked ICs, the interlayer microfluidic cooling scheme is adopted and analyzed in this study focusing on a single cooling layer performance. The effects of cooling mode (single-phase versus phase-change) and stack/layer geometry on thermal management performance are quantitatively analyzed, and implications on the through-silicon-via scaling and electrical interconnect congestion are discussed. Also, the thermal and hydraulic performance of several two-phase refrigerants is discussed in comparison with single-phase cooling. The results show that the large internal pressure and the pumping pressure drop are significant limiting factors, along with significant mass flow rate maldistribution due to the presence of hot-spots. Nevertheless, two-phase cooling using R123 and R245ca refrigerants yields superior performance to single-phase cooling for the hot-spot fluxes approaching $\sim 300 \text{ W/cm}^2$. In general, a hybrid cooling scheme with a dedicated approach to the hot-spot thermal management should greatly improve the two-phase cooling system performance and reliability by enabling a cooling-load-matched thermal design and by suppressing the mass flow rate maldistribution within the cooling layer.

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1 Introduction

As the complementary metal-oxide semiconductor (CMOS) technology advanced to sub-100 nm to fulfill the demands of high-performance computing and information technology, the challenges of on-chip wiring or interconnect density, and matching the interconnect performance with that of transistors have become increasingly critical [1]. In the future gigascale integrated systems, the signaling interconnections or wiring need to be driven at ever-higher clock speed, even with the increased number and length of global wires [2]. Consequently, a substantial fraction of power consumption in the high-power chips is attributed to the increasing interconnect loading, such as wiring networks used for clock distribution [3]. Geometric flexibility in the stacked chip design and chip-to-chip routing within a stack, which can be enabled by three-dimensional (3D) stacking, have been proposed to address the interconnect delay and power consumption issues [4]. The employment of the third dimension provides higher device density and smaller chip area in 3D ICs [5]. Also, 3D integration may be used either to partition a single chip into multiple strata to reduce on-chip global interconnects length and/or to stack chips that are homogeneous or heterogeneous [6].

To practically implement and fully exploit the 3D integration of electronic systems, the accompanying thermal issues need to be addressed. By stacking active device layers, the heat dissipation

rates per unit volume and per unit horizontal footprint area are proportionally increased. Also, the interior layers of the 3D structure are thermally removed from the heat sink [7]. Heat transfer is further restricted by the low thermal conductivity bonding interfaces and thermal obstacles in multiple IC layers. Moreover, the inherent spatial nonuniformity of the power/heat flux distribution/dissipation within each active layer generates hot-spots of localized intense power dissipation, which yields a spot temperature increase, degrading the functionality of circuits and creating thermal stress issues due to nonuniform thermal expansion. In particular, high temperatures brought by local hot-spots and/or excessive power consumption cause degradation of carrier mobility and escalated leakage power [8].

Thus, thermal design in sub-100 nm IC technologies has been one of the major challenges to the IC computer-aided design (CAD) community [9]. Also, the thermal management solutions cost 1–3 USD or more per watt of heat dissipated for high-performance processors [10,11]. Consequently, power—as well as temperature—aware microprocessor design, modeling and implementation, which include spatially nonuniform power distribution, have been substantially explored for planar (2D) ICs [8,9,12–15]. Among pioneering efforts, Kleiner et al. [16] performed the thermal analysis on the vertically integrated circuits (VICs) and showed that the silicon thickness of the upper chip layers is a crucial parameter in determining the thermal performance of VICs. Rahman and Reif [17] conducted the 3D system-level modeling of power dissipation, and analytical and numerical modeling of device-level and package-level heat removal. Loi et al. [18] studied the benefits of 3D technology under the influence of ther-

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mal constraints using a processor-cache-memory system, and the performance of 3D architecture was compared with a conventional planar (2D) design.

Several kinds of advanced cooling technologies also have been presented such as microjet impingement [19,20], compact thermosyphon [21], loop heat pipe [22], electro-osmotically pumped loop [23], stacked microchannel heat sink [24], thermoelectric micro-cooler [25], miniature vapor compression heat pump [26], and miniature absorption heat pump [27]. However, such cooling solutions for 2D planar circuits do not translate readily to 3D stack, with the limited surface area available for thermal management, and the large vertical thermal resistance between the bottom layer and the heat sink of 3D integrated circuits. Koo et al. [28] conducted thermal analysis for integrated interlayer microchannel cooling for a 3D electronic circuit architecture and indicated that a layer of integrated microchannel cooling can remove heat densities up to 135 W/cm^2 within a 3D architecture with a maximum circuit temperature of 85°C . This study considered the vertical (i.e., for different device layers) nonuniformity of power distribution and resulting thermal couplings, but assumed a uniform power distribution within each layer. However, in-plane nonuniformity of power distribution and hot-spots will bring much higher local surface temperatures than predicted by the above mentioned calculations. Brunschweiler et al. [29] experimentally characterized the capability of area-interconnect-compatible interlayer cooling in vertically integrated high-performance chip stacks, in which several types of heat transfer structures have been explored. A maximum heat removal capability of 537 W/cm^2 with 60 kPa of pressure drop was measured with de-ionized water as a single-phase working fluid. Sekar et al. [30] and Bakir et al. [31] proposed a cooling solution for 3D ICs, which features the use of microchannel heat sink in each stratum of the 3D stack and the use of wafer-level batch fabricated electrical and fluidic chip input/output (I/O) interconnects. Lee et al. [6] considered the routing with multifunctional interconnects, including through-silicon vias (TSVs) for signal, thermal, and power distribution networks in 3D ICs and demonstrated the methodology to account for various physical (space), electrical, and thermomechanical requirements.

In summary, thermal management in 3D has emerged as one of the key enabling technologies for the practical implementation of 3D integration of ICs. Thermal performance of the 3D circuit architectures remains a critical bottleneck, and further investigation of different cooling schemes and associated performance improvement is needed. In this work, the integrated interlayer microfluidic cooling scheme is adopted and numerically investigated. Using the model, the effects of the cooling mode (i.e., single-phase versus two-phase convective cooling) and geometry variation on the cooling performance are quantitatively analyzed, yielding an insight and guidance on the TSV scaling and electrical interconnect congestion. The heat transfer and pressure drop performance of the two modes are evaluated and compared. Lastly, the significance of planar nonuniformity of power distribution resulting in a presence of spatially distributed hot-spots is discussed.

2 3D-Stacked IC and Nonuniform Power Map

Figure 1 shows the spatial heat flux distribution, or power map, of the 45 nm Intel Core 2 Duo processor code-named Penryn [32], in which the two cores are mirror images of each other right below the L2 cache. To create this map, a publicly released die photo of the Penryn was examined and the floor plan was generated [33]. The total power of each core and L2 cache are 43.1 W and 4.32 W , respectively. The power density of L2 cache region is 11.3 W/cm^2 , which is negligibly small compared with the maximum power density value 305 W/cm^2 .

Each active layer in Fig. 2 consists of a single Penryn core on which a single L2 cache is stacked. The four-tier IC structure was designed to simulate a hypothetical 3D quad-core processor by

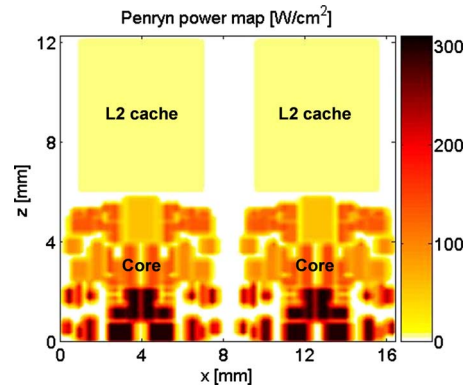


Fig. 1 Power map: Intel Core 2 Duo processor—Penryn

stacking the four active layers integrated with intermediate metal-oxide isolation layers. Microfluidic channel layer capped with polymer Avatrel cover, as illustrated in Fig. 2, are integrated for thermal management of each high-power processor tier. While the active layers are the main power consuming layers, heat is also generated in the metal-oxide layers due to Joule heating. The microfluidic channels are capped with thin polymer (Avatrel 2000 P) coatings ($\sim 30 \mu\text{m}$) [34]. The thicknesses of the Avatrel cover and the metal-oxide layers are set to be $10 \mu\text{m}$ and $6 \mu\text{m}$, respectively. The dimensions of $100 \mu\text{m}$, $200 \mu\text{m}$, $50 \mu\text{m}$, and $50 \mu\text{m}$ are taken for the baseline channel depth, width, side-wall thickness, and base thickness. Unless specifically noted, all of the calculations reported have been conducted for the baseline geometry described above. Only for the performance comparison in Sec. 4.4 and Table 3, the physical dimensions of the microfluidic channels are parametrically varied within the ranges listed in Table 1. The numbers in the parenthesis are the corresponding numbers of microfluidic channels.

3 Model Description

The thermal model of Koo et al. [28] is enhanced to deal with the three-dimensional thermal transport including the lateral temperature and fluid flow rate distribution due to nonuniform power/heat flux distribution. Figure 3 shows the cross-sectional view of the 3D-stacked IC with embedded microfluidic channels. It is assumed that the temperatures of the fluid and the solid domains (including the side-wall, base, Avatrel cover, and the oxide layer) are different but uniform at each cross section within each control volume. In reality, the temperature of the Avatrel cover and the oxide-metal layer will be slightly different from that of the silicon structure. However, these layers are very thin ($< 10 \mu\text{m}$) so that the temperature differences across these layers are insignificant even with the low thermal conductivity ($\sim 10 \text{ W/m K}$). Thus, the

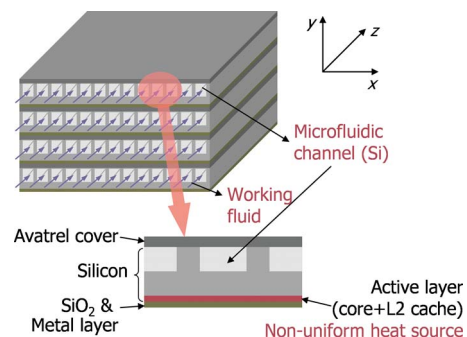


Fig. 2 3D-stacked ICs integrated with microfluidic channels for thermal management

Table 1 Physical dimensions of 3D-stacked IC and microfluidic channel. (The numbers in the parenthesis are the corresponding numbers of microfluidic channels with a single-pass channel configuration. For dual-pass, the number of channels is doubled.)

| Description | Values (*: baseline) |
|---|--|
| Channel depth (μm) | 50, 100*, 150, 200 |
| Channel width (μm) | 150 (40), 200*(32), 300 (22), 400 (17) |
| Channel side-wall thickness (μm) | 25 (35), 50*(32), 100 (26), 150 (22) |
| Channel base thickness (μm) | 25, 50*, 75, 100 |
| Avatrel cover (μm) | 0, 10* |
| Oxide layer (μm) | 6 |
| Channel length (mm) | 6 |
| Channel total width (mm) | 8 |

silicon structure temperature (T_w) can be reasonably considered as the representative temperature of the control volume without any destructive influences on the thermal behaviors of the silicon structures. Also, the horizontal thermal resistances of these layers are usually more than 100 times higher compared with those of silicon structures due to the low thermal conductivity and the thin layer; the horizontal direction heat transfers through these layers are negligibly small. Thermal and fluid flow in microfluidic channels are described by the following energy and momentum conservation equations:

$$\dot{m} \frac{di}{dz} = \eta_o h_{\text{conv}} \tilde{P}(T_{w,j} - T_{f,j}) + h_{\text{conv}} w (T_{w,j+1} - T_{f,j}) \quad (1)$$

$$-\frac{dP}{dz} \Big|_{\text{sp}} = \frac{2fG^2}{d_h \rho} \quad (\text{for single-phase flow}) \quad (2a)$$

$$-\frac{dP}{dz} \Big|_{\text{tp}} = \left(\frac{2f_j G(1-x_v)}{d_h \rho_l} \right) \phi_l^2 + G \frac{d}{dz} \left(\frac{x_v^2}{\varepsilon \rho_v} + \frac{(1-x_v)^2}{(1-\varepsilon)\rho_l} \right) \quad (\text{for two-phase flow}) \quad (2b)$$

$$\frac{\partial}{\partial x} \left(k_w \frac{\partial T_w}{\partial x} \right) + \frac{\partial}{\partial y} \left(k_w \frac{\partial T_w}{\partial y} \right) + \frac{\partial}{\partial z} \left(k_w \frac{\partial T_w}{\partial z} \right) + \dot{q}_g + \dot{q}_{\text{conv}} = 0 \quad (3)$$

where T_w and T_f represent the temperatures of solid and fluid, respectively, and \dot{m} , i , and h_{conv} are mass flow rate, enthalpy, and convective heat transfer coefficient, respectively. For each microfluidic channel, heat is supplied only to the channel base, and the channel side-wall is analyzed as a fin attached to the base (η_o is the overall surface efficiency, including an array of fins and the base surface). The microchannel geometry is described by the

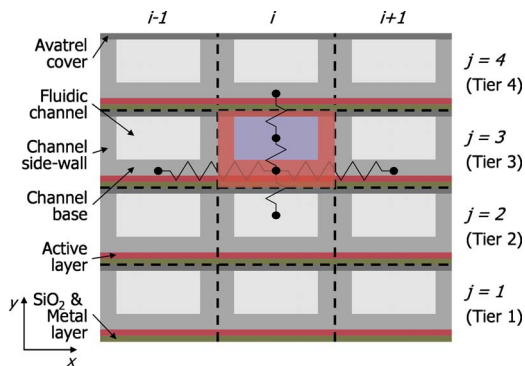


Fig. 3 Cross-sectional grids for thermal analysis of the 3D-stacked IC integrated with microfluidic liquid cooling channels

channel perimeter \tilde{P} and width w . Equation (3) is the three-dimensional thermal transport equation for the solid, consisting of Si. It has two source/sink terms owing to heat generated from the active and metal-oxide layers and convective heat transfer to the fluid.

Equation (1) represents the fluid enthalpy change due to the convective heat transfer owing to the temperature difference between the solid and fluid. The two terms on the right-hand-side of Eq. (1) does account for the vertical (across the stack) thermal coupling between the layers, which in essence specify the thermal resistances between each fluid-filled channel in a given chip layer and the walls above and below it. Since these interlayer walls are shared between the different layers in the stack, it provides thermal coupling between the layers and is equivalent to an interface condition between the layers that would be used in a more general 3D formulation of the problem. A general correlation of Garimella et al. [35] is adopted in this study for evaluating single-phase convective heat transfer coefficients for fully developed as well as simultaneously thermally-hydraulically developing flow regions in the rectangular channel. The correlation covers laminar and turbulent flow having Reynolds numbers ranging from 118 to 10,671, Prandtl numbers from 6.48 to 16.20, and bulk-to-wall property variations (μ_b/μ_w) from 0.243 to 0.630.

Several correlations for two-phase heat transfer coefficients have been proposed for small channels and/or microchannels [36–41]. The boiling number $\text{Bo} = q''/G\lambda$ allows one to determine the quality at which the transition from nucleate-boiling-dominated to convective-boiling-dominated heat transfer occurs [36]. Lazarek and Black [36] suggested that the occurrence of nucleate-boiling-dominated heat transfer all the way up to CHF could be attributed to the high (above 5×10^{-4}) Boiling numbers of their data. Lin et al. [42] observed that for heat fluxes greater than $\sim 60 \text{ kW/m}^2$, the heat transfer coefficient decreases as vapor quality increases, which suggests that nucleate boiling is the dominant heat transfer mechanism, regardless of vapor quality at these heat fluxes. For these conditions, the heat transfer coefficient is almost constant or slightly decreases, as the vapor quality increases. Since the Boiling number in this study ranges from 4×10^{-4} to 2×10^{-3} , nucleate boiling is the dominant heat transfer mechanism. Therefore, an enhancement of heat transfer in two-phase flow due to convection, which increases with increasing vapor quality, is largely suppressed so that the heat transfer coefficient is fairly independent of vapor quality change. The model of Tran et al. [37] suggests that nucleate boiling is a dominant two-phase heat transfer mechanism. The present study adopts the model of Yu et al. [40], who modified the model of Tran et al. [37].

The single-phase pressure drop along the microfluidic channel is obtained from the fluid momentum balance Eq. (2a), wherein P , G , and ρ are pressure, mass flux, and density of the fluid, respectively. A fanning friction factor for laminar flow in a rectangular channel and Blasius equation [43]. for turbulent flow were adopted according to the following equations:

$$f_{\text{lam}} \text{Re} = 24(1 - 1.3553\beta + 1.9467\beta^2 - 1.7012\beta^3 + 0.9564\beta^4 - 0.2537\beta^5) \quad (4a)$$

$$f_{\text{tub}} = 0.079 \frac{1}{\text{Re}^{0.25}} \quad (4b)$$

For two-phase pressure drop, a separate model with a two-phase multiplier is used in Eq. (2b). Lee and Mudawar [44] proposed a correlation for the C value, which appeared in the classical two-phase multiplier correlation of Lockhart and Martinelli [45]. The void fraction ε can be calculated using the model of Zivi [46].

De-ionized water is considered as a working fluid for single-phase cooling. For two-phase cooling, several refrigerants have been explored as listed in Table 2, with their critical pressures and saturation pressure ranges corresponding to the temperatures

Table 2 Tested refrigerants with their critical pressures and saturation pressures

| Refrigerants | P_{crit} (kPa) | P_{sat} ($T_{sat}: 30-70^\circ\text{C}$) (kPa) |
|--------------|------------------|--|
| Water | 22,059 | 4-31 |
| R134a | 4059 | 771-2117 |
| R113 | 3392 | 54-201 |
| R236ea | 3502 | 244-784 |
| R227ea | 2929 | 527-1486 |
| R245ca | 3925 | 122-436 |
| R123 | 3662 | 110-377 |

range of 10–70 °C. Equations (1), (2a), (2b), and (3) are numerically integrated over a control volume and then discretized using the upwind scheme [47]. The resulting system of linear algebraic equations is iteratively solved using the successive under relaxation (SUR) method. The thermophysical properties of water and the refrigerants are determined using REFPROP 6.0 software [48]. The inlet fluid temperature for the single-phase cooling was set at 30 °C at atmospheric pressure. For two-phase cooling, all the working fluids enter the microfluidic channels at saturated liquid state ($x_{v,in}=0$). The corresponding saturation temperatures are set as 50 °C for the refrigerants R134a, R236ea, R227ea, R245ca, and R123 whereas for water and R113 saturation temperature of 70 °C is required due to their small hydraulic budgets as listed in Table 2. Due to single inlet and exit ports for all microfluidic channels in the layer, the pressure drop from the inlet to the outlet of each microfluidic channel is fixed at 30 kPa and 50 kPa, for single-phase and two-phase cooling, respectively. Note that for two-phase cooling with water as working fluid, fixed pressure drop of 20 kPa was imposed considering the saturation pressure of 31.2 kPa at 70 °C. It is assumed that the inlet and outlet pressure heads do not affect the mass flow rate maldistribution.

4 Results and Discussion

4.1 Model Validation. Zhang et al. [49] conducted an experimental study on the single-phase and two-phase convective flow with single-channel and multichannel microstructures. The multichannel design consists of 2 cm-long 40 microfluidic channels, 20 μm-wide and 70 μm-deep ($d_h=31 \mu\text{m}$). Due to the lateral heat loss, as well as the size mismatch between the attached heater and the microfluidic channel, the heat flux is nonuniformly distributed. In Figs. 4(a)–4(c) the measured pressure drops (Fig.

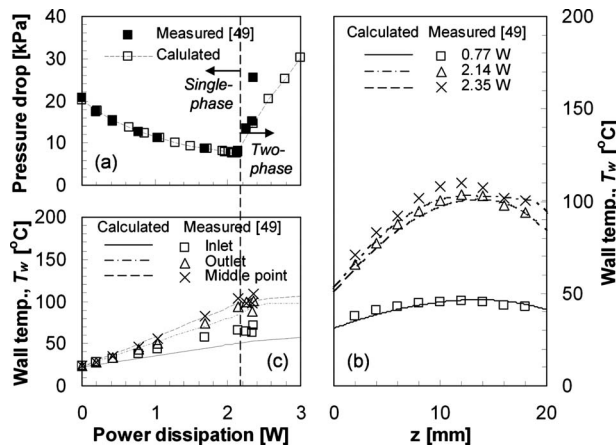


Fig. 4 Comparisons of calculated (a) pressure drop, (b) wall temperature distribution, and (c) local wall temperatures with the experimental data of Zhang et al. [49] for a microfluidic channel heat sink

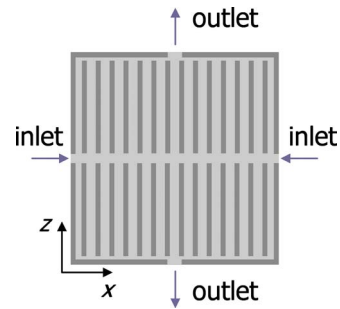


Fig. 5 Dual-pass microfluidic channel heat sink

4(a)), wall temperature distributions (Fig. 4(b)), and local wall temperatures (Fig. 4(c)) captured from Zhang et al. [49] are compared with the calculated data using the present model. Both the pressure drop changes with respect to power dissipation in Fig. 4(a), and the wall temperature distributions in Fig. 4(b) are in very good agreement except the last data point (power dissipation 2.35 W), for which the measured pressure drop was unexpectedly higher. The middle point and the outlet local wall temperatures in Fig. 4(c) were also well predicted, whereas the inlet local wall temperatures were slightly underpredicted. Zhang et al. [49] reported that their microstructures had significant heat loss up to 39% of applied heat power with 20% lost to preheating of inlet water. Since the inlet heat loss information was not available in detail, the inlet heat loss seems to be overestimated in this study.

4.2 Dual-Pass Microfluidic Channel Heat Exchanger.

Kandlikar and Upadhye [50] presented a novel microchannel heat exchanger for single-phase flow, which has a split-flow arrangement (dual-pass), as depicted in Fig. 5. By providing dual-pass for refrigerant flow inside microchannels, both the flow length and the mass flux of each microchannel are reduced by half so that the pressure drop can be significantly (roughly by one-fourth) reduced. However, the thermal performance of dual-pass microfluidic channel, with single-phase flow, seems to be slightly inferior to that of single-pass microfluidic channel, as observed in Figs. 6(a) and 6(b). As aforementioned, in the comparison in Figs. 6(a) and 6(b), the total pressure drop through the channel was fixed at 30 kPa. The wall temperature at the strongest hot-spot was slightly increased from 60.07 °C to 60.97 °C by adopting the dual-pass configuration. It should be, however, noted that most of the hot-spots are located in the lower part of the power map so that most of the dissipated heat (90% of total power) from the Penryn core was imposed on the bottom set of channels, whereas the top channels have been largely unutilized. As expected, the mass flow rate for the tier 1 was augmented from 2.1 g/s to 7.1 g/s due to the aforementioned feature of dual-pass configuration, which made the thermal performance of the half length microfluidic channel comparable to that of full length microfluidic channel. For two-phase flow, the dual-pass configuration featured slight improvement in hot-spot temperatures as observed in Figs. 7(a) and 7(b).

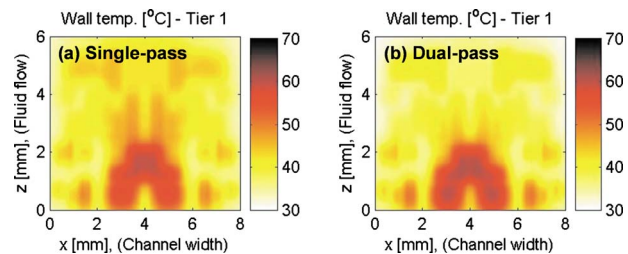


Fig. 6 Wall temperature distributions of the tier 1 with single-phase (a) single-pass microfluidic channel cooling and (b) dual-pass microfluidic channel cooling

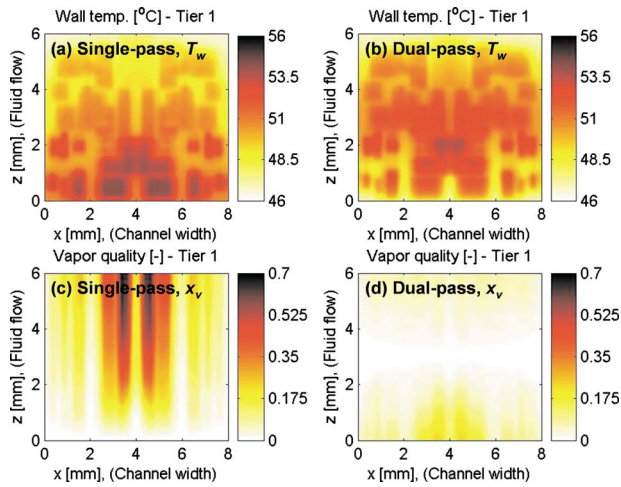


Fig. 7 Wall temperature and vapor quality distributions of the tier 1 with two-phase (a and c) single-pass microfluidic channel cooling and (b and d) dual-pass microfluidic channel cooling using R236ea as a working fluid

The highest hot-spot temperature was 54.29°C and 53.78°C for single-pass and dual-pass configurations, respectively. It should be noted that due to the pressure drop, microfluidic channel has the lowest fluid temperature at the outlet as long as the fluid flow is in two-phase throughout the microfluidic channels. Therefore, the strength of the hot-spot located in the lowest part (0 mm < z < 1 mm) in Fig. 7(a) is suppressed in Fig. 7(b). Under the uniform pressure drop of 50 kPa with R236ea coolant, dual-pass microfluidic microchannel heat exchanger offered increased mass flow rate of 7.3 g/s for tier 1, which is about four times the single-pass configuration mass flow rate, 2.0 g/s. Consequently, vapor quality distribution in Figs. 7(c) and 7(d) indicate that the dual-pass configuration allowed more refrigerant to flow through microfluidic channels so that the outlet vapor qualities were much lower than those in single-pass configuration. The vapor quality is a very important parameter to determine the reliability of the thermal management system. Since at sufficiently high vapor quality, dry-out (or partial dry-out) can occur, and the channel will suffer from a lack of liquid-phase to cool the chip. The chip temperature will be drastically increased due to the poor heat transfer coefficient of refrigerant vapor. Thus, Figs. 7(c) and 7(d) suggest that the dual-pass configuration offers significantly enhanced reliability.

The drawback of the dual-pass configuration is the larger pumping power consumption. The total pumping power with the dual-pass configuration was 1.23 W, whereas with the conventional single-pass configuration it was only 0.36 W. However, the pumping powers are negligibly small compared with the total power (189.68 W) generated by the stacked chips. The comparison of pumping power between the configurations is thus not very meaningful; the pumping power budget is still abundant. If the thermal performance could be enhanced, higher pumping power would be needed to pump the coolant at sufficiently high flow rates.

4.3 Nonuniform Heat Flux. The total power generated from the nonuniform power map of all four tiers is ~190 W. Assuming a uniform power dissipation map, with the same total power, yields the power density (heat flux) of ~100 W/cm² that would result in the highest wall temperature of ~43°C. Meanwhile, the highest temperature observed in Fig. 8 is ~61°C. This means that the about 20°C of the wall temperature difference between the two simulated cases should be attributed to the in-plane nonuniformity of the power density, known as the hot spots. The fluid temperature difference was around 5°C, which brought about a variation in the fluid properties, such as density and viscosity and,

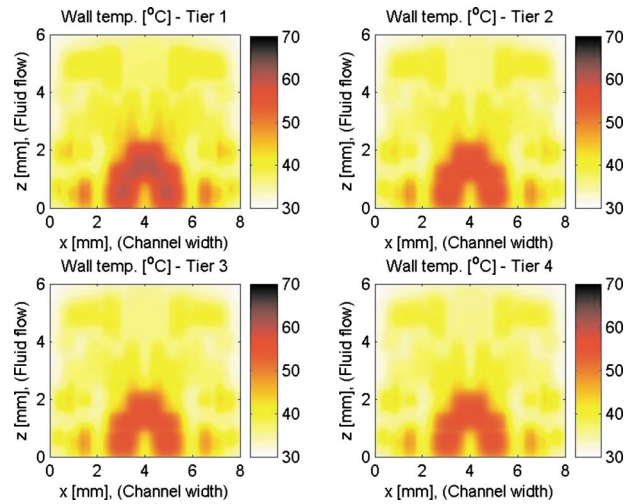


Fig. 8 Wall temperature distributions with single-phase dual-pass microfluidic channel cooling

in turn, channel-by-channel maldistribution of the mass flow rate. Figure 9(a) shows that the microfluidic channels in the hot-spot region have higher mass flow rates, which is consistent with the results of Zhang et al. [49] plotted in Fig. 4(a). Given that G is constant, from Eqs. (2a) and (4), the single-phase pressure drop scales as $\Delta P_{sp} \sim \mu^a \rho^{-1}$ ($a=1$ for laminar, $a=0.25$ for turbulent flow). When the water temperature changes from 29°C to 34°C, both the viscosity and density decrease, but the density change is negligibly small. Thus, the reduced viscosity at the elevated fluid temperature should result in a smaller pressure drop. Under the fixed pressure drop condition, the viscosity reduction will reciprocally induce a higher flow rate through the microfluidic channels in the hot-spot region. This improves thermal performance of the single-phase microfluidic channel, and facilitates hot-spot temperature suppression because higher flow rate usually provides higher heat transfer coefficient.

Although the same power density and floor plan are imposed on each tier, vertical wall temperature differences and distribution are observed in Fig. 8. This is because the first tier thermal management only depends on the microfluidic channel above it, while the other tiers have double-sided cooling, as shown in Fig. 3. Also, tier 4 does not share the cooling power of microfluidic channel heat exchanger above it with other tiers. Therefore, tier 4 has the lowest maximum wall temperature, which is reduced by 5°C rela-

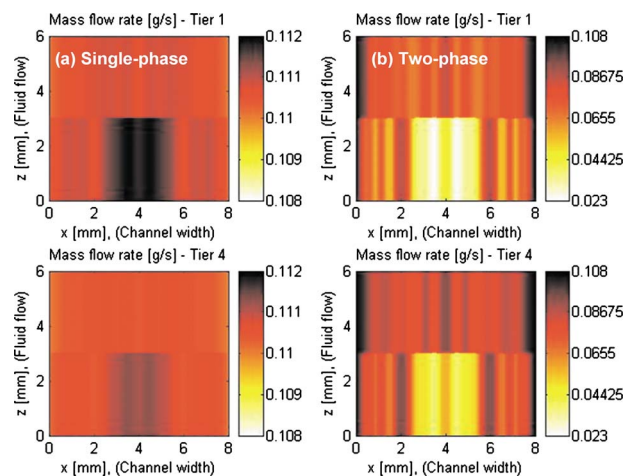


Fig. 9 Mass flow rate distributions for (a) single-phase and (b) two-phase (R123) dual-pass microfluidic channel cooling

Table 3 Single-phase dual-pass microfluidic channel cooling performance with respect to channel geometry variations

| Description | $T_{w,max}$ (°C) | $T_{f,max}$ (°C) | \dot{m} (g/s) | W_p (W) |
|---------------------|---------------------|---------------------|--------------------|--------------|
| $d=50 \mu\text{m}$ | 77.92 | 45.67 | 6.03 | 0.19 |
| $d=100 \mu\text{m}$ | 60.97 | 33.66 | 28.36 | 0.91 |
| $d=150 \mu\text{m}$ | 54.14 | 31.77 | 59.07 | 1.89 |
| $d=200 \mu\text{m}$ | 51.32 | 31.11 | 94.81 | 3.03 |
| $w=150 \mu\text{m}$ | 60.85 | 34.28 | 23.92 | 0.76 |
| $w=200 \mu\text{m}$ | 60.97 | 33.64 | 28.36 | 0.91 |
| $w=300 \mu\text{m}$ | 62.01 | 33.09 | 32.96 | 1.08 |
| $w=400 \mu\text{m}$ | 63.35 | 32.80 | 36.45 | 1.23 |
| $s=25 \mu\text{m}$ | 59.37 | 33.38 | 30.99 | 0.99 |
| $s=50 \mu\text{m}$ | 60.97 | 33.64 | 28.36 | 0.91 |
| $s=100 \mu\text{m}$ | 65.29 | 34.24 | 23.07 | 0.75 |
| $s=150 \mu\text{m}$ | 69.07 | 34.75 | 19.55 | 0.64 |
| $b=25 \mu\text{m}$ | 63.01 | 33.81 | 28.36 | 0.91 |
| $b=50 \mu\text{m}$ | 60.97 | 33.64 | 28.36 | 0.91 |
| $b=75 \mu\text{m}$ | 59.56 | 33.53 | 28.36 | 0.91 |
| $b=100 \mu\text{m}$ | 58.47 | 33.44 | 28.36 | 0.91 |

tive to the maximum wall temperature of tier 1. This suggests placing higher power chip close to tier 4 for improved thermal performance. When tiers 3 and 4 are inactive and only tiers 1 and 2 are active, the observed highest wall temperature was 53.4°C. With the reversed operation (i.e., tiers 3 and 4 are active, while tiers 1 and 2 are inactive), the highest wall temperature rose to 58.0°C. This implies an existence of between the layer flow maldistribution. Indeed, the mass flow rate distribution in different layers of a 3D stack is shown in Fig. 9(a) with significant nonuniformity between the cooling layers. The maximum mass flow rates in tier 1 and tier 4 are 0.1119 g/s and 0.1113 g/s (per channel), respectively, which are passing through the hot-spot region. However, the effects on the total mass flow rates were insignificant; total mass flow rates through tier 1 and tier 4 are 7.10 g/s and 7.08 g/s, respectively.

4.4 Microfluidic Channel Geometry. The on-chip thermofluidic network is composed of fluidic TSVs and microfluidic channels. It is assumed that all the fluidic TSVs are located outside the region where all the gates and metal wiring are distributed. Thus, only microfluidic channels are considered for routing requirement analysis. Since microfluidic channels are fabricated on the back side of a silicon die, they do not affect routing capability on metal layers. However, these channels obstruct TSV connections. Due to their large size, the microfluidic channels decrease the routing capacity of TSVs quite considerably. In fact, the scarcest resource is usually the signal TSV capacity. Due to the microfluidic channels placement, many routing tiles have no capacity left for signal TSVs [6]. Therefore, the microfluidic cooling channels compete with wire routability for space.

The effect of channel geometry variation on cooling system parameters and performance is summarized in Table 3. As the channel depth increases, the microfluidic channel gains more mass

flow rate (under fixed pressure drop), which augments the heat transfer capability of the fluid. Also, since the fluid temperature rise is reduced by the increased mass flow rate, the wall and fluid temperatures can be further lowered. An increase in the channel depth from 50 μm to 200 μm reduced the hot-spot temperature by 26.6°C. However, in terms of TSV performance, shorter channel depth as well as TSV length are preferred. Lee et al. [6] reported that the reduced TSV signal length brought by the channel depth decrease from 100 μm to 50 μm increased the y -direction routing capacity, so that the y -direction routing tile usage has been 17.7%. An increase in the channel width also leads to the mass flow rate augmentation, but the number of microfluidic channels is, at the same time, reduced. Consequently, the total mass flow rate increment induced by the channel width increment is less than that by the channel depth increment. Also, the available surface area (per unit volume) for heat transfer between the fluid and the channel wall is reduced by 15%, as channel width increases from 150 μm to 400 μm . Hence, as shown in Table 3, the channel width increment has negative effect on the thermal performance, increasing the hot-spot temperature by 2.5°C.

Two heat transfer modes, convection and conduction, are incorporated by microfluidic channel cooling. Convective heat transfer occurs between the solid and the fluid dissipating the IC power to the fluid. Meanwhile, conductive heat spreading moderates hot-spots. Increases in the channel side-wall and/or base thickness improve the conductive heat transfer. However, Table 3 shows that the increment of the channel base thickness reduced the hot-spot temperature by 4.54°C, while the increment of the channel side-wall thickness leads to the increase in hot-spot temperature by 9.7°C. This is because the increment of the channel side-wall thickness diminishes the convective heat transfer capability by eliminating a total number of available microfluidic channels, while incrementing the channel base thickness effectively augments the conductive heat transfer, without any adverse effect on convection. However, for TSV routing capacity, a wider channel side-wall is preferred and the channel base thickness is limited by the allowable TSV length.

4.5 Two-Phase Cooling. For the baseline channel geometry, the calculated heat transfer coefficients for single-phase cooling were quite uniform at $\sim 5.0 \times 10^4 \text{ W/m}^2 \text{ K}$, while two-phase heat transfer coefficients ranged from $\sim 5.0 \times 10^4$ to $\sim 7.0 \times 10^5 \text{ W/m}^2 \text{ K}$, with the average value of $3.5 \times 10^5 \text{ W/m}^2 \text{ K}$ using R134a as a working fluid. If 10°C of driving temperature difference is taken, the two-phase cooling can, roughly, deal with the power density of 350 W/cm^2 , whereas a single-phase cooling capability is limited to 50 W/cm^2 . Moreover, single-phase flow has an additional penalty due to coolant temperature increase along the channel caused by the sensible heat transfer. The inlet fluid temperature, therefore, should be much lower in a single-phase flow, which requires larger cooling load at the air-side heat exchanger (or condenser) in the system. Thus, the higher heat transfer coefficient and a relatively constant fluid temperature indicate a better thermal performance of a two-phase cooling system.

The two-phase cooling results are summarized in Table 4. Most

Table 4 Two-phase dual-pass microfluidic channel cooling performance

| Refrigerants | $T_{w,max}$ (°C) | \dot{m} (g/s) | W_p (W) | $x_{v,max}$ | $h_{conv,max}$ ($\text{W/m}^2 \text{ K}$) |
|--------------|---------------------|--------------------|--------------|-------------|--|
| Water | 135.50 | 2.11 | 0.048 | 0.999 | 28,316 |
| R134a | 52.92 | 45.32 | 2.215 | 0.109 | 726,630 |
| R113 | 74.69 | 16.56 | 0.626 | 0.874 | 382,470 |
| R236ea | 53.78 | 30.39 | 1.229 | 0.234 | 499,420 |
| R227ea | 52.26 | 39.58 | 1.685 | 0.227 | 921,210 |
| R245ca | 55.38 | 19.60 | 0.807 | 0.329 | 328,970 |
| R123 | 55.03 | 18.26 | 0.715 | 0.519 | 354,000 |

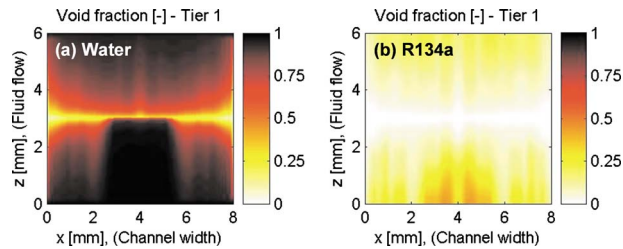


Fig. 10 Void fraction distributions of the coolant in the tier 1 with two-phase dual-pass microfluidic channel cooling using (a) water and (b) R134a as working fluids

of the refrigerants successfully kept the wall temperatures well below 85°C with the difference between maximum wall and inlet fluid temperatures only $2\text{--}5^{\circ}\text{C}$, which is significantly smaller than that for single-phase cooling. Considering that pumping power is comparable and inlet fluid temperatures are much higher, two-phase cooling seems to be very promising, as compared with single-phase. However, the channel interior pressures of R134a and R227ea yielding the best performance among the refrigerants are around 1300 kPa and 900 kPa , respectively, which are too high to be safely maintained in the thin silicon structure. On the other hand, the saturation pressure of water is sufficiently low to be allowable. However, the thermal performance of water shown in Table 4 was poor, due to its hydraulic properties providing exceptionally small mass flow rate through the channels. The saturation pressure of water at 70°C is only 31.2 kPa , which is very close to its triple point. The augmentation of flow rate for the increment of cooling capability could make the water easily reach its triple point and thus cause blockage of channel with ice; thus, the two-phase water cooling suffers from the lack of “hydraulic budget.” Besides, the proximity of the water saturation pressure to its triple point further degrades its thermal capability by considerably amplifying the two-phase flow pressure drop. As shown in void fraction model by Zivi $\varepsilon = [1 + (1/x_v - 1)(\rho_v/\rho_l)^{2/3}]^{-1}$ [46], void fraction is determined by vapor quality and vapor-phase and liquid-phase density ratio ρ_v/ρ_l . At the saturation pressures near the triple point $\rho_v/\rho_l \rightarrow 0$, which makes $\varepsilon \sim 1$ even with low vapor quality. In fact, the two-phase multiplier is strongly related to void fraction. For annular flow, the two-phase multiplier can be approximated by $\phi_l^2 \sim (1 - \varepsilon)^{-2}$ [51], which implies low void fraction of water due to the proximity to its triple point, leading to a large two-phase multiplier. The additional pressure drop due to the liquid-vapor interaction during two-phase flow is, therefore, larger for water as a working fluid.

Figures 10(a) and 10(b) compare the void fraction distributions of water and R134a. At the vapor quality of ~ 0.11 , the void fraction approaches 0.97, which means most of the channels were already filled with water vapor. The corresponding void fraction for R134a was only 0.44. These result in the two-phase pressure drop multipliers of $\phi_l^2 = 18.5$ and 2.35 for water and R134a, respectively. Also, the accelerational pressure drop, the second term of the right-hand side of Eq. (2b), strongly depends on the vapor-phase and liquid-phase densities and increases with increasing density difference between the phases, which is one of the indications of proximity to its triple point. Thus, poor thermohydraulic characteristics, such as the low hydraulic budget and a severe pressure drop in two-phase flow, which were mainly attributed to its proximity to triple point, considerably reduced the cooling capability of water and resulted in the maximum wall temperature of 135.5°C , well beyond an allowable limit of 85°C for the ICs.

The proximity of the saturation pressure to its critical point can be represented by reduced pressure $P_r = P_{\text{in}}/P_{\text{crit}}$, which is a “distance” of the saturation pressure from its critical point where the property differences between liquid and vapor phases vanish. In Fig. 11, the dependences of mass flow rates and maximum heat

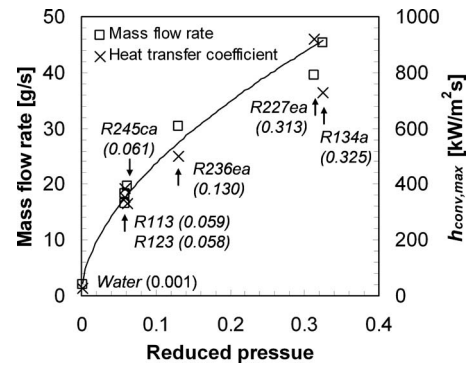


Fig. 11 Dependences of mass flow rates and maximum heat transfer coefficients on the reduced pressure. (The numbers in the parenthesis are the corresponding reduced pressures of each working fluid.)

transfer coefficients of refrigerants on the reduced pressure of the fluid in the microfluidic channel inlet are depicted. It is clear that the mass flow rate strongly depends on the reduced pressure, regardless of refrigerant. Interestingly, the maximum heat transfer coefficients clearly follow the curve fitting the mass flow rate data, which indicates that the thermal performance is also dominantly determined by the reduced pressure. Considering that the reduced pressure generally dictates the hydraulic budget as well as the pressure drop potential, Fig. 11 shows that the pressure drop in channels is a significant limiting factor, which mainly results from the small channel hydraulic diameter. Also, it is obvious that the reduced pressure can be used as a valuable indicator to determine a refrigerant compatibility to two-phase microfluidic channel cooling. Based on these results, R245ca and R123 can be considered as viable working fluids for two-phase microfluidic cooling system. Although R113 shows similar thermal performance, its use has been prohibited by the Kyoto protocol.

Mass flow rate maldistribution can be observed in Fig. 9(b) for R123 refrigerant. Compared with the single-phase case in Fig. 9(a), the maldistribution was more severe in two-phase flow. Moreover, fluid flow rate was significantly reduced in the hot-spot region. In tier 1, the maximum mass flow rate was 0.104 g/s (per channel), which was reduced to 0.024 g/s in the channel passing through the hot-spot region. The vertical flow rate distribution was also observed. The total mass flow rate supplied to tier 1 and tier 4 were 4.3 g/s and 4.9 g/s , respectively, and the maximum and minimum mass flow rates (per channel) in tier 4 were 0.105 g/s and 0.038 g/s , respectively. As previously mentioned, the two-phase multiplier and the accelerational pressure drop increase with increasing vapor quality. The fluid passing through the channels above the hot-spot region absorbs more heat from the chip and thus more vapor is generated. Consequently, the mass flow rate decreases under the fixed pressure drop condition due to an increased flow resistance by the generated vapor. This is a positive feedback loop, in which the reduction in mass flow rate and increase in vapor quality enhance each other, ultimately leading to the failure of the cooling system. Therefore, the negative effect of the mass flow rate maldistribution is much more amplified than may be intuitively expected. Indeed, as shown in Fig. 12, only 50% reduction in the power dissipation resulted in around 90% of vapor quality reduction. Thus, although some of the two-phase refrigerant, namely R123 and R245ca, performed satisfactorily with the hot-spot fluxes of $\sim 300\text{ W/cm}^2$, all liquid coolants may potentially suffer from a lack of coolant delivery to the hot-spots up to 1 kW/cm^2 as expected in the future 3D ICs. Further studies on the hot-spot management technique and cooling integration schemes [52–54] should greatly improve performance of conventional two-phase thermal management systems.

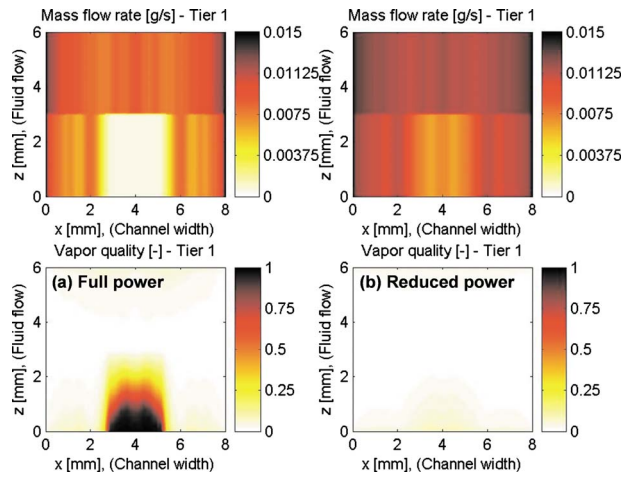


Fig. 12 Mass flow rate and vapor quality distributions for two-phase, dual-pass microfluidic channel cooling using water as a working fluid: (a) full power map and (b) 50% reduced power map

5 Conclusion

In the present study, we have numerically investigated the performance of interlayer microfluidic channel cooling for 3D-stacked ICs. Both in-plane, as well as, vertical nonuniformity in heat flux for both single-phase and two-phase flow are examined. It is verified that the dual-pass heat exchanger greatly helps in augmenting the mass flow rate through microfluidic channels so that the outlet vapor quality can be reduced, and the reliability of the cooling system can be considerably enhanced in two-phase cooling. Parametric investigation showed that increases of channel depth and channel base thickness are useful in reducing the wall temperature. However, this is limited by the maximum length scale of TSVs. The effect of channel width change was found not to be significant. For improved thermal performance, it is better to keep the channel side-wall thickness small; however, wider spacing between channels offers more vertical direction routing capacity.

A two-phase cooling scheme provided enhanced thermal performance as compared with single-phase cooling due to the higher heat transfer coefficient and relatively constant fluid temperature. However, R134a and R227ea were not suitable for the chip cooling application, due to the resulting high interior pressures. Thermal performance of the two-phase water cooling was significantly degraded because of its poor hydraulic properties. In two-phase microfluidic channel cooling, pressure drop acted as the significant limiting factor. The reduced pressure can be a good indicator of refrigerant compatibility to two-phase microfluidic channel cooling. Mass flow rate maldistribution has been also observed. Due to the positive feedback between the mass flow rate reduction and a vapor quality increase, fluid flow avoids the channels passing through the hot-spot regions. In summary, R245ca and R123 were shown to be viable working fluids for two-phase cooling system, which performed satisfactorily in terms of reliability and showed superior performance to the single-phase cooling system. In general, however, dedicated hot-spot thermal management and the hybrid cooling schemes combining different cooling methods based on their power dissipation capability are expected to be the major drivers to improve the 3D IC cooling system performance by suppressing the mass flow rate maldistribution, maintaining temperature uniformity within the stack, and enhancing the reliability.

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Nomenclature

- Bo = boiling number, $q''/G\lambda$
- b = channel base thickness (m)
- c_p = specific heat (J/kg K)
- d = channel depth (m)
- d_h = channel hydraulic diameter (m)
- f = fanning friction factor
- G = mass flux ($\text{kg}/\text{m}^2 \text{ s}$)
- h_{conv} = convective heat transfer coefficient ($\text{W}/\text{m}^2 \text{ K}$)
- i = enthalpy (J/kg)
- k = thermal conductivity ($\text{W}/\text{m K}$)
- L = channel length (m)
- \dot{m} = mass flow rate (kg/s)
- Nu = Nusselt number, hd_h/k_f
- P = pressure (Pa)
- \tilde{P} = perimeter (m)
- Pr = Prandtl number, $\mu c_p/k$
- P_r = reduced pressure
- \dot{q}_{conv} = volumetric convective heat transfer rate (W/m^3)
- \dot{q}_g = volumetric heat generation rate (W/m^3)
- q'' = heat flux (W/m^2)
- Re = Reynolds number, Gd_h/μ
- s = channel side-wall thickness (m)
- T = temperature ($^\circ\text{C}$)
- We = Weber number, $G^2 d_h/\rho\sigma$
- W_p = pumping power (W)
- w = channel width (m)
- X = Martinelli parameter
- x, y, z = Cartesian coordinates (m)
- x_v = vapor quality

Greek Symbols

- β = channel aspect ratio
- ε = void fraction
- ϕ = two-phase multiplier
- η_o = overall heat transfer efficiency
- λ = latent heat (J/kg)
- μ = dynamic viscosity ($\text{kg}/\text{m s}$)
- ρ = density (m^3/kg)
- σ = surface tension (N/m)

Subscripts

- b = bulk
- crit = critical
- f = fluid
- fd = fully developed
- i, j, k = index corresponding to Cartesian coordinates $x, y,$ and $z,$ respectively
- in = inlet
- l = liquid-phase
- lam = laminar flow
- lo = liquid only in channel
- max = maximum
- sat = saturation
- sp = single-phase
- tp = two-phase
- tub = turbulent flow
- v = vapor-phase
- w = channel wall

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