Full-Chip Multiple TSV-to-TSV Coupling Extraction and Optimization in 3D ICs

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ABSTRACT

TSV-to-TSV coupling is a new parasitic element in 3D ICs and can become a significant source of signal integrity problem. Existing studies on its extraction, however, becomes highly inaccurate when handling more than two TSVs on full-chip scale. In this paper we investigate the multiple TSV-to-TSV coupling issue and propose an accurate model that can be efficiently used for full-chip extraction. Unlike the common belief that only the closest neighboring TSVs affect the victim, our study shows that non-neighboring aggressors also cause non-negligible impact. Based on this observation, we propose an effective method of reducing the overall coupling level in multiple TSV cases.

Categories and Subject Descriptors

B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms

Design

Keywords

3D IC, TSV, Coupling, TSV-to-TSV Coupling

1. INTRODUCTION

Through-silicon-via (TSV) and three-dimensional integrated circuits (3D ICs) are expected to be the key technology trend in high performance and low power systems. Industries are already designing 3D DRAMs using TSVs [6], and academia are reporting the impact of TSVs on 3D ICs in many studies [4].

One of the essential signal integrity (SI) characteristics in studying TSVs is coupling. Recognizing that the impact of the coupling of TSVs is non-negligible, many studies have reported methodologies for reducing TSV-to-TSV coupling [3] [5] [2]. However, these studies have mostly focused on the impact of TSV-to-TSV coupling on only single TSV-pair cases and not on multiple TSV-pair cases [5]. Studies have also focused on the analysis of multiple TSV coupling, but they only analyzed TSV arrays that were not on a full-chip level [2]. A study proposed a methodology that performs full-chip TSV-to-TSV coupling analysis [3], but the analysis may not have been accurate because the analytical model they used overestimated the coupling capacitance.

Therefore, in this paper, we study the multiple TSV-to-TSV coupling effect inside 3D ICs on a full-chip level. We describe the true phenomena that take place inside the ICs and propose a compact model that captures the coupling effect between multiple TSVs. Then, we propose a methodology that performs an analysis of multiple TSV coupling on a full-chip level. The main contributions of this work include the following: (1) A physical limit of the coupling capacitance: We prove that TSV-to-TSV coupling has a maximum capacitance limit. (2) Non-neighboring aggressor impact on TSV-to-TSV coupling: Unlike wire coupling, we show that TSV coupling is affected not only by the closest neighbor, but also by the non-neighboring aggressors. (3) A compact multiple TSV-to-TSV coupling model and extraction algorithm: To the best of the authors' knowledge, we propose the first compact multiple TSV-to-TSV coupling model and extraction algorithm that can be applied on a full-chip level. (4) TSV coupling optimization methodology: We propose a design optimization methodology that reduces TSV-to-TSV coupling in large-scale full-chip 3D IC designs.

2. MOTIVATION

In this section, we describe the motivation of our work and show our findings. We also show why [3] is inaccurate. In this paper, we use the TSVs of a radius of 2μm, a height of 60μm, a SiO_2 liner of 0.5 μm, and a minimum pitch of 10μm.

2.1 Maximum Coupling Capacitance

In [3], the authors assumed that silicon substrate capacitance depends only on the distance between two TSVs. We describe why this assumption is inaccurate. When a victim TSV is surrounded by more than one aggressor, the total coupling capacitance of the silicon substrate has a maximum limit and does not increase linearly.

Many TSV modeling papers [3] [5] claim that the silicon substrate capacitance follows Eq. 1, which is the capacitance between two parallel, circular conducting wires,

$$C_{\mathrm{si}} = \frac{\pi\epsilon_0\epsilon_{\mathrm{si}}L}{\ln[(P/2r) + \sqrt{(P/2r)^2 - 1}]} \quad (1)$$

in which, ϵ_{si}, L, P, and r are the permittivity of the silicon substrate, the height of the TSVs, the pitch between the TSVs, and the radius of the TSVs, respectively. By this equation, when the coupling capacitance between an aggressor and a victim in a certain pitch is 1x, the victim will see 8x coupling capacitance when there are eight aggressors in every direction.

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DAC'13, May 29 - June 07 2013, Austin, TX, USA.
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However, Eq. 1 is correct only when there are no other neighbors near the two TSVs. When TSV aggressors are close to another aggressor, the total substrate capacitance that a victim sees will increase but not linearly. Fig. 1 illustrates this concept when the radius is $2\mu m$ and the pitch between TSVs is $10\mu m$. We simulated the total coupling capacitance using Synopsys Raphael when different number of aggressors are near a victim TSV. Fig. 1 shows that although more TSVs are near the victim, the increase in total coupling capacitance is minor. For example, (d) has two more aggressors than (c), but the total capacitance increase is only 0.51x. For (e), four more aggressors are added than (d), but the capacitance increase is only 0.05x. From this study, we prove that Eq. 1 cannot be used for multiple TSV coupling analysis. We also point that even when there are same number of aggressors, TSV coupling capacitance changes when aggressors are in different locations. For example, Fig. 1 (b) and (c) have same number of aggressors but the total capacitance is different by 0.1x. This is because the E-field that forms capacitance changes due to different locations of the TSVs. Thus, we conclude that the coupling capacitance is a function of location, as well as a function of distance.

We show that a maximum substrate capacitance limit exists for a TSV victim when the radius (r) and the minimum pitch (P) are given. Even when an infinite number of aggressors are near a victim, the maximum substrate capacitance cannot be larger than that of a coaxial TSV, whose inner conductor radius is r, and the outer conductor, whose inner radius is P. We show this formula of a coaxial TSV in Eq. 2 [1].

$$C_{\mathrm{si,max}} = \frac{2\pi\epsilon_0\epsilon_{\mathrm{si}}L}{\ln\left(P/r\right)} \tag{2}$$

Regardless of how many aggressors surround a victim TSV, the total sum of TSV coupling capacitance will be smaller than Eq. 2. In other words, no matter how many aggressors surround a victim (Fig. 1 (f)), the E-field between the victim and the aggressors cannot be formed as strongly as a coaxial TSV (Fig. 1 (g)). Although the values of the maximum coupling capacitance will vary on different TSV radii and pitches, when the radius is $2\mu m$ and the minimum pitch between TSVs is $10\mu m$, the maximum capacitance will be around 2.26x. We conclude that the capacitance sum between a victim and the aggressors has a physical limit. Therefore, it cannot be larger than Eq. 2.

2.2 Neighbor Effect on TSV Coupling

Unlike the common belief that only the nearest aggressors impact TSV coupling, TSV coupling occurs even between the non-neighbor aggressors. In this section, we prove this and also prove that neighbor TSVs can reduce the capacitance of other aggressor TSVs.

First, we show that TSV coupling occurs between the far aggressor and the victim. Assume a simple layout where a victim TSV is neighboring two aggressor TSVs in a straight line (see Fig. 2 (a)). We performed modeling using the proposed model in Section 3.1 and the model was validated using Ansys HFSS. We intuitively think that the far aggressor will not affect coupling because a closer neighbor is near by. However, Fig. 3 shows that the far aggressor affects as much coupling voltage (139.6mV) as the close aggressor (184.6mV) when 1GHz signal is applied in 45nm Nangate technology. This is because the far aggressor also has a significant amount of capacitance between the victim (close aggressor: 9.46fF, far aggressor: 4.14fF, see Fig. 4 Case 3). Though the close aggressor shields the E-field between the victim and the far aggressor, it cannot be perfect. A strong E-field detours the first aggressor and forms capacitance between the far aggressor and the victim (see

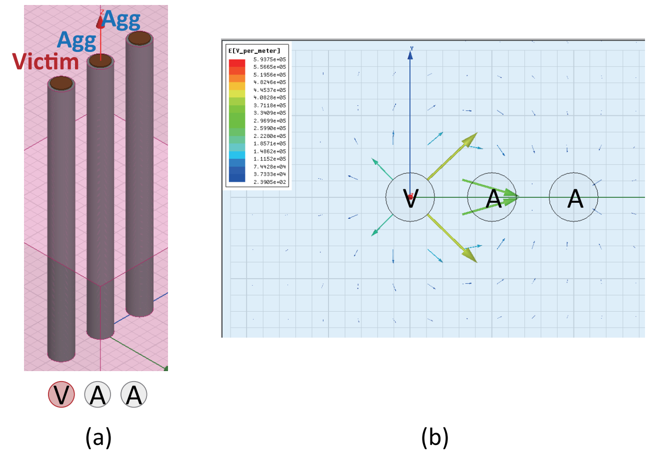

Figure 2: Neighbor Effect. (a) Two aggressor model in HFSS, (b) the E-field distribution between the TSVs.

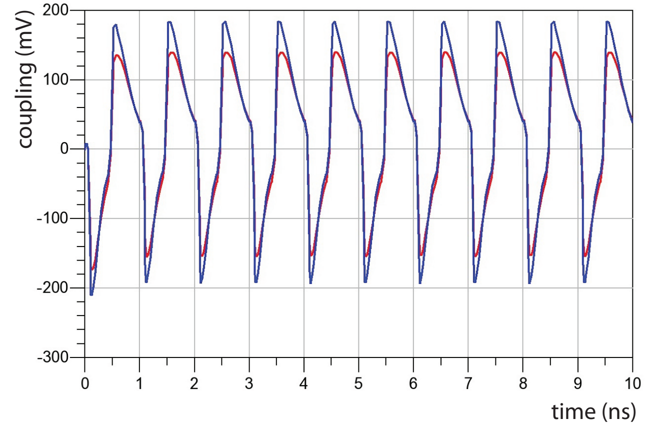

Figure 3: Coupling voltage of the near (blue) and far (red) aggressors shown in Figure 2.

Fig. 2 (b), field distribution simulated using Ansys Q3D). Despite the far aggressor has less than 50% capacitance of the close aggressor, V_{far} reduces by only 40mV. This is because of the complicated coupling network that TSVs compose, explained in [7].

Second, we show that neighbor TSVs can reduce the capacitance of other aggressor TSVs. Fig. 4 describes the far aggressor impact in terms of capacitance. Assume there are only two TSVs as Case 1 and Case 2. Each capacitance is 12.4fF (near aggressor) and 8.5fF (far aggressor). However, in a layout where two aggressors are together (Case3), the coupling capacitance of both aggressors decreases to 9.4fF and 4.1fF. This is because the TSVs in the layout correlate each other and create a new E-field distribution. We call this "Neighbor Effect". Using the Neighbor Effect, if we want to reduce the coupling capacitance between an aggressor and a victim, adding another TSV near the original aggressor will reduce the capacitance of both the original aggressor and the new TSV. Described in Section 2.1 Eq. 2, since there is a physical limit to the total coupling capacitance, no matter how many TSV neighbors are added, the total capacitance will be smaller than a certain value. Therefore, we conclude that the coupling capacitance is a function of distance, location, and also a function of neighbors.

3. MULTI-TSV COUPLING EXTRACTION

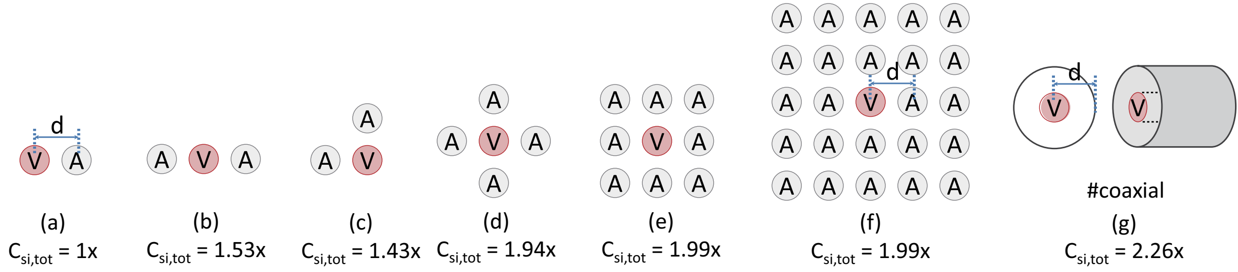

Figure 1: Illustration showing non-linear capacitance increase when the number of aggressors increase, and (g) the maximum limit of coupling capacitance of a TSV.

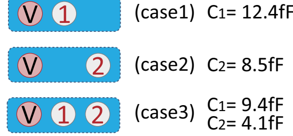

Figure 4: Neighbor Effect case study on how neighbor TSVs affect other aggressors.

In this section, we propose a compact multiple TSV-to-TSV coupling model and an extraction algorithm for full-chip analysis.

3.1 Compact Multi-TSV Coupling Model

[8] proposed an analytical multiple TSV model that can be used for performing coupling analysis. However, this model consists of many RLC components even when there are only few TSVs. Thus, we propose a compact multi-TSV-to-TSV coupling model that can be easily used on full-chip analysis. Fig. 11 in the supplement (a) shows the original model, and (b) shows our proposed model.

To describe the formulas of our model, we explain the concepts used in [8]. Assume three aggressors ($N = 3$) are near a victim. An $N + 1$ system can be considered as N-conductor transmission line. We assume the victim TSV (#0) as the ground and use the multi-conductor transmission line theory. Thus, the victim TSV does not have inductance and only have resistance. A TSV can be expressed as a resistor (R_{TSV}) and an inductor (L_{TSV}) in series. A SiO_2 liner surrounds the TSV for isolation, and is expressed as a capacitor (C_{ox}). Silicon substrate can be expressed as a resistor ($R_{\mathrm{si,ij}}$) and a capacitor ($C_{\mathrm{si,ij}}$) in parallel, of which is the resistance and the capacitance between aggressor i and aggressor j. When $i = j$, it is the resistance and the capacitance of the substrate between the victim and the aggressor.

For $R_{\mathrm{si,ij}}$ and $C_{\mathrm{si,ij}}$, we calculate $L_{\mathrm{si,ij}}$, which is the substrate inductance between two TSVs. L_{si} is expressed in matrix ($[L_{\mathrm{si}}]$), and consists of self-loop inductance and mutual-loop inductance. The following equations describe how to calculate these values,

$$L_{\mathrm{si,ii}} = \frac{\mu L}{\pi} \ln \left[\frac{P_{\mathrm{i0}}}{r + t_{\mathrm{ox}}} \right] \tag{3}$$

$$L_{\mathrm{si,ij}} = \frac{\mu L}{2\pi} \ln \left[\frac{P_{\mathrm{i0}} P_{\mathrm{j0}}}{P_{\mathrm{i0}}(r + t_{\mathrm{ox}})} \right] \tag{4}$$

where P_{i0} is the pitch between the victim TSV ($\#0$), and the aggressor TSV($\#i$) and P_{ij} is the pitch between two aggressor TSVs ($\#i$, and $\#j$). By the relation between the inductance matrix and the capacitance matrix in a homogeneous medium [10], we calculate $[C_{\mathrm{si}}]$,

$$[C_{\mathrm{si}}] = \mu_0 \epsilon_0 \epsilon_{\mathrm{si}} L^2 \left[L_{\mathrm{si}}\right]^{-1} \tag{5}$$

where C_{si} can be defined as Eq. 6.

$$[C_{\mathrm{si}}] = \begin{bmatrix} \sum_{k=1}^{N} C_{1k} & -C_{12} & \dots & -C_{1N} \\ -C_{21} & \sum_{k=1}^{N} C_{2k} & \dots & -C_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{N1} & C_{N2} & \dots & \sum_{k=1}^{N} C_{Nk} \end{bmatrix} \tag{6}$$

The conductance matrix $[G_{\mathrm{si}}]$ can be defined as

$$[G_{\mathrm{si}}] = \frac{\sigma}{\epsilon_0 \epsilon_{\mathrm{si}}} [C_{\mathrm{si}}] \tag{7}$$

In our compact model, we only use $C_{\mathrm{si,ii}}$ and $G_{\mathrm{si,ii}}$. The other RLC components can be reduced. This is reasonable because we only consider the impact between a victim and an aggressor, not the impact between two different aggressors. Using our model, we can reduce the RLC count around 60% when N=3. The RLC count reduces more as N increases. We ignore self inductance and mutual inductance in our model for two reasons. First, the TSV inductance impacts in a very high frequency (> 10 GHz). Second, a coupling path (C_{ox}) exists before the TSV inductance can impact coupling.

To validate our model, we first place aggressor TSVs around the victim TSV randomly in a fixed space. Then, we perform modeling using 3D EM solver HFSS, and also generate a SPICE netlist based on our compact model. We generate 10 layouts for each sample cases, and we compare the S-parameter of these two and report the maximum error of insertion loss. Fig. 5 shows the S-parameter comparison when N=3, and Table 1 shows the validation result. We show that our model is very accurate, even in a multiple TSV structure, by reporting the maximum difference in insertion loss less than 0.02dB.

3.2 Extraction Algorithm

In our previous discussions (Section 2.1 and 2.2), we showed that TSV coupling capacitance is a function of distance, location, and neighbor aggressors. To extract TSV-to-TSV coupling capacitance accurately, an approach considering only the closest neighbor or limiting the maximum target distance to calculate coupling capacitance cannot be used. Therefore, we propose an algorithm that considers distance, direction, and Neighbor Effect all in a holistic manner when extracting the coupling capacitance for all nets in the layout for full-chip analysis. Algorithm 1 describes how this works.

From a given layout, we first extract the (x,y) coordinate of each TSVs. Then, for a victim TSV, we sort all neighbor aggressor TSVs

Table 1: Model validation on general layouts

TSV dimensions (μm)			# TSVs	Average error (dB)	Max. error (dB)
Radius	Min. pitch	Height			
2	5	30	6	0.008	0.016
			8	0.011	0.015
			10	0.008	0.014
			12	0.011	0.015
		60	6	0.009	0.015
			8	0.011	0.016
			10	0.011	0.015
			12	0.008	0.014
4	10	30	6	0.010	0.016
			8	0.009	0.014
			10	0.011	0.017
			12	0.011	0.018
		60	6	0.010	0.017
			8	0.009	0.014
			10	0.010	0.015
			12	0.008	0.014

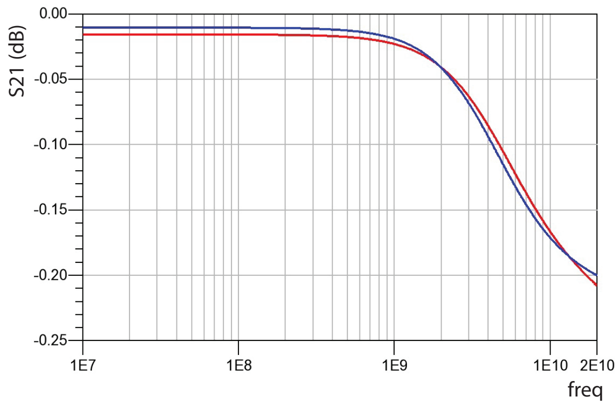

Figure 5: S-parameter comparison between our model and HFSS (red: HFSS, blue: our model)

by the closest Euclidean distance to the victim. We choose N neighbor aggressor TSVs (N: a significantly large number) from the sorted result that are closest from the victim and calculate the capacitance between the victim and the chosen aggressors. Once we calculate the capacitance of the aggressors, we create a coupling network between the victim and the aggressor that the capacitance is higher than a certain value (e.g., C > 0.01fF).

We choose a significant number of aggressors (N: more than 100) after sorting to guarantee that we do not neglect any meaningful, physically far but does not have any closer neighbors in the pathway, aggressors. Fig. 6 illustrates this idea. Unless we choose a certain number of aggressors for analysis, we can accidentally miss the valid aggressors that must be considered for extraction. For example, when N=10, the aggressor circled in blue is ignored. This can be considered only when N is bigger than 114. Therefore, N has to be a big number that can consider all the effective neighbors in a layout. By performing this extraction on every victim TSVs, we can extract the coupling capacitance on full-chip scale.

The advantage of this algorithm is that it is fast and considers all effective aggressors that affect the victim. In a layout, it is not the distance, but the location and the neighbors that is important. Since our algorithm calculates the coupling capacitance from a very large number of aggressors, not by distance, it does not neglect any aggressors that must be considered.

Algorithm 1: Multiple TSV-to-TSV capacitance extraction

1 **Algorithm:** Multiple TSV-to-TSV capacitance extraction
2 Locate all TSVs by its coordinate (x,y);
3 **while** *For a victim TSV* **do**
4   **while** *For all neighbor aggressor TSVs* **do**
5   Calculate the Euclidean distance of the aggressor TSVs to the victim TSV
6   **end**
7   Sort the neighbor aggressor TSVs by the closest Euclidean distance to the victim TSV;
8   Choose N aggressors that is closest to the victim;
9   Calculate the coupling capacitance of the N aggressors using the formula in Section3.1;
10   **if** *The calculated TSV capacitance is higher than C* **then**
11   Generate a coupling network between the aggressor and the victim;
12   **else**
13   Assign the TSV coupling capacitance to be zero;
14   **end**
15 **end**

Table 2: TSV coupling impact on crosstalk and timing.

	W/O coupling	W/ coupling [3]	W/ coupling (Our results)
Footprint (μm)	970 × 823	970 × 823	970 × 823
Total coupling noise (V)	590.77	732.75	815.01
Longest path delay (ns)	2.734	3.165	2.852
Total negative slack (ns)	-61.65	-115.07	-75.24

4. FULL-CHIP ANALYSIS

Using our extraction flow, we perform full-chip SI analysis in this section and compare our results to [3].

4.1 Full Chip 3D SI Analysis Flow

Since existing SI analysis tools cannot analyze 3D circuits accurately, we modified the 3D SI analysis flow in [3] to implement our results. First, we extract the SPEF file for each dies using RC extraction tool. Then, we run our script that implements the algorithm developed in Section 3.2 to create the SPEF file of TSV parasitics that can be plugged in to our flow. Then, we create a top-level verilog file. Once these files are prepared, we use Synopsys PrimeTime to read the verilog file, and create a top-level stitched SPEF file that contains RC information of all dies and the TSVs. Then, we analyze the stitched SPEF file and generate a SPICE netlist for each individual net for performing coupling noise simulation. The SPICE netlist has all the coupling information including wire-coupling, TSV coupling network by the extraction algorithm, and the aggressor signal and the victim driver models. We run HSPICE on each nets one by one, and report the peak noise at each port.

4.2 Design and Analysis Results

We designed FFT 256-8, which is a 256 point with 8 bit precision, real and imaginary, FFT as a test circuit. The circuit has 140K gates and 211 TSVs. The design is a 2-tier 3D IC based on Nangate 45nm technology. Our TSVs are 2μm in radius, 60μm in height, 0.5μm SiO_2 in liner, and 10μm on minimum pitch. Landing pad is 5 × 5μm, and each TSVs have a 0.5μm keep-out zone that no standard cells can be placed inside. The designs were based on our Cadence Encounter design flow to generate 3D layouts [9].

In Fig. 7 and Table 2, coupling analysis results of top-hierarchy

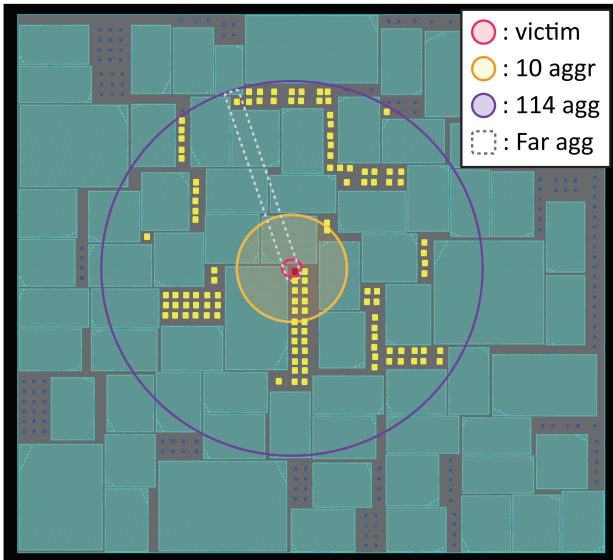

Figure 6: Comparison between a small N (10 aggressors) and a large N (114 aggressors) in the proposed algorithm.

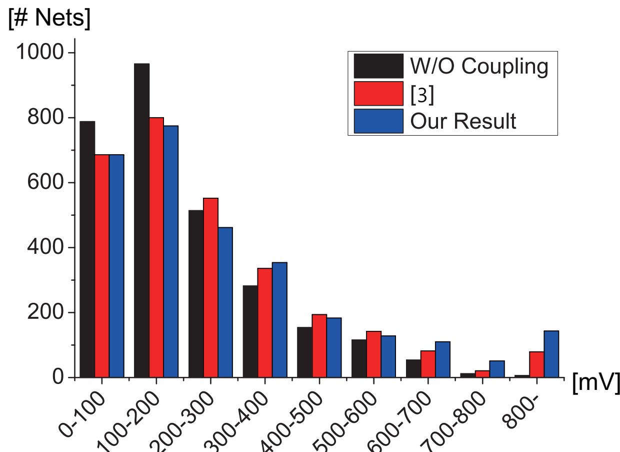

Figure 7: Coupling analysis result.

nets are shown and compared with [3]. Based on the results, we observe the following impacts: First, both approaches calculate higher coupling noise than w/o TSV coupling (590V). Second, [3] is missing a significant amount of TSV coupling impact that must be considered because it considers only the closest neighbors. Third, despite [3] is overestimating the coupling capacitance by linear superposition, our results show higher total noise voltage. The total coupling noise is 732V using the flow in [3] and 815V in our result. This is because our model considers more neighbor aggressors than [3] that must be considered. Therefore, we conclude that we cannot ignore Neighbor Effect. Second, in timing analysis, because [3] overestimates the total coupling capacitance, it also overestimates the timing degradation by TSVs as well. Since the maximum substrate capacitance is limited by Eq.2, by using the correct TSV model, we can save a significant amount of timing margin. In summary, we save more than 83V coupling voltage, more than 300ps in longest path delay, and more than 40ns total negative slack compared to [3].

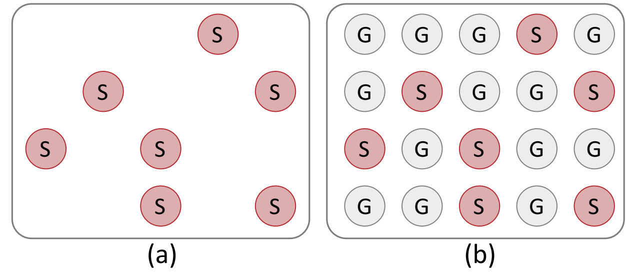

Figure 8: TSV Path Blocking in a layout: (a) Before TSV Path Blocking, (b) after TSV Path Blocking.

Table 3: Impact of TSV Path Blocking - block level design

	W/O Path Blocking	W/ Path Blocking
Footprint (μm)	970 × 823	970 × 823
Total coupling noise (V)	815.01	745.02
Longest path delay (ns)	2.852	2.811
Total negative slack (ns)	-75.24	-79.62
3D coupling noise (V)	224.24	154.25

5. TSV-TO-TSV COUPLING REDUCTION

Based on our findings, we propose a TSV-to-TSV coupling reduction method. We validate our methodology in block-level and wide-I/O design.

5.1 TSV Path Blocking

We propose a design optimization method based on that TSV coupling capacitance is a function of distance, direction, and neighbor aggressors. For a layout that has an aggressor and a victim, when an additional TSV is included in the design, the capacitance of the aggressor and the additional TSV both decrease (Section 2.2). Thus, whenever a space between an aggressor and a victim exists, we add GND TSVs between them. We name our coupling reduction method "TSV Path Blocking". By adding GND TSVs between an aggressor and a victim, we block the E-field path between the aggressor and the victim, and thus reduce the coupling capacitance. When applying this method in the layout, we assign as many GND TSVs as possible in empty spaces as Fig. 8. We may think that by adding GND TSVs, the total capacitance of the victim will increase. However, in a layout, a TSV is surrounded by many neighbors that the total coupling capacitance will saturate in a range around 2x (when $C_{\text{one victim}-\text{one aggressor}}$ = 1x) . Thus, adding GND TSVs near the neighbor does not have a big impact on increasing the total coupling capacitance (Section 2.1) of a victim.

Table 3 shows the impact of our method. By adding TSVs inside the empty space, the total coupling noise reduces from 815V to 745V. Considering 3D noise only, we reduce the 3D coupling noise by 32% from 224V to 154V. We report that TSV Path Blocking has a minor impact on timing. When GND TSVs are added, the total capacitance will increase slightly since more TSVs are placed near the victim. By the increased capacitive load, the total negative slack increases, but the impact is minor since the total capacitance has a maximum limit, and it is shared by the aggressor and the GND TSVs. We conclude that TSV Path Blocking is an effective way in reducing TSV-to-TSV coupling that has minor impact on timing performance. In a situation where we do not have enough space to insert GND TSVs, we can increase the area occupied by the TSVs and apply our technique. We show the impact of increasing the area occupied by the TSVs in wide-IO design.

Table 4: Impact of TSV Path Blocking - wide I/O design

	Original array	Spread array	W/ Path Blocking
Area by TSV (μm)	160 × 140	320 × 140	320 × 140
Total coupling noise (V)	824.26	797.9	742.37
Longest path delay (ns)	2.907	2.963	2.925
Total negative slack (ns)	-77.26	-74.51	-82.04
3D coupling noise (V)	193.99	157.41	105.81

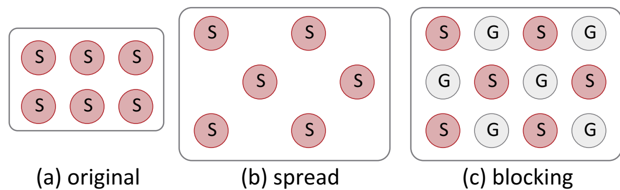

Figure 9: (a) Initial wide-I/O design (b) wide I/O design with spread TSVs (c) wide-I/O design with TSV Path Blocking

5.2 Optimization for Wide-I/O Design

We show the impact of TSV Path Blocking in wide-IO design. TSV Path Blocking can be an effective way to reduce coupling with the cost of increased TSV area. We designed three wide-I/O layouts and compare the SI impact. Fig. 9 (a) is our initial wide I/O design (original), (b) is the wide-I/O design with increased area (spread), and (c) is the wide-I/O design with our technique applied (blocking). Fig. 10 shows an actual layout applying our technique. For fair comparison, we did not modify the placement of the blocks and only increased the area used by TSVs. If the total die size changes due to increased TSV area, then the whole design will change. Therefore, the die size is the same for all cases.

By our technique, we see that the TSV occupied area doubles, but the total coupling noise reduces from 824V to 742V. Considering 3D noise only, we reduce the 3D coupling noise by 45% from 193V to 105V. Note that just by spreading the wide I/O array like Fig. 10 (d), the total coupling noise reduces too. However, if we include GND TSVs as (b), we observe more TSV coupling reduction. Wide I/O with spread TSV shows less total negative slack because the capacitance that a victim sees reduces due to the increased distance. When TSV Path Blocking is applied, we observe more coupling reduction in cost of a minor increase in total negative slack due to increased capacitance. In conclusion, in wide I/O design, we obtain a significant amount of coupling reduction by our technique in the cost of TSV area and small timing performance.

6. CONCLUSIONS

In this paper, we proposed a compact multiple TSV-to-TSV coupling model and an extraction algorithm for 3D ICs. Based on our model and simulations, we demonstrated that TSV-to-TSV coupling has a maximum capacitance limit, and the effect of non-neighboring aggressors is also critical to the total coupling capacitance. We developed a compact multiple TSV-to-TSV coupling model and an algorithm that can accurately consider the impact of far-neighbors on full-chip 3D signal integrity analysis. Using this model, we demonstrated that the far-neighbor aggressors have a significant impact on TSV-to-TSV coupling. To reduce the TSV-to-TSV coupling noise, we proposed a coupling reduction technique: TSV Path Blocking. We applied our technique on block level and wide-I/O design, and experimental results show that by TSV path blocking, 45% 3D coupling reduction can be obtained.

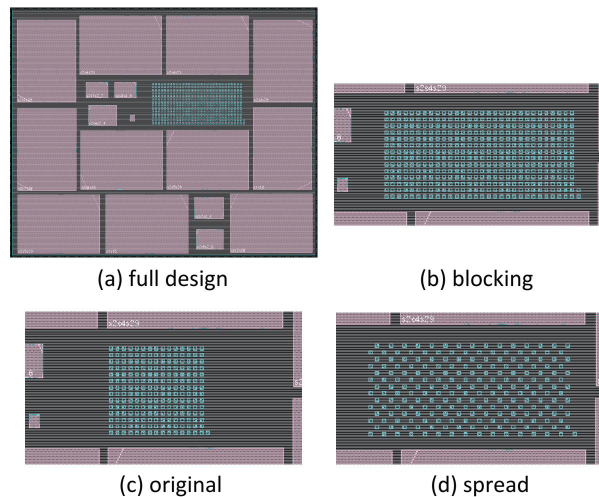

Figure 10: (a) TSV Path Blocking in Wide-I/O layout, (b) zoom-in photo of (a), (c) initial wide I/O design, (d) wide-I/O with spread TSVs

7. ACKNOWLEDGMENTS

This material is based upon the work supported by the NSF (CCF-1018216, CCF-0917000), SRC (1836.075, 2239.001), and the CISS funded by the MEST Global Frontier Project of the South Korean Government (CISS-2-3).

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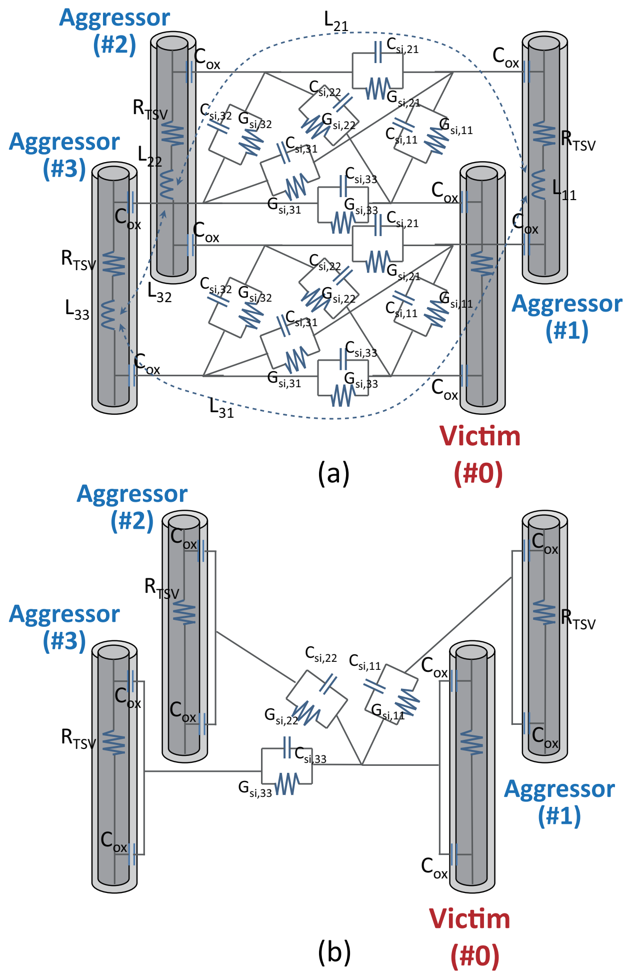

Figure 11: (a) Original model proposed in [8], (b) proposed compact TSV model for full-chip analysis.

SUPPLEMENT

S1 Multiple TSV-to-TSV Model

In this supplement, we provide an illustration and compare the multiple TSV-to-TSV coupling model that was proposed in [8] to our model (see Fig. 11). The model proposed in [8] (a) models the interaction between all TSVs. [8] takes into account for not only the interaction between the victim and the aggressors, but also the interaction between the different aggressors as well. Therefore, [8] may be feasible to model the interaction between multiple TSVs for a small number, but it may not be a feasible model for full chip analysis when the TSV count increases to a high number (such as more than 100) due to the high total RLC count. However, our model (b) reduces the RLC count significantly by considering the interaction between the victim and the each aggressor only. Therefore, our model gives us a reasonable amount of RLC count that enables full-chip analysis.

Note that even when there are only 3 aggressor TSVs, [8] uses 42 RLC components (20 capacitors, 16 resistors, three inductors, and three mutual inductors). However, our model uses only 18 components (11 capacitors and 7 resistors). This is about 60% reduction in the total component count. The RLC count reduction will be more significant when the number of aggressor TSVs in the layout increases.