On-chip Integrated Voltage Regulators: Frontside, Backside, or Off-Chip?

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***Abstract*—Back-end-of-line (BEOL) integrated voltage regulators (IVRs) significantly enhance power integrity by reducing on-chip and off-chip dynamic IR-drop compared to traditional off-chip IVR solutions. As semiconductor technologies scale down, power delivery networks increasingly suffer from parasitic limitations, impacting efficiency and performance. While backside power delivery networks (BS-PDNs) offer improvements by mitigating frontside parasitics and power density challenges, conventional architectures remain limited by package-level parasitics in 2.5D interposer systems. To address these constraints, we introduce optimized BEOL IVR structures suitable for BEOL integration, utilizing amorphous tungsten-doped indium oxide (IWO) transistors to enable monolithic 3D integration without additional footprint overhead. Our results demonstrate that BEOL IVRs achieve up to 61% and 54% reductions in on-chip dynamic IR-drop for frontside and backside configurations, respectively, with backside BEOL IVRs providing an additional 18% improvement. Furthermore, BEOL IVRs substantially decrease off-chip dynamic IR-drop by up to 71%, presenting a scalable and technology-node-independent solution for advanced IC designs.**

I. Introduction

As semiconductor technology nodes scale down, power density and voltage (IR) drop challenges become increasingly critical. Advanced nodes produce interconnects with parasitic resistances approaching $1k\Omega$ [5], significantly worsening IR-drop and impairing signal integrity and device reliability.

Low-power designs, particularly beyond the 8nm node, demand tighter power supply margins [4], intensifying scaling issues. Even minor voltage fluctuations can trigger instability or functional failures. Furthermore, emerging architectures such as Monolithic 3D (M3D) and Heterogeneous 3D (H3D), which feature increased integration densities, are especially susceptible. The rising complexity of many-core processors and system-on-chip (SoC) designs further underscores the importance of efficient, fine-grained voltage regulation across multiple voltage domains.

Traditionally, voltage regulators have been implemented off-chip, requiring significant additional area and cost due to the large passive components necessary for robust load regulation. However, the shift toward highly integrated many-core systems and densely packed SoCs makes purely off-chip voltage regulator solutions increasingly unfavorable, highlighting the need for scalable alternatives.

Integrated voltage regulators (IVRs) offer an attractive alternative to overcome limitations associated with off-chip regulators. Inductor-based IVRs have been successfully integrated within packages [3], [7], [9], [12], [13] or interposers [14]. However, these solutions are restricted to off-die integration, making them susceptible to impedances from package/interposer structures and C4 or μ-bump interfaces, thus requiring larger passive components or complex active regulation circuitry.

On-chip integration of IVRs typically employs capacitor-only architectures, due to difficulties integrating inductors directly on the silicon die. Such on-chip IVRs significantly mitigate the parasitic effects associated with off-chip components. Current state-of-the-art (SOTA) solutions primarily involve low-drop-out (LDO) and switched-capacitor (SC) regulators but are generally limited to CMOS nodes around 28nm or larger, imposing additional footprint overhead to accommodate active IVR circuitry [1]. Innovations such as deep trench, 3D, or 2.5D capacitor structures [8] can enhance capacitor density, yet existing on-chip IVR implementations remain constrained by footprint and node compatibility issues, especially at sub-10nm nodes.

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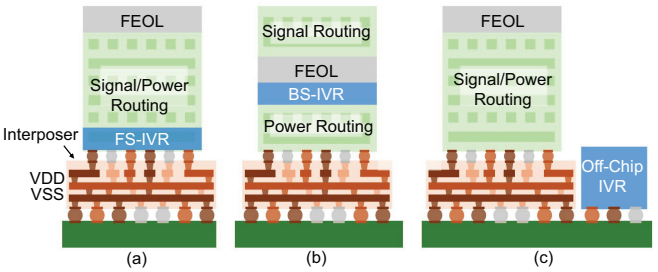

Fig. 1. Various BEOL IVR and off-chip IVR configuration stackups. (a) Frontside BEOL IVR configuration (b) backside BEOL IVR configuration (c) off-chip IVR configuration with either FS-PDN or BS-PDN.

To address these limitations, J. Kwak et al. [6] introduced a BEOL-compatible on-chip IVR approach leveraging tungsten-doped indium oxide (IWO) transistors [15] for monolithic 3D integration. IWO transistors are capable of being fabricated in the BEOL because they have a low thermal budget of $<250^{\circ}$C [15] opening doors for BEOL monolithic 3D integration. The BEOL IVR utilizes a switched-capacitor architecture, enabling true on-chip integration without incurring extra footprint overhead or node limitations, thus offering greater flexibility in advanced sub-10nm nodes.

However, comprehensive investigations into BEOL IVRs at the system level remain lacking. Existing studies fail to rigorously consider off-chip component parasitics, detailed on-chip power delivery network (PDN) modeling, and dynamic chiplet switching behaviors. Therefore, we introduce two novel BEOL IVR solutions integrated into both conventional frontside PDN (FS-PDN) and emerging backside PDN (BS-PDN) configurations, as depicted in Fig. 1. We perform comparative analyses against traditional off-chip buck converter solutions providing power through FS-PDN and BS-PDN.

The adoption of backside PDN and backside BEOL IVRs (BS-IVRs) addresses critical scaling challenges, with leading foundries reporting BS-PDN adoption for their upcoming 2nm technology node [10]. Moving PDNs from frontside to backside provides several benefits, including reduced IR-drop hotspots [11], minimized signal and clock routing congestion, and improved overall power, performance, and area (PPA) metrics.

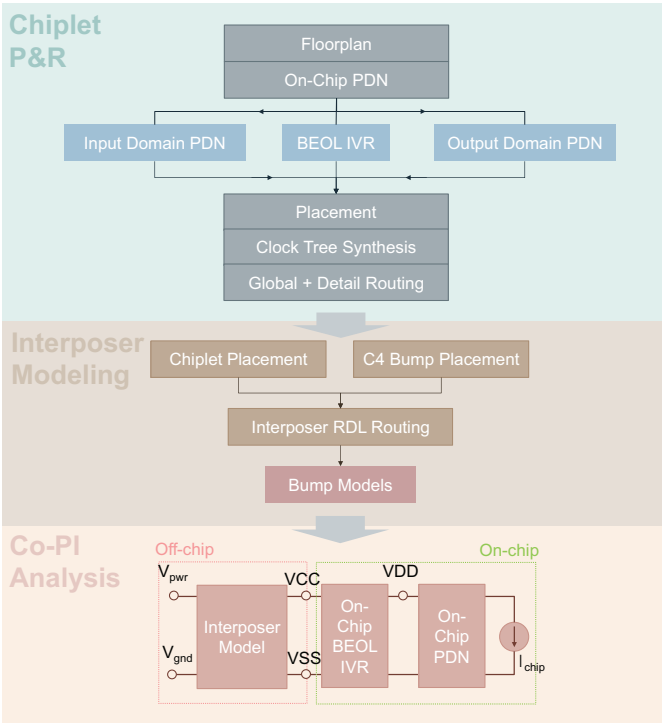

Fig. 2. End-to-end design and simulation flow of on-chip BEOL voltage regulators using Synopsys and Ansys EDA tools for concurrent power integrity (co-PI) analysis of off-/on-chip components.

Integrating BEOL IVRs on-chip, however, faces significant hurdles due to the absence of established Electronic Design Automation (EDA) flows and Process Design Kits (PDKs) capable of modeling BEOL-compatible devices and supporting comprehensive power integrity analyses from off-chip components down to chiplet switching devices.

Addressing these challenges, our work presents a novel IWO-based PDK developed for commercial technology nodes, enabling flexible integration in backside and frontside BEOL. Additionally, we propose an end-to-end physical design methodology encompassing FS-IVR and BS-IVR implementations, accounting fully for both on-chip PDNs and off-chip components. Our comprehensive design flow is illustrated in Fig. 2.

The achievements of this work are summarized in three-fold:

1) Proposal and characterization of two novel BEOL IVR configurations utilizing IWO transistors: frontside IVR (FS-IVR) and backside IVR (BS-IVR).
2) Comprehensive end-to-end modeling of power integrity impacts from off-chip interconnects (C4 bumps, interposer redistribution layers (RDL), micro-bumps) down to on-chip chiplet switching circuits.
3) Demonstration of BEOL IVR solutions achieving up to 61% reduction in on-chip dynamic IR-drop and up to 71% reduction in off-chip dynamic IR-drop.

II. On-Chip BEOL Integrated Voltage Regulator Design

In this section, we present the design and implementation of two variants of on-chip back-end-of-line (BEOL) integrated voltage regulators (IVRs): backside and frontside IVRs. Our design leverages a switched-capacitor DC-DC converter topology and targets power

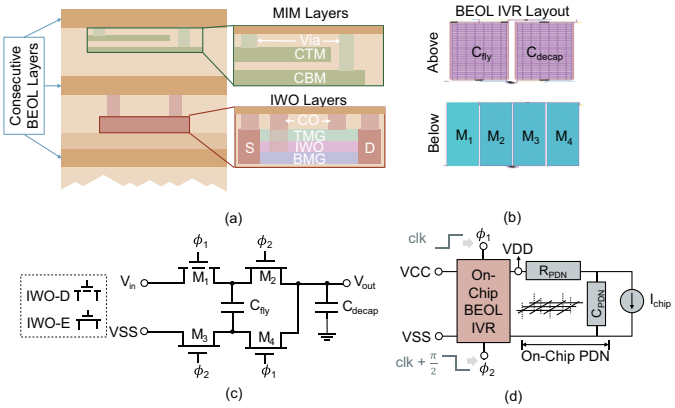

Fig. 3. IWO PDK and BEOL IVR design. Possible BEOL layers for the IVR consist of either MB1-MB3 (bottom to top, backside configuration) or M7-M9 (bottom to top, frontside configuration). (a) PDK metal stackup with IWO and MIM capacitor layers; (b) final BEOL IVR layout - capacitors overlap IWO devices; (c) switch-capacitor topology of BEOL IVR unit; (d) simplified IVR loading circuit with chiplet dynamic behavior.

TABLE I
Amorphous Tungsten-doped Indium Oxide (IWO) Device Specifications [15]

Layer	Material	Thickness (μm)
Top Metal Gate (TMG)	Pd	0.100
TMG Insulator	HfO_2	0.005
Source / Drain (S/D)	Pd	0.050
Channel	IWO	0.007
BMG Insulator	HfO_2	0.005
Bottom Metal Gate (BMG)	Pd	0.020

delivery to on-chip 3nm technology node switching devices. Consequently, we adopt a 2:1 voltage conversion ratio, stepping down from 1.4 V to 0.7 V. To facilitate rigorous design, modeling, and verification of BEOL IVRs, we developed a custom IWO Process Design Kit (PDK) based on a commercial 65nm technology node, ensuring compatibility with standard industry workflows. The on-chip technology node (3nm-based) and IWO PDK (65nm-based) are independent of each other. Furthermore, we systematically evaluate the performance of BEOL IVRs against conventional off-chip voltage regulation solutions, providing a comparative analysis of power efficiency and integration benefits; all IVR designs in this study omit active voltage regulation circuitry, assessing raw conversion efficiency and passive regulation capabilities.

A. IWO Process Design Kit

The IWO PDK accurately designs and models the behavior of emerging IWO BEOL devices based on manufacturing constraints [15] and commercial design rules. The IWO device follows a dual-gate CMOS-like structure, and the device layer specifications are described in Table I. We integrate two IWO device variants in our PDK: depletion mode (IWO-D) and enhancement mode (IWO-E) to design BEOL power circuitry [6]. Additionally, we leverage metal-insulator-metal 2D capacitors based on commercial 65nm technology to design capacitors.

B. Frontside IVR

To enable monolithic 3D integration of back-end-of-line (BEOL) integrated voltage regulators (IVRs) for frontside configuration (FS-IVR), it is essential to accurately model, design, verify, and integrate

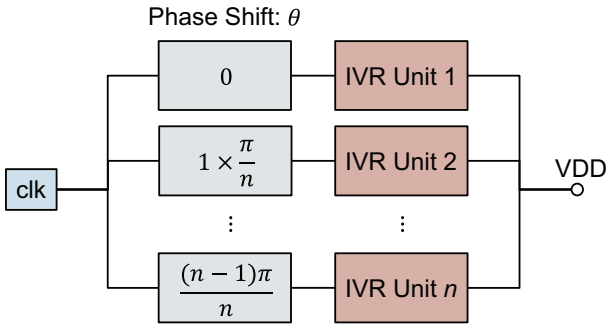

Fig. 4. Parallel IVR configuration with interleaved primary clock signals.

TABLE II
BEOL IVR FINAL DESIGN SPECIFICATIONS

Metrics	Value
Footprint (mm^2)	0.0149
IWO # Fingers	125
IWO W_{total} / L $(\mu m/\mu m)$	10,000 / 0.050
IWO W_{eff} (μm)	80
MIM Capacitor W/L $(\mu m/\mu m)$	72.82 / 72.82
C_{fly}, C_{decap} (pF)	175
$C_{density}$ $(pF/\mu m^2)$	0.033
Op. Freq. (MHz)	400

both active BEOL IWO devices and BEOL MIM capacitors within the frontside BEOL metal stack. Given the constraints imposed by initial FS-PDN implementation, all signal and clock routing are restricted to frontside metal (FSM) layers M2 through M6 during placement-and-route (P&R). To ensure minimal interference with these critical routing resources, the FS-IVR is integrated within FSMs M7 through M9.

As illustrated in Fig. 3a, the consecutive BEOL layers M7, M8, and M9 are arranged from bottom to top. Consequently, IWO devices are placed between M8 and M7, while MIM capacitors are positioned between M9 and M8. In Fig. 3b, the FS-IVR layout has MIM capacitors above the IWO devices, enabling more device packing and a compact footprint. The FS-PDN of the chiplet originates from M7 and extends downward to M4 and M1, ensuring power delivery to memory macros and standard cells, respectively. The FS-IVR outputs the VDD supply from M7, providing efficient power distribution to the integrated circuitry.

C. Backside IVR

Backside process technology offers significantly lower resistivity metals compared to frontside BEOL metals, enhancing power delivery efficiency. Additionally, the decoupling of power distribution between the frontside and backside mitigates frontend congestion and leads to substantial improvements in power, performance, and area (PPA). However, since backside processing has traditionally been utilized exclusively for power delivery network (PDN) decoupling and implementation, backside metals (BSMs) remain largely underutilized, resulting in considerable dead space. To capitalize on the abundant available real estate in the backside and the lower resistivity of backside metals, we propose integrating back-end-of-line integrated voltage regulators (BEOL IVRs) in the backside (BS-IVR) as an alternative approach.

Our 3nm in-house PDK, developed for standard cell and memory macro characterization, supports backside metallization, enabling the implementation of power rails at the buried power metal layer (MBPR). Buried power rails have demonstrated notable benefits in reducing pin capacitance and frontside routing congestion, thereby enhancing standard cell PPA [11]. To fully leverage the advantages of backside integration, we construct our backside power distribution network (BS-PDN) using metal layers from the first backside metal (MB1) down to the MBPR layer, incorporating nano-Through-Silicon-Vias (nTSVs) to establish interconnectivity.

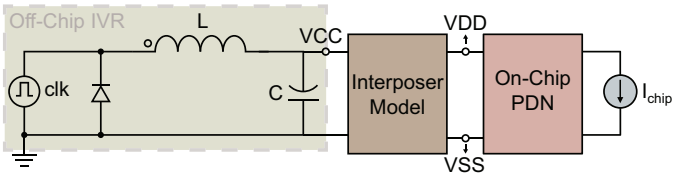

Fig. 5. Baseline off-chip IVR based on conventional buck converter architecture.

To comply with the backside manufacturing process, the BEOL configuration illustrated in Fig. 3a is flipped for BS-IVR integration compared to its frontside counterpart; IWO devices are positioned above the MIM capacitors rather than beneath them. As a result, according to 3, the consecutive BEOL layers for the backside case are MB1-MB3 from bottom to top. The IWO devices reside between MB1 and MB2, and MIM capacitors are positioned between MB2 and MB3. Consequently, as shown in Fig. 3, the BS-IVR layout mirrors the FS-IVR structure, with the primary distinction being the placement of MIM capacitors beneath the IWO devices, reversing their order.

D. IVR Design Exploration

To perform a fair comparison between FS-IVR and BS-IVR, we perform design exploration on BEOL IVRs and apply the design specifications to both IVR variants. All BEOL IVRs are constrained by PDN RLC parasitics and dynamic chip load to evaluate the IVR's capabilities rigorously. Furthermore, the goals of our work are to not target rigorous optimization of IVRs, but to investigate how different BEOL configurations (frontside vs. backside) present advantageous solutions to the voltage regulation problem for advanced technology node ICs.

To target large dynamic switching current behavior as well as on-chip PDN impedance, the BEOL IVR must have high drive current and large capacitance to improve efficiency. Increasing drive strength incurs greater W/L proportions of IWO devices, and increasing flying and decoupling capacitance incurs sizing up the capacitor. However, sizing up devices and capacitors naively requires additional footprint overhead as well as significantly larger parasitic resistance. To mitigate physical limitations, we implement an interleaved parallel IVR architecture illustrated in Fig. 4. Given that a BEOL IVR requires a primary clock signal for each unit, the primary clock signal is phase shifted based on the number of IVRs implemented in the design. The parallel IVR solution significantly improves voltage ripple while improving individual IVR unit efficiency. Table II records our final design specifications of FS-/BS-IVR solutions.

III. Off-Chip Voltage Regulator

To fairly analyze the on-/off-chip power integrity impacts of on-chip BEOL IVRs, we compare against conventional off-chip IVRs, specifically the DC-DC buck converter depicted in Fig. 5. Our off-chip IVR resides on the package/PCB or outside the interposer illustrated in Fig. 1. The chiplet follows standard power planning during placement-and-route flow and we implement both cases: FS-PDN and BS-PDN.

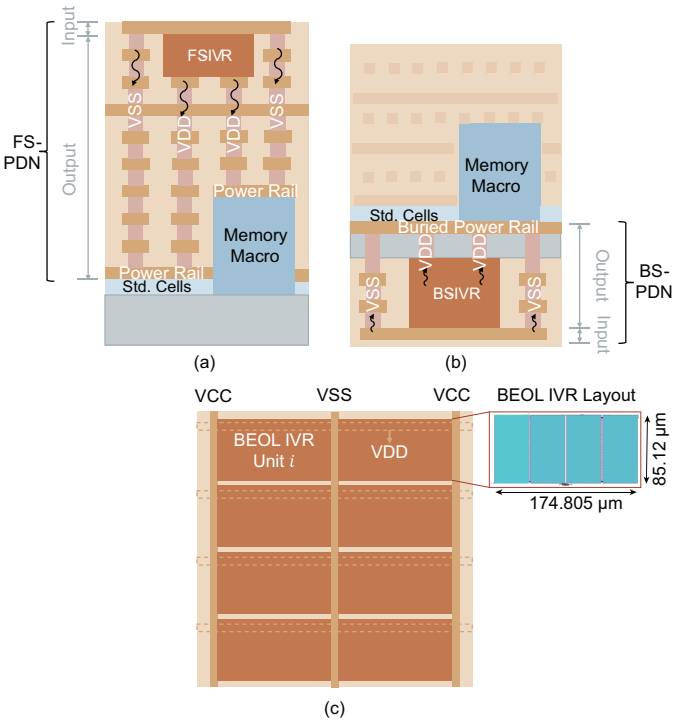

Fig. 6. On-chip integration configurations for FS-IVR and BS-IVR. (a) FS-IVR with FS-PDN integration (b) BS-IVR with BS-PDN integration (c) top-view of multiple BEOL IVRs placed; layout showcases IWO devices covering capacitors.

TABLE III
ON-CHIP POWER DELIVERY NETWORK CONFIGURATIONS AND PROPERTIES

Where?	Layer	Width (μm)	Pitch (μm)	Res. ($\Omega/\mu m$ or Ω)
FS	M9-M8	FS-IVR routing		
	M7-M6	2.0	4.032	0.241
	M1	0.025	0.24	9.407
BS	MBPR [16]	0.025	0.24	6.77
	nTSV	0.06	2.016	5
	MB1-MB2	2.0	4.032	0.128
	MB1-MB3	BS-IVR routing		

Off-chip inductor based IVRs typically offer higher power conversion efficiency and superior load regulation, however, they introduce significant design and integration challenges. Achieving high inductor quality necessitates complex manufacturing processes and larger form factors, resulting in substantial footprint overhead [7], [9], [13], [17]. These limitations render off-chip solutions impractical for dense integration scenarios, especially in advanced technology nodes, where area efficiency and tight packaging constraints are critical. While discrete passive components, such as SMD type inductors, present a lower cost and readily available alternative, their use introduces additional system level challenges. Chief among these is the susceptibility to electromagnetic interference (EMI), which can degrade signal integrity, introduce coupling noise, and necessitate additional filtering or shielding strategies, adding to design complexity.

Moreover, off-chip inductors and capacitors are physically separated from the logic die, which inherently limits their ability to respond quickly to rapid current transients within the chip. This spatial disconnect exacerbates issues of on-chip power integrity, especially in modern nodes, where supply voltages are lower and current demands are highly dynamic. The resulting voltage droop and noise propagation can impact timing margins and overall reliability. Consequently, off-chip IVR designs must be carefully optimized not only for power efficiency and footprint, but also for electromagnetic compatibility and robust power delivery at the point of load.

In this work, we explore a minimally sized off-chip IVR configuration, without active regulation circuitry, as a baseline for evaluating the tradeoffs in footprint and power delivery relative to BEOL integrated IVRs. Our study operates under the assumption that reduced inductance and capacitance values correspond to a proportionally smaller off-chip IVR footprint. However, it is important to note that while footprint may be minimized, the aforementioned challenges related to EMI, noise coupling, and insufficient on-chip regulation remain fundamental limitations of off-chip approaches in advanced integration scenarios.

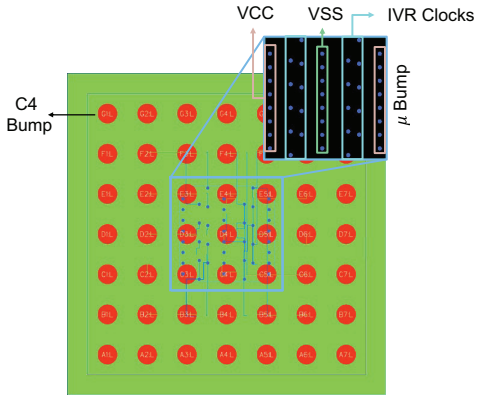

Fig. 7. Off-chip passive silicon interposer model with C4 bumps, chiplet μ-bumps, and RDL routing.

TABLE IV
PASSIVE SILICON INTERPOSER PROPERTIES

Metric	Value
Footprint (mm^2)	1.44
# of RDL Layers	3
RDL Width / Pitch (μm)	0.4 / 0.4
# C4 Bumps	49
C4 Bump Diameter (μm)	75.0
C4 Bump Pitch (μm)	150.0
# μ-Bumps	44
μ-Bump Diameter (μm)	12.5
μ-Bump Pitch (μm)	25.0

IV. FULL-DESIGN EVALUATION

A. Design and Simulation Setup

1) On-Chip P&R and Integration: This study implements an end-to-end physical design EDA flow to analyze the effects of power integrity of the full stack from interposer down to the power pins of standard cells and memory macros. We investigate the impacts of loading off-chip IVRs and on-chip BEOL IVRs with off-chip PDN parasitics, on-chip PDN parasitics, and dynamic switching behavior of the chiplet. For practical benchmarking, the chiplet is the RISC-V OpenPiton-Ariane single-core-configured processor [2]. The chiplet technology is based off our 3nm in-house technology node with the option of incorporating buried power rails for backside power delivery and regulation. All standard cell and memory macros require a power supply voltage of 0.7 V. Placement-and-route (P&R) of our design is accomplished using Synopsys® IC Compiler II.

TABLE V
PPA COMPARISON BETWEEN THREE VOLTAGE REGULATOR DESIGNS - OFF-CHIP IVR, FS-IVR WITH FS-PDN, AND BS-IVR WITH BS-PDN. POSITIVE $\Delta\%$ IMPLIES GAIN OVER RESPECTIVE OFF-CHIP IVR CASE.

Metrics	Off-Chip IVR + FS-PDN	FS-IVR + FS-PDN	Off-Chip IVR + BS-PDN	BS-IVR + BS-PDN
Chiplet Power, Performance, Area				
On-Chip Metal Stack (BSM + FSM)	0 + 7	0 + 9	3 + 6	3 + 6
Footprint (mm^2)	0.128		0.128	
Cells Count (#)	347,391	347,391	338,374	338,374
Signal+Clk WL (m)	1.340	1.340	1.316	1.316
WNS (ps)	-122.09	-122.09	-61.41	-61.41
Eff. Freq. (ps)	0.970	0.970	1.030	1.030
Total Static Power (mW)	87.400	87.400	85.166	85.166
On-Chip Power Integrity				
PDN Utilization (%)	25		25	
IVR Count (#)	1	8	1	8
Conversion Ratio ($V:V$)	1.4 : 0.7		1.4 : 0.7	
Switching Freq. (MHz)	400	400	400	400
Decoupling Cap. (nF)	-	0.125	-	0.125
Internal Cap. (nF)	2.0	0.125	2.0	0.125
Inductor (nH)	0.25	-	0.25	-
Settling Time (ns)	150.0	12.6 (+91.6%)	100.0	10.3 (+89.7%)
Worst Dyn. IR-Drop (V)	0.626	0.244 (+61.02%)	0.392	0.180 (+54.08%)
Steady-State Output Swing (V)	0.0807	0.031 (+61.59%)	0.262	0.041 (+84.35%)
Off-Chip Power Integrity				
PDN Impedance (Ω)	7.145		7.145	
PDN Dyn. IR-Drop (V)	0.0123	0.008 (+34.96%)	0.028	0.008 (+71.43%)

Based on Fig. 2, we break apart the traditional power planning stage to incorporate our BEOL IVRs for complete on-chip integration and analysis. The PDN is partitioned into two domains: input and output. Fig. 6 illustrates how the PDN for frontside and backside cases are partitioned into input and output power delivery networks. The input power delivery network supplies a target voltage of 1.4 V, and the output power delivery network supplies an ideal target of 0.7 V; BEOL IVRs and front-end-of-line (FEOL) cells share the same VSS line. For a fair comparison, FS-PDN and BS-PDN share the same specification in Table III. Given the partitioned PDN, we maximize the utilization of BEOL layers by filling the remaining unutilized space with BEOL IVRs.

The integration of BEOL IVRs requires a practical layout of the IVR to ensure IVR routing resources cause blockages within the chiplet. We ensure our IVR layouts pass DRC and LVS to generate realistic layouts. Siemens® Calibre is used to perform DRC and LVS checks. For parasitic extraction Synopsys® StarRC is used because our technology parasitics follow Synopsys's proprietary Interconnect Technology Format (ITF). The final layout is translated into LEF file for proper integration into the chiplet's BEOL stack in the design block.

2) Off-Chip Modeling: Modeling off-chip components is required to analyze off-chip power integrity with voltage regulators. When working with BEOL IVRs, the pad locations of μ-bumps are dependent on the placement of BEOL IVRs due to tight packing. Additionally, a parallel IVR solution with n IVR units necessitates $2n$ unique clock signal pads on top of VCC and VSS pads. Our study does not account for on-die signal IOs, but will be considered for future work. We design all IVR cases on a passive silicon interposer consisting of three redistribution layers (RDLs). Table IV describes our passive silicon interposer specifications including RDL routing and bump plans.

Interposer routing and design is constrained upon chiplet μ-bump placement. Siemens® Xpedition is utilized to define the RDL stack, design the interposer, establish μ-/C4-bump placements, and perform RDL routing. Fig. 7 is a snapshot of the final passive silicon interposer layout. Given our complete interposer design, Siemens® Hyperlynx is used to extract the interposer as an S-parameter model for off-chip power integrity analysis.

3) Analysis Testbench: After integrating BEOL IVRs into the chiplet post-P&R design block and extracting the interposer design, power integrity analysis is conducted. Ansys® RedHawk is utilized for dynamic power integrity analysis; however, the tool has limitations in evaluating dynamic IR-drop when the supply line is driven by analog circuitry. To accurately analyze the impact of dynamic IVR behavior driven by off-chip components and loaded by on-chip PDN and dynamic switching activity, the on-chip PDN's RLC parasitics are extracted using RedHawk's CPM utility, exporting the PDN RLC network as a SPICE netlist. The final concurrent off-chip and on-chip power integrity analysis testbench integrates the off-chip model's S-parameters, the BEOL IVR SPICE netlist with IWO Verilog-A behavioral models, the on-chip PDN RLC SPICE netlist, and the chiplet's dynamic switching activity. Dynamic simulation is performed over 100ns with a 20% propagated switching activity workload assumption.

V. EXPERIMENTAL RESULTS

The PPA summary, on-chip power integrity, and off-chip power integrity results of OpenPiton benchmark with off-chip IVR, BS-IVR, and FS-IVR are tabulated in Table V. Power integrity numbers are larger than typical due to large dynamic switching load, aggressive chiplet technology node, and, primarily, no active feedback circuitry for load regulation.

Our contributions focus on the physical characteristics of IVR circuitry and assess their ability to regulate advanced technology node dynamic switching load without additional load regulation circuitry and optimization. Consequently, we motivate towards IVR integration into the BEOL as an alternative solution for monolithic 3D integration and for further exploration in improving monolithic integration of BEOL IVRs.

A. PPA Analysis

For fair comparison, we ensure that the designs that utilize the same PDN type (e.g. FS-PDN, BS-PDN) are the same between off-chip

IVR and BEOL IVR cases. Consequently, the PPA results between off-chip IVR and BEOL IVR design blocks are the same given the same PDN for both cases. It is clear that BS-PDN-based designs will yield improved overall PPA. There is approximately 50% decrease in worst negative slack (WNS) implying about 6% increase in maximum frequency. The number of cells is greater for FS-PDN case due to the necessity for greater number of buffers/inverter-pair repeaters to drive longer wirelength signal/clock nets.

B. Off-Chip and On-Chip Power Integrity Analysis

Off-chip IVR designs follow the schematic presented in Fig. 5. Note that the off-chip IVR with FS-PDN case utilizes 7 FSMs compared to the FS-IVR counterpart leverages 9 FSMs. FS-IVR requires an additional 2 FSMs to compensate for internal FS-IVR routing; therefore, the off-chip IVR case only leverages 7 FSMs. All IVRs are configured for 2:1 conversion policy from 1.4 V to 0.7 V switching at 400 MHz.

The off-chip IVR cases indicate significant settling time delays compared to their BEOL IVR counterparts due to voltage conversion/regulation occurring much earlier in the design stack. The output voltage of the off-chip IVR will suffer IR-drops due to interposer parasitics as well as on-chip PDN parasitics. BS-IVR showcases approximately 90% improvement in settling time compared to its off-chip IVR counterpart. Additionally, BS-IVR with BS-PDN improves settling time of IVR by 18% compared to FS-IVR with FS-PDN because FS-PDN has greater parasitics compared to BS-PDN. This is also observed in the off-chip IVR case between FS-PDN and BS-PDN.

Significant benefits are observed for BEOL IVR cases in terms of on-chip and off-chip IR-drop. The on-chip worst dynamic IR-drop metric measures the dynamic IR-drop at the worst instance in the entire design. BS-IVR and FS-IVR improve worst-case on-chip dynamic IR-drop by 54% and 61%, respectively, compared to their off-chip IVR counterparts. BS-IVR showcases the best on-chip power integrity by default compared to FS-IVR with about 18% improvement. However, designs with FS-PDN showcase improved steady-state output swing of IVRs consistently, predominantly due to improved capacitive filtering. Finally, FS-IVR and BS-IVR reduce dynamic off-chip IR-drop by 35% and 71%, respectively. Therefore, BEOL IVRs present a promising solution to mitigating both off-chip and on-chip power integrity issues in advanced technology node designs.

VI. Conclusion

Integrating IVRs directly into the BEOL presents significant advantages over traditional off-chip IVR solutions, effectively addressing scaling challenges in advanced-node ICs. This study provides a comprehensive evaluation of the power integrity impacts of BEOL IVRs compared to off-chip alternatives, spanning from C4 bumps through off-chip PDNs, micro-bumps, and finally through the on-chip PDN. The analysis considers dynamic chiplet switching behaviors to assess dynamic loading of IVRs and resultant IR-drop waveforms from the perspective of standard or memory cells. BEOL IVRs demonstrate substantial improvements, including up to 61% reduction in on-chip dynamic IR-drop, 71% reduction in off-chip dynamic IR-drop, and 90% improvement in voltage settling time compared to off-chip solutions. Additionally, when comparing BS-IVR with BS-PDN against FS-IVR with FS-PDN, the on-chip dynamic IR-drop and settling time further improve by 18%. BEOL IVRs thus represent a viable strategy for monolithic IVR integration, independent of the targeted technology node constraints.

VII. Future Work

Future work will focus on extending the investigation of BEOL-integrated IVRs to older technology nodes and scaling scenarios such as many-core processors and state-of-the-art (SOTA) system-on-chip (SoC) designs. Since BEOL device fabrication introduces additional complexity and cost to the manufacturing process, exploring the viability of BEOL-based power delivery in mature nodes presents an attractive and pragmatic research direction. In particular, integrating BEOL solutions into dies fabricated in mature process technologies (e.g., 16nm, 28nm/32nm, and 45nm) opens the door for developing analytical cost models that quantify trade-offs in performance, integration effort, and economic feasibility. Toward this goal, we aim to generalize the IWO PDK to apply for any technology node (mature or advanced) to enable a rigorous evaluation of BEOL IVR applicability across a broader technology spectrum.

Our findings also motivate the development of automated design methodologies that optimize IVR configurations based on specific application requirements. Automating the IVR co-design process, particularly for BEOL-integrated solutions, represents a promising avenue for enabling scalable, application-aware power delivery in heterogeneous systems.

Another important direction concerns thermal considerations. Since IWO transistors are monolithically integrated within the BEOL stack, localized thermal hotspots and associated reliability concerns become non-negligible. Future work will explore thermal modeling and management strategies for BEOL-integrated devices to ensure safe and efficient operation under realistic workloads.

Our study also has several limitations that will be addressed in future work. In particular, our current evaluation lacks a rigorous comparison against SOTA on-chip IVR solutions, which are typically fabricated on the same die as the target chiplet and constrained to a fixed technology node (e.g., 32nm or 45nm). Furthermore, our current off-chip IVR baseline does not reflect the latest advancements in off-chip power delivery, and thus may underestimate the full potential of such solutions. Based on these observations, we plan to conduct an in-depth comparative study of BEOL IVRs against both SOTA on-chip and off-chip IVR implementations, to more comprehensively assess the trade-offs in performance, integration complexity, and overall system efficiency.

VIII. Acknowledgements

This work was supported by the Semiconductor Research Corporation (SRC) through the JUMP 2.0 Center Program (CHIMES 3136.002). Additional support and collaboration were provided through CHIMES projects 3136.010 with Dr. Shimeng Yu and Jungyoun Kwak, and 3136.007 with Dr. Suman Datta. This research was also supported by the Ministry of Trade, Industry & Energy of South Korea (1415187652, RS-2023-00234159).

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