A Novel Backside Signal Inter/Intra-Cell Routing Method Beyond Backside Power for Angstrom nodes

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Abstract: For the first time, we investigate a power-performance-area (PPA) benefit of novel backside (BS) signal (BSS) routing using BS gate/source-drain contact targeting the Angstrom node. INVx1 with BS-pin has a smaller miller capacitance (C_{miller}) and shows 3.0 ~ 3.3 % higher ring oscillator (RO) frequency at iso-power by BSS inter-cell routing. Even without BS-pin, standard cells can improve frontside (FS) routing congestion and an energy-delay product (EDP) by using BSS intra-cell routing. BSS intra-cell routing based chip has a larger IR drop, but it is mitigated when the μBump pitch is small. The BSS intra-cell routing based chip shows an 8.61 ~ 9.46 % lower power delay product (PDP).

Introduction: Over the past few years, the BS power (BSP) delivery network has been extensively studied due to its advantages in greatly improving IR drop and FS routing congestion [1]-[2]. Among various BSP methods, connecting power lines using BS source-drain contacts is studied as the most effective method [3]. Utilizing the BS space has great potential; placing only power lines in BS can be a waste of space. Thus, in a recent study, the BS clock tree using nanoTSV has been studied, improving chip power and performance **(Fig. 1a)** [4]. Furthermore, a BS gate contact (BSGC) that enables BSS without utilizing nanoTSV has also been implemented **(Fig. 1b)** [5]-[6]. Utilizing a BSGC enables a more sophisticated design compared to nanoTSV, including BSS intra and inter-cell routing using BS-pin. However, BSS using BSGC has only been implemented in a single device, and its detailed utilization methods and benefits have not been studied. In this paper, we analyzed the BSS intra/inter-cell routing method using BSGC and its PPA benefit in terms of cell and chip.

Device and cell design assumptions: For BSP **(Fig. 2a)** and BSS cells **(Fig. 2b)**, forksheet-FET (FSFET) based 80 nm cell height and 4-track standard cells are assumed to target the angstrom node. In the BSS cell, two BSS routing tracks are used, and BSS has a relatively smaller power line and BSC width. We used a 4-channel FSFET with a 20 nm channel width **(Fig. 3a)**. Wrap-around contact (WAC) improves contact resistance and drive current [7]. Thus, before forming S/D BSC and BSGC, the WAC process should be applied in advance **(Fig. 3b)**. There is no performance difference between BSP and BSS devices because WAC is used for both devices; thus, we use the same BSIM parameters. Interconnect materials and resistivity are assumed to be the same as in the previous paper [8] **(Table I)**. We used Synopsys tools and modified the previous PDK when creating our Angstrom node PDK. Bi-directional metal lines are applied for cell design.

Standard cell design options: In the BSS cell, FS and BS-pin can be used selectively, and the INVx1 can be designed in four different layouts **(Fig. 4a)**. If the input and output pins are formed on different sides, the pin capacitance (C_{pin}) is reduced due to the reduction of C_{miller} **(Fig. 4b)**. Reduction of C_{pin} impacts the interconnect load capacitance (C_{load}), which can improve overall chip power and performance. Placing both pins on the BS shows the highest C_{pin} because the power line is on the BS, which occurs the C_{para} between the BS pin and the power line **(Fig. 4c)**. 15stage RO (fan-out = 3) simulation shows that BS routing only RO has a slightly lower frequency than FS only RO **(Fig. 5)**. On the contrary, RO utilizing both side routing shows 3.0 ~ 3.3 % improved freq due to improved C_{miller}. The BS-pin very clearly improves the cell, but advancements in EDA tools for chip design that can consider BSS inter-cell routing are not ready yet. To avoid the chip design issue of BS-pin, BSS intra-cell routing can be an alternative.

Backside signal intra-cell routing: In the BSP cell, pin metal and non-pin metal are located on the FS **(Fig. 6a)**. On the contrary, in the BSS cell, C_{miller} can be reduced while maintaining FS-pin by relocating only non-pin metal **(Fig. 6b)**; and we call it BSS intra-cell routing cell. Also, it increases the FS routing space, simplifying place and route. We designed 42 standard cells for BSP and BSS intra-cell routing **(Fig. 7a)** and assumed only one thin BS metal layer for intra-cell signal routing **(Fig. 7b)**. However, some BSS cells, including INVx1, do not have non-pin metal and do not use BSS signal routing tracks **(Fig. 7c)**. In this case, the only difference between BSP and BSS cells is MB1 power line width. Thus, INVx1 has almost no change for BSP and BSS **(Table II)**. BUFx1 uses BSS routing and shows a smaller C_{pin}. However, BUFx1 showed little change in EDP because its internal parasitic did not change significantly due to the simple layout. DFFHQNx1 has a more complex layout and many non-pin metal lines. Since relocating all non-pin metals to the BS is impossible, we placed them selectively on the BS. BSS utilized DFFHQNx1 significantly improves parasitic, showing a 4.4 % smaller C_{pin} and 4.5 ~ 6.0 % lower EDP for both fast and slow cases.

IR drop analysis: Three BS metal layers and μBump were applied for chip simulation **(Fig. 8a)**. The power line of the BSS cell has a smaller width **(Fig. 8b)**, smaller thickness, and larger resistivity **(Table I)**, which affects the IR drop of the power mesh. We also considered the ideal case BSP with a large MB1 width. BSS chip has a 17 ~ 19 % higher IR drop than the BSP and 51 ~ 63 % higher than the BSP_ideal **(Fig. 9a)**. When the μBump pitch is a typical 40 μm [9], BSS has an IR drop of more than 100 mV, which is about 40 mV larger than the BSP_ideal. However, if a less than 20 μm μBump pitch is achieved through package innovation, the IR drop is very low even in the BSS chip. Even in the large BS power mesh pitch cases with a lot of spare space on the BS, BSS has a very low IR drop at the small μBump pitch **(Fig. 9b)**. Thus, a large power mesh pitch can be used, and it shows the potential of applying BSS inter-cell routing using BS spare space.

Chip PPA analysis: In all benchmarks with ideal power mesh, the BSS intra-cell routing based chip shows a smaller internal ($P_{internal}$) and switching power (P_{switch}) than the BSP based chip due to the improved FS routing space and reduced cell's C_{pin} and P_{int}, showing 4.1 ~ 4.7 % smaller total power consumption (P_{total}) **(Table III)**. Also, the BSS chip improves the worst (WNS) and total negative slack (TNS) and shows 4.7 ~ 5.3 % higher effective frequency ($Freq_{effective}$). Overall, the BSS chip shows 8.61 ~ 9.46 % PDP improvement for all benchmarks. Clearly, BSS intra-cell routing is a novel scheme that can improve the chip beyond BSP without concerns about power mesh IR drop and BS-pin design.

Conclusion: We unveiled PPA benefit of BSS inter and intra-cell routing scheme compared to BSP. BSS inter-cell routing improves RO, but BS-pin chip design is a concern. BSS intra-cell routing using FS-pin achieves lower EDP, especially for complex cells. At ideal bump pitch, the BSS chip shows low IR drop, and the BSS intra-cell routing based chip shows 8.61 ~ 9.46 % PDP reduction. Obviously, BSS intra-cell routing is a promising scheme beyond BSP that enables chip improvement without BS-pin design issue.

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References: [1] D. Prasad *et al.*, *IEDM*, 2019, pp. 446–449. [2] J. Lee *et al.*, *VLSI*, 2023, pp. 1-2. [3] S. Yang *et al.*, *VLSI*, 2023, pp. 1–2. [4] P. Vanna-iampikul *et al.*, *VLSI*, 2024, pp. 1–2. [5] J. Park *et al.*, *VLSI*, 2024, pp. 1–2. [6] M. Kobrinsky *et al.*, *IEDM*, 2023, pp. 1-4. [7] W. -L. Sung *et al.*, *IEEE TED*, vol. 68, no. 6, pp. 3124-3128, 2021. [8] V. Vashishtha *et al.*, *Microelectronics Journal*, 2022, pp. 1–2. [9] S. B. Samavedam *et al.*, *IEDM*, 2020, pp. 1–10.

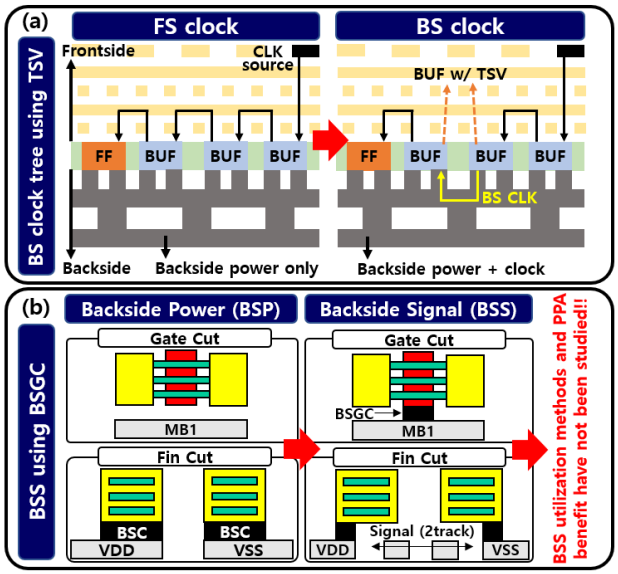


Fig. 1. Two different methods using BS region. (a) BS clock tree using nanoTSV, (b) BSS using BSGC.

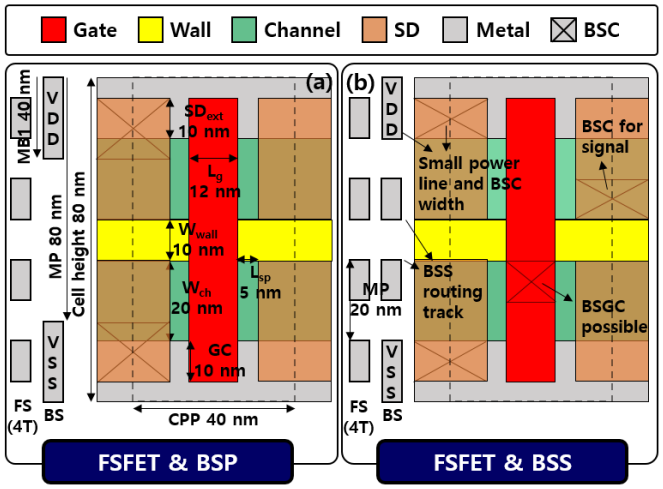
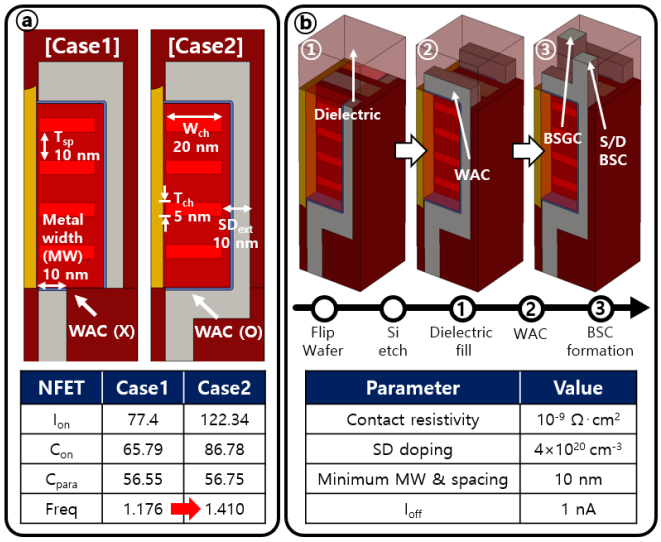


Fig. 2. Metal and layout configuration of (a) FSFET & BSP and (b) FSFET & BSS. For both cases, 4 metal tracks and FSFET with 80 nm cell height are assumed.



NFET	Case1	Case2
I_{on}	77.4	122.34
C_{on}	65.79	86.78
C_{para}	56.55	56.75
Freq	1.176	1.410

Parameter	Value
Contact resistivity	10^{-9} Ω·cm^2
SD doping	4×10^{20} cm^{-3}
Minimum MW & spacing	10 nm
I_{off}	1 nA

Fig. 3. (a) Two different BSC cases. BSC without WAC shows poor performance. (b) WAC and BSC process flow and key parameters of TCAD simulation. We assumed WAC for both BSP and BSS.

TABLE I. Assumption of MOL & BEOL metal layers and dielectric.

※ BSP: MB1 = 40 nm / BSP_ideal: MB1 = 70 nm

※ Aspect ratio of M1~M9 = 2, M0 = 3, MB1~MB3 = 1 (MB1, BSS = 2)

	Permittivity
LowK	2.7
Dielectric Barrier	4.8

	Liner	Material
M0	2 nm	Tungsten
M1~M3, MB1	1 nm	Cobalt
M4~M9, MB2~MB3	2 nm	Copper

		BSP	BSS			BSP	BSS
M0	Width (nm)	10		M8 ~ M9	Width (nm)	30	
	ρ (Ω·μm)	0.356			ρ (Ω·μm)	0.043	
M1 ~ M3	Width (nm)	10		MB1	Width (nm)	40/70	10/30
	ρ (Ω·μm)	0.189			ρ (Ω·μm)	0.103/ 0.084	0.189/ 0.127
M4 ~ M5	Width (nm)	15		MB2	Width (nm)	90/140	70
	ρ (Ω·μm)	0.073			ρ (Ω·μm)	0.029/ 0.025	0.032
M6 ~ M7	Width (nm)	20		MB3	Width (nm)	140	140
	ρ (Ω·μm)	0.057			ρ (Ω·μm)	0.025	0.025

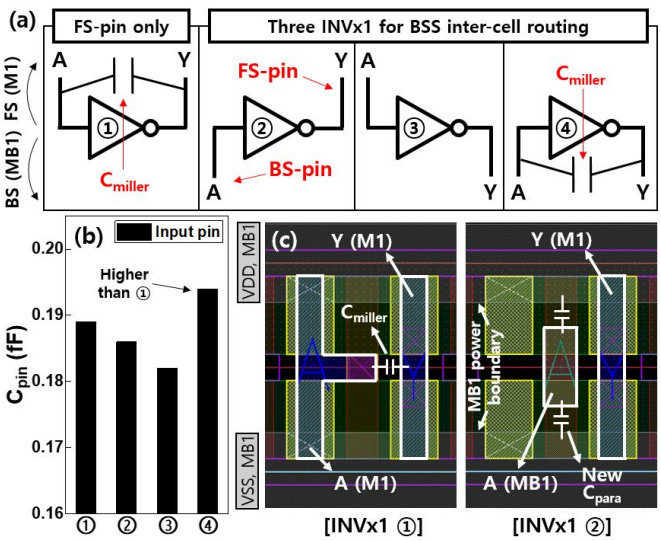


Fig. 4. (a) Four possible INVx1 designs considering FS and BS-pin. (b) Using both side (FS/BS) pins reduces C_{pin}. (c) Two INVx1 layouts have different pin configurations.

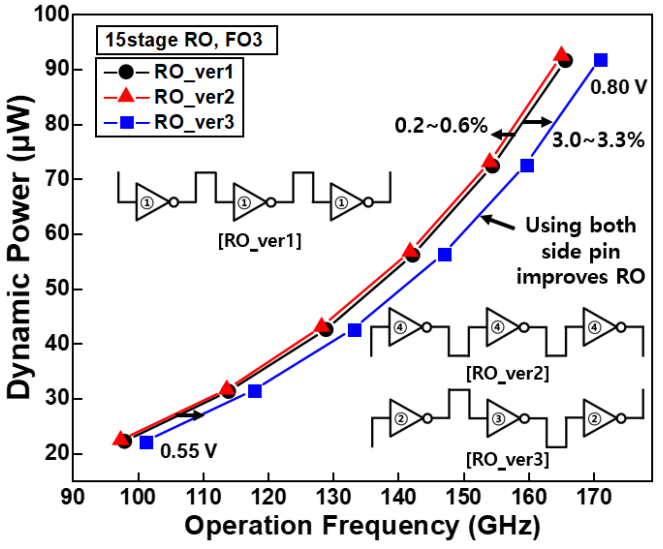


Fig. 5. 15stage RO (fan-out = 3) simulation results for different routing schemes. RO_ver3 effectively reduces C_{miller} and shows 3.0 ~ 3.3 % frequency improvement at iso-power.

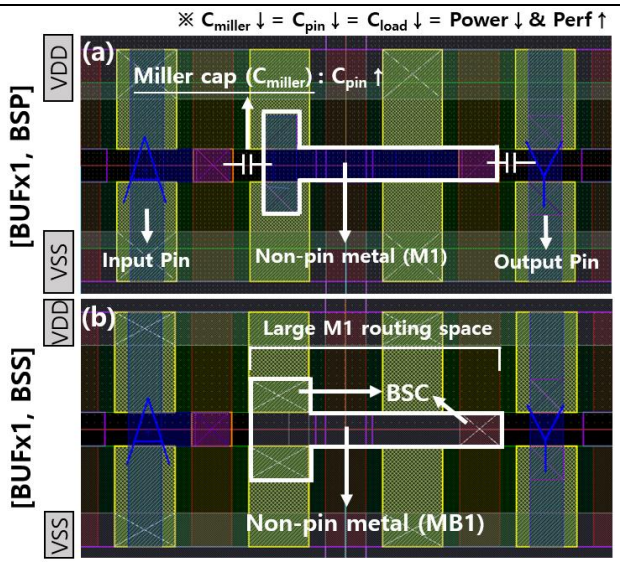


Fig. 6. BUFx1 layout with (a) BSP and (b) BSS intra-cell routing. BSS intra-cell routing can reduce the C_{miller} between the pin and non-pin metal. Also, the BSS cell secures additional M1 routing space.

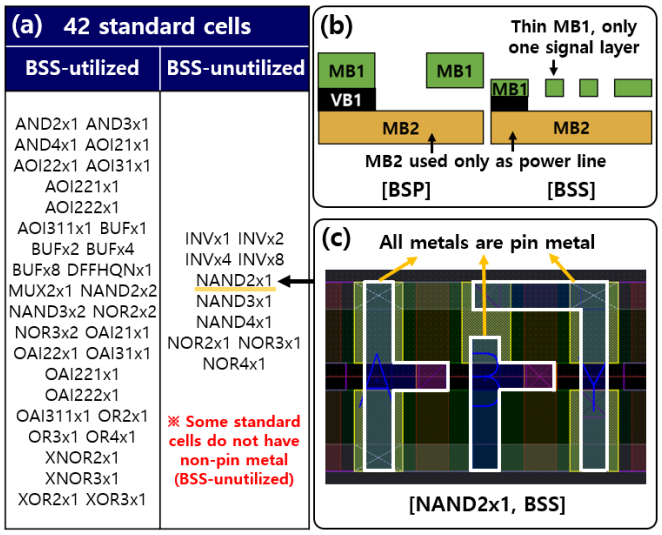


Fig. 7. (a) Distinction of BSS intra-cell routing utilized and unutilized standard cells. (b) BSS cell has a small and thin MB1 layer, and only MB1 has a BSS line. (c) Example of BSS-unutilized cell layout.

TABLE II. Comparison of BSP and BSS intra-cell routing based standard cells. BSS utilized cell shows smaller C_{pin}. Complex standard cell utilizing BSS shows a significantly improved EDP.

※ EDP Unit: 10^{-39} J·s

	INVx1		BUFx1		DFFHQNx1	
	BSP	BSS	BSP	BSS	BSP	BSS
Area	0.007	0.007	0.013	0.013	0.054	0.054
C_{pin} (fF)	0.189	0.189	0.187 →	0.183	0.195 (clk) →	0.186 (clk)
Fast case: Input slew: 10 ps Output cap: 1.44 fF						
Delay (ps)	7.96	7.96	8.70	8.70	15.92	15.70
t_{tran} (ps)	10.76	10.76	10.13	10.11	11.15	11.13
P_{int} (fJ)	0.01258	0.01255	0.04636	0.04628	0.2247	0.2172
EDP	797	795	3508	3502	5694 →	5353
Slow case: Input slew: 40 ps Output cap: 5.76 fF						
Delay (ps)	30.71	30.71	25.48	25.49	34.86	34.58
t_{tran} (ps)	42.11	42.11	38.79	38.76	39.17	39.15
P_{int} (fJ)	0.01749	0.01746	0.07154	0.07141	0.2504	0.2429
EDP	16494	16466	46446	46398	304290 →	290454

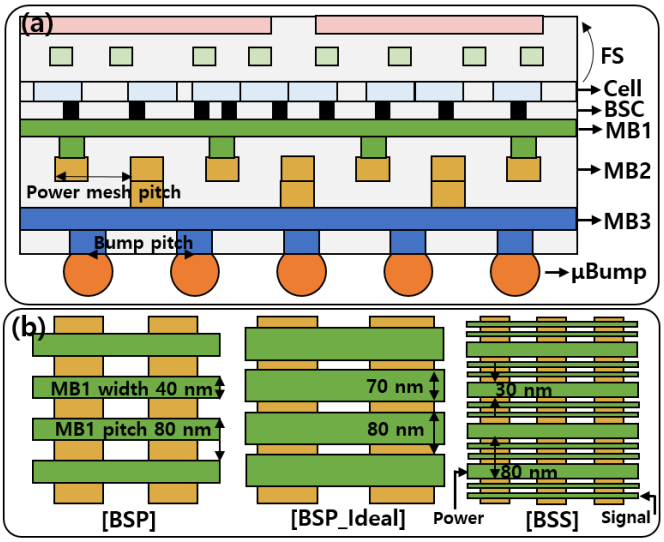


Fig. 8. (a) Cross-section that illustrates our chip configuration. MB1~3, µBump are considered. (b) Top view of MB1, MB2 power mesh for BSP, BSP_ideal, and BSS chips.

Pitch (µm), (BSP, BSP_ideal, BSS)	Case1	Case2	Case3
MB2 (V)	0.18, 0.28 ,0.14	0.5	1
MB3 (H)	0.28	0.5	1
µBUMP	10 ~ 40		

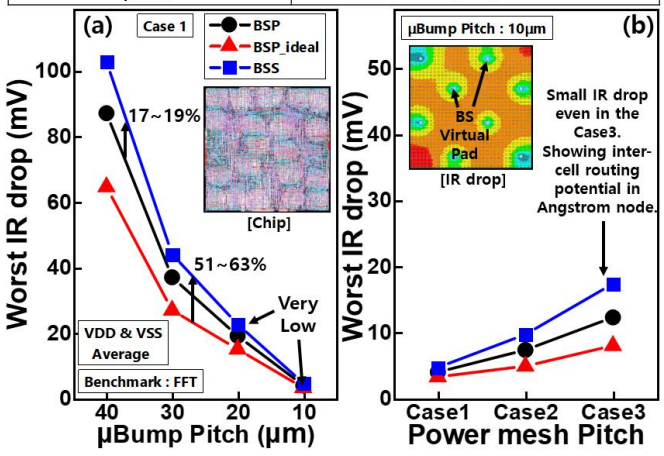


Fig. 9. (a) IR drop comparison of power meshes for different µBUMP pitches. (b) BSS has a higher IR drop, but even in the large power mesh pitch case, BSS shows a low IR drop at a small µBUMP pitch.

TABLE III. Power and performance metrics between BSP and BSS intra-cell routing based chip for various benchmarks. BSS chip improves P_{Total} & $Freq_{effective}$.

※ P_{Total}: $P_{internal}$ + $P_{switching}$ + $P_{leakage}$

※ Assuming ideal power mesh (low IR drop)

Chip	AES		JPEG		FFT	
	BSP	BSS	BSP	BSS	BSP	BSS
$Freq_{target}$ (Ghz)	6.67		2.78		4	
$P_{internal}$ (pW)	3.50	3.34	64.0	61.4	385	370
$P_{switching}$ (mW)	2.69	2.56	17.6	16.9	99.2	94.6
$P_{leakage}$ (mW)	0.023	0.023	1.06	1.02	2.17	2.13
P_{Total} (mW)	6.21 →	5.92	82.7 →	79.3	486 →	466
ΔP_{Total} (%)	-4.7 %		-4.1 %		-4.1 %	
WNS (ps)	-16.33	-8.44	-65.74	-47.18	-45.73	-31.19
WNS (% period)	-10.88	-5.62	-18.26	-13.11	-18.29	-12.48
TNS (ps)	-1080	-340	-9226	-8389	-2914	-1627
$Freq_{effctive}$ (Ghz)	6.01 →	6.31	2.35 →	2.46	3.38 →	3.56
$\Delta Freq_{effctive}$ (%)	+4.99 %		+4.7 %		+5.3 %	
ΔPDP (%)	-9.46 %		-8.61 %		-9.18 %	