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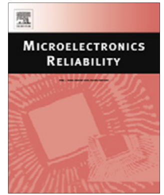

Backend dielectric reliability simulator for microprocessor system

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ABSTRACT

Backend dielectric breakdown is one of the major sources of wearout for microprocessors. We present test data and a methodology to accurately estimate the lifetime for a microprocessor system due to backend dielectric breakdown. Our methodology incorporates activity in the nets surrounding each dielectric segment in the layout, temperature, and all layout spacings among parallel tracks. We analyze several layouts using our methodology and show the impact of backend dielectric wearout on microprocessor system lifetime.

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1. Introduction

Each technology generation reduces the interconnect dimensions without always reducing the supply voltage in proportion. This results in higher electric fields within the backend dielectric. At the same time, as the dielectric constant (k) decreases to reduce parasitics, as prescribed by the *International Technology Roadmap for Semiconductors,* the porosity of materials must increase, at the possible cost of increasing the vulnerability of materials to breakdown. These factors combine to increase the risk of failure of chips due to backend dielectric breakdown in the newer technology nodes.

The standard approach to assess backend dielectric reliability is using process data. The typical test structure is a comb structure, as shown in Fig. 1a. In testing a comb structure, a voltage difference is applied between the two combs. The current between the combs is monitored to determine the time-to-failure (*TF*).

Test structures are stressed at high voltages and high temperatures to accelerate dielectric breakdown. Appropriate adjustments and extrapolations are made to the test results to scale them to operating conditions. In addition, corrections are also needed to account for the difference between the vulnerable area of the microprocessor and the test structure.

The physics describing backend IC failure mechanisms has matured as a result of years of refinement to existing theories. However, the extension of these models to large and complex microprocessor systems has not proven to be straightforward and is complex. Microprocessor system reliability analysis requires techniques to extend the results gathered from small test structures to large complex microprocessors. Such an endeavor includes methods to manage the deluge of data that comes with analyzing large layouts.

The purpose of this paper is to present a methodology to assess microprocessor lifetimes based on low-k TDDB test structure lifetimes, by developing the link between data collected from test structures and the microprocessor system. We demonstrate the feasibility of our methodology by presenting results from a simulator based on the proposed methodology.

Because backend dielectric breakdown is activity and temperature dependent, our methodology includes determining the stress for each dielectric segment of a microprocessor while running benchmarks and a method to estimate the temperature distribution for a microprocessor system by using a thermal modeling tool.

The ultimate purpose of our work is to introduce backend dielectric reliability in the design of a microprocessor system, by conveying to the designer accurate estimates of processor lifetimes, including the breakdown among layers and blocks, in a designer-friendly manner. This enables a designer to make any updates in the design to enhance reliability prior to committing a design to manufacture.

In this paper, we first summarize our methodology to estimate microprocessor lifetime, based on data collected from test structures, in Section 2. Section 3 discusses our test structures and test data. In Section 4, we outline our methodology to incorporate the microprocessor geometries, temperature profile, and stress conditions in the simulator. Section 5 gives an overview of the acquisition flow for thermal and electrical stress profiles. Next, in Section 6, we study the estimated lifetimes for the microprocessor system under study from our simulator, and we conclude the paper in Section 7.

2. Backend dielectric breakdown models and microprocessor lifetime estimation

The most important reliability concerns for interconnects are electromigration [1–4], stress-induced voiding [5–7], and time-dependent dielectric breakdown (TDDB) of the backend dielectric.

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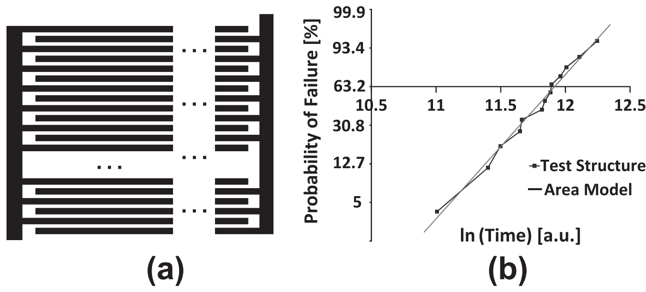

Fig. 1. (a) Comb test structure. (b) Data collected from comb test structure.

Our purpose is to consider only TDDB of the backend dielectric. Future work will add in these other wearout mechanisms.

2.1. TDDB models

We note that models that describe backend TDDB, although they may have been initially developed for device TDDB, are of the general form [8–11]

$$\ln \eta = A - \gamma E^{m} - E_a/kT \quad (1)$$

where A is a constant that depends on the material properties of the dielectric, γ is the field acceleration factor, m is one for the E model and 1/2 for the $\sqrt{E}$ model, and η is the characteristic lifetime. In this paper, only E and $\sqrt{E}$ models are considered. The electric field, $E = V/S$, is a function of voltage, V, and linespace between any two lines, S. A typical layout has a large number of linespaces. The temperature dependence is modeled with the Arrhenius relationship in Eq. (1) [10,12], where k is the Boltzmann constant, q is the electronic charge, ϕ_B is the trap barrier height, ε is the dielectric constant, π is a mathematical constant and the activation energy, $E_a \propto q(\varphi_B - \sqrt{qE/\pi\varepsilon})$, is field dependent.

Eq. (1) provides a correction between the electric field during use conditions and accelerated stress tests. Geometries with different line spacings scale differently to use conditions, as noted in [13,14]. Eq. (1) also provides a correction between chip operating conditions and accelerated stress conditions.

2.2. Microprocessor lifetime models

It should be noted that microprocessor systems wearout for a variety of reasons, both related to devices and interconnect. All of these wearout mechanisms happen simultaneously. It is common to describe reliability mechanisms with a Weibull distribution

$$P(TF) = 1 - \exp\left(-(TF/\eta)^{\beta}\right), \quad (2)$$

having two parameters: the characteristic lifetime, η, and shape parameter, β. The characteristic lifetime is the time-to-failure at the 63% probability point, when 63% of the population have failed, and the shape parameter describes the dispersion of the failure rate population. Typically, the shape parameter is close to one. If we have a collection of n independent wearout mechanisms modeled with Weibull distributions, having parameters, η_i, $i = 1, \ldots, n$, and β_i, $i = 1, \ldots, n$, then the characteristic lifetime of the system, $\eta_{processor}$, is the solution of [13,15,16]:

$$1 = \sum_{i=1}^{n} (\eta_{processor}/\eta_i)^{\beta_i} \quad (3)$$

Similarly [15],

$$\beta_{processor} = \sum_{i=1}^{n} \beta_i (\eta_{processor}/\eta_i)^{\beta_i} \quad (4)$$

The components in Eqs. (3) and (4) could be different wearout mechanisms, different layers of a microprocessor, different geometries within a layer, or different geometries within a layer at different temperatures. Hence, all a reliability simulator has to do is to (a) determine the characteristic lifetimes and shape parameters for all of the underlying wearout mechanisms and geometries, after all components are scaled for temperature and to use conditions with Eq. (1) and (b) apply Eqs. (3) and (4) to solve for $\eta_{processor}$ *and* $\beta_{processor}$.

3. The test structures and test results

3.1. The test structures

We have designed test structures to assess the impact of linespace and area on Cu/low-k TDDB. The details of the test struc-

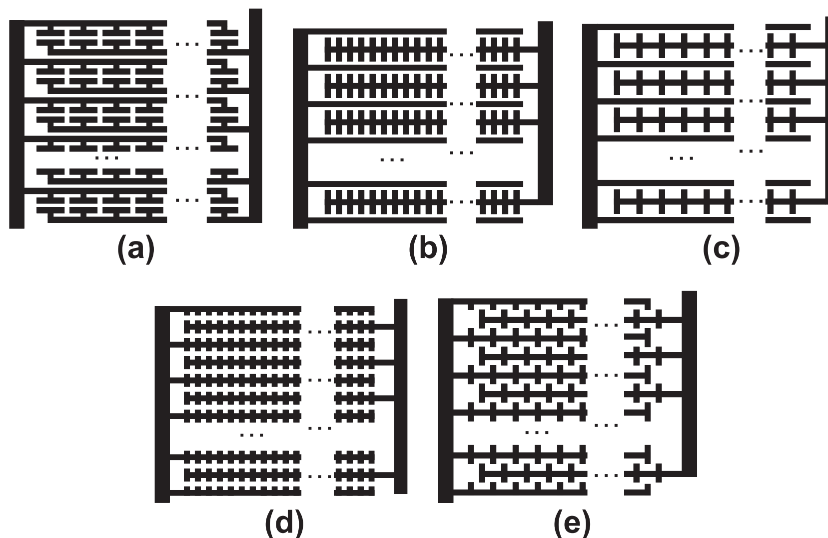

Fig. 2. Top views of test structures to characterize the impact of geometry on backend time-dependent dielectric breakdown. (a) Reference, (b) PTT, (c) TLa, (d) TLb, (e) TTa and (f) TTb.

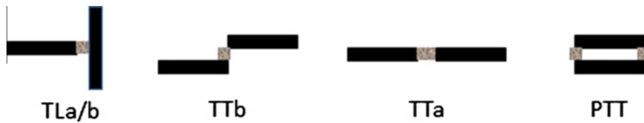

Fig. 3. Vulnerable line ends that need to be extracted from a layout.

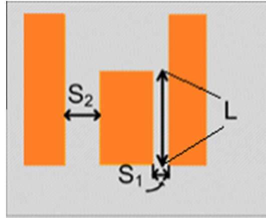

Fig. 4. Vulnerable area associated with a line space. The rectangles are Cu wires and the shaded area is the backend dielectric.

tures, their design and results, are given in [13,15,17]. The test structure in Fig. 1a is used to determine the lifetime of the dielectric between parallel tracks with a specific line spacing. This test structure has a fixed linespace, *S,* and vulnerable length, *L*. The vulnerable area is *LS.* To test the lifetime of such a feature, a voltage difference is applied between the two combs. The current between the combs is monitored to determine the time-to-failure. The data set from several samples is fit with a Weibull distribution to estimate η_t and β_t.

In previous work, we have shown that full chip lifetimes may be affected by irregular geometries [17]. We also take into account the impacts of those irregular geometries in this work. Fig. 2 shows the top views of these test structures and the fragments of these test structures are shown in Fig. 3.

The test structures were manufactured with an industrial 45 nm dual-damascene process and were tested at 3.6 MV/cm and at 150 °C, and a current limit of 10 μA between the lines was set to detect dielectric breakdown. This current limit detects hard failure. The increase in current at hard breakdown is very rapid, making the time-to-failure not very sensitive to the exact value of the current limit.

3.2. Test results

The data collected from the test structures is presented in [13,17]. We've extracted η_t and β_t by fitting the data with a Weibull distribution. Once these parameters have been determined for the unit area, the relationship between characteristic lifetimes for different areas is known.

4. TDDB lifetime simulator for microprocessor systems

4.1. Vulnerable area and full processor reliability simulation

The simulator operates by determining the vulnerable length of the microprocessor layout for each linespace. The vulnerable length is defined as the length of a block of dielectric between two copper lines separated by linespace S_i, illustrated in Fig. 4. A given layout is analyzed by determining the pairs (S_i, L_i) for each layer for all linespaces. The details of our methodology can be found in [13,15–17].

Next, after feature extraction, we compute feature-level Weibull parameters and combine these to determine the full-

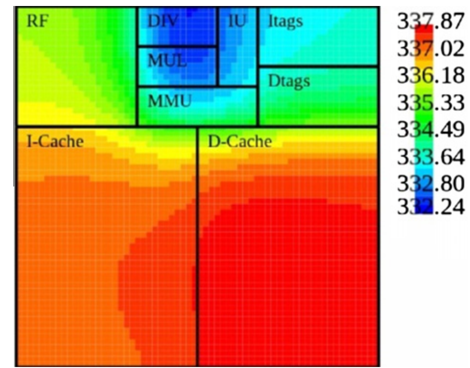

Fig. 5. Average temperature distribution for the microprocessor while running a set of standard benchmarks.

microprocessor lifetime parameters. Let η_t be the Weibull characteristic lifetime for a test structure with vulnerable linespace S_i of length L_t. Then, if the microprocessor has a vulnerable length, L_{ij}, associated with the same linespace, S_i, on the *j*th layer, the corresponding characteristic lifetime of the portion of the layer with linespace S_i is [13,15]

$$\eta_{ij} = \eta_t (L_t/L_{ij})^{1/\beta ij}, \quad (5)$$

where β_{ij} is the Weibull shape parameter for the *i*th linespace in the *j*th layer. If there is no test structure with the linespace, S_i, η_t is found using other test structures and the field acceleration Eq. (1).

Since each layer has many spacings, S_i, and a microprocessor has many layers, the characteristic lifetimes and shape parameters are combined with (3) and (4).

4.2. Vulnerable area and vulnerable feature extraction

We have developed our layout extraction tool using the standard object oriented programming language C++. The layout extraction flow is shown in Algorithm 1. Two inputs to the program are a layout *L* whose features are to be extracted and maximum line spacing, S_{max}. The program then outputs a table for vulnerable areas and vulnerable features (#TLa/b, #TTa, #TTb, #PTT). The detailed explanation of Algorithm 1 is given in [17].

4.3. Temperature modeling for microprocessor

The design under study was implemented on an FPGA board. For analyzing the impact of backend dielectric wearout on a microprocessor system, we have used the well-known open-source LEON3 IP core processor [18] with superscalar abilities. The microprocessor logic units consist of a 32-bit general purpose integer unit (IU), a 32-bit multiplier (MUL), a 32-bit divider (DIV) and a memory management unit (MMU). Storage blocks include a window-based register file unit (RF), separate data (D-Cache) and instruction (I-Cache) caches and cache tag storage units (Dtags and Itags).

For modeling the temperature distribution of a microprocessor, we collected the activity of nets of the system under study, based on running a series of standard benchmarks [19] on the system and used the temperature modeling tool HotSpot [20] to estimate the temperature distribution for every single unit of the microprocessor system. Fig. 5 shows the average temperature distribution when the microprocessor system is running a set of standard benchmarks.

Algorithm 1. The pseudocode of the layout extraction flow

Input: The maximum line spacing S_{max} and a layout L
Output: Tables of vulnerable areas (VulnerableAreaTable) and new features (TLab, TTa, TTb, PTT)
for each metal layer m do
  LineData (m) ← ReadLineSegments (L); // BucketSort
  TTa (m) ← 0; TTb (m) ← 0; PTT (m) ← 0; TLab (m) ← 0;
  c ← 1; n ← 2;
  while $c < N_{line}$ do // N_{line}: # lines in LineData
    L_1 ← LineData (m,c); // cth line
    L_2 ← LineData (m,n); // nth line
    PTT (m) + = CheckPTT (L_1, L_2); // check PTT between L_1 and L_2
    TTa (m) + = CheckTTa (L_1, L_2); // check TTa between L_1 and L_2
    TTb (m) + = CheckTTb (L_1, L_2); // check TTb between L_1 and L_2
    TLab (m) + = CheckTLab (L_1, L_2); // check TLab between L_1 and L_2
    if Spacing (L_1, L_2)< = S_{max} **then**
      VulnerableAreaTable (m) ← VulnerableArea (L_1, L_2);
      LineData (m) ← Split (L_1, L_2);
      Adjust (N_{line}, c, n);
    else c ← c+1;
      n ← n + 1;
    end
end

Including the temperature map in the layout statistics adds another dimension to the problem, because now we have to consider the different characteristic lifetimes at different temperatures for every linespace. If we have a collection of m different temperatures for a linespace, S_i, then the corresponding characteristic lifetime for the linespace is

$$\eta_{s_i} = \sum_m (1/\eta_m^\beta)^{-1/\beta}, \tag{6}$$

where η_m is the characteristic lifetime adjusted to the mth temperature from the test conditions of the test structure using Eq. (1).

Characteristic lifetimes for the microprocessor system can be calculated using Eq. (3) to combine the characteristic lifetimes for each linespace.

4.4. Activity profile

Not just temperature, but also the electric field affects the relationship between test conditions and use conditions. The relationship between test conditions and use conditions is given in Eq. (1). However, the test structure is stressed with DC stress while the microprocessor dielectrics undergo AC stress. Nonetheless, it should be noted that the backend dielectric TDDB under AC stress does not show recovery [21], as observed in bias temperature instability degradation, and lifetime relaxation or healing, as observed in degradation due to electromigration [1–4].

Dielectric segments of the microprocessor may undergo different signal activity factors for different benchmarks. In prior work [13,17], we assumed that any dielectric segment is under stress 50% of the time, i.e. $\alpha = 0.5$. Specifically, the signals on each side of a dielectric segment are the same 50% of the time and different 50% of the time. Therefore,

$$\eta_{ac} = \eta_{dc}/\alpha \tag{7}$$

where η_{ac} is the characteristic lifetime under use conditions, with a probability of stress of α, and η_{dc} is the characteristic lifetime under dc test conditions. Hence, in prior work, $\eta_{ac} = 2\eta_{dc}$.

In our current implementation, we compute the probability that each adjacent net has opposite voltages. Let's suppose that there are n different probabilities of segments being under stress, α_n, for linespace, S_i. Then the corresponding characteristic lifetime for linespace, S_i, under use conditions is

$$\eta_{s_i} = \eta_{dc} \sum_m (\alpha_n^\beta)^{-1/\beta}. \tag{8}$$

In this work, instead of assuming a fixed stress probability, we collect the activity profiles of each net within the microprocessor while running benchmarks. The microprocessor system includes 195 k nets which form around 21 million dielectric segments to be analyzed in the layout.

5. Electrical/thermal profile acquisition

The time-to-failure of TDDB is a function of device stress and the thermal profile. To get accurate lifetime results, a framework for the accurate acquisition of spatial and temporal thermal/electrical stress of the system was constructed. Fig. 6 summarizes the electrical and thermal profile acquisition flow. For activity tracking, the hardware RTL/netlist was synthesized for emulation on an FPGA, and counters were placed at the I/O ports, which track both the state probabilities and the toggle rates of the ports during application runtime, as illustrated in Fig. 7. A standard set of benchmarks were used as the applications for the analysis.

The I/O activities and the gate-level netlist were then used for activity propagation to each net in the design, depending on its logic behaviour, for a complete stress/transition probability profile of the internal nodes of the microprocessor under study. Thus we have the probability of a transition occurring at any node and the probability at each state, i.e. the probability at logic "1". It is this probability at logic "1" and logic "0" that we need to compute the probability that each dielectric segment is under stress. The

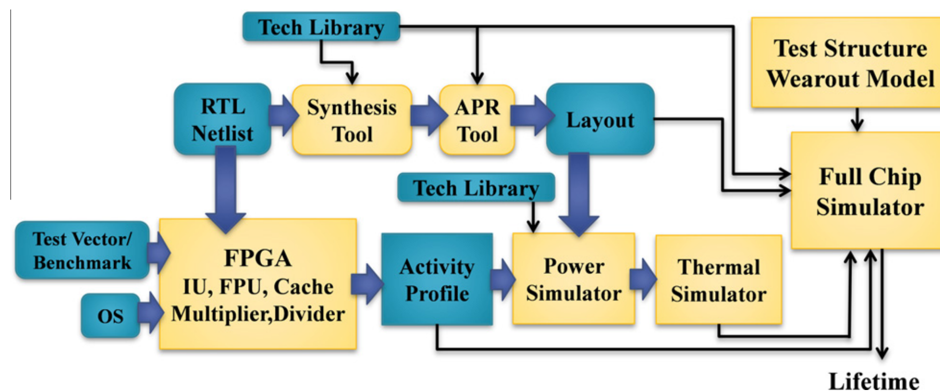

Fig. 6. The flow for extracting electrical and thermal profiles.

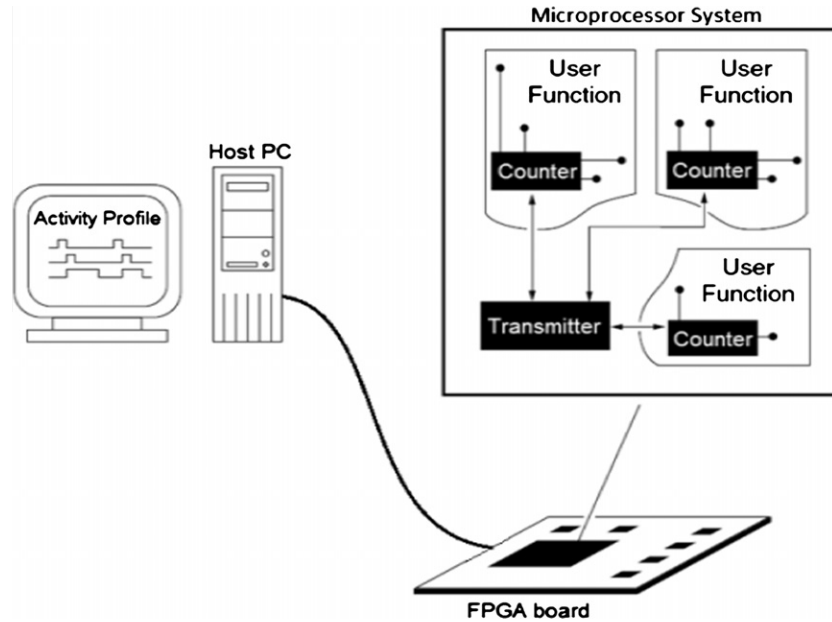

Fig. 7. The system to collect the activity profile of the microprocessor.

probabilities of dielectric stress of each dielectric segment then can be determined by

$$\alpha = \alpha_1(1 - \alpha_2) + \alpha_2(1 - \alpha_1), \tag{9}$$

where α is the probability of dielectric stress, α_1 and α_2 are the stress probabilities of each net, in each pair of nets which border the dielectric segments.

The netlist was also used for layout generation. The RC information from the layout, together with the net activity, was used for the extraction of the power profile and the consequent thermal profile, through the power simulator [22] and the thermal simulator [19], respectively, for every single unit of the microprocessor system.

Then, using the layout, the thermal profile and the calculated probability of voltage stress, we can use device level models to characterize TDDB in every unit of the microprocessor under study to estimate the lifetime of the system.

The runtime for the TDDB simulator is the sum of the time taken to extract features from the layout, propagate activities to each net in the design, and a constant time to evaluate Eqs. (3) and (4). Complexity of feature extraction and database extraction is $O(n)$, where n is the number of feature since bucket-sort is used. Complexity of extracting statistics from the features is also $O(n)$, because we scan the bucket from the bottom most element, and the maximum number of features within a fixed distance from an element is constant. Complexity of activity propagation is $O(n)$, where n is the number of gates in the system. Lifetime is estimated in constant time. Hence, the overall complexity of the TDDB simulator is $O(n)$.

6. Estimated lifetime for the microprocessor system

A set of standard benchmarks were run on the microprocessor system under study. The microprocessor includes around 20–25 k gates, while the runtime for executing a set of standard benchmarks on the system is around 15 min. The electrical and thermal profiles, together with the lifetime models from Section 4, were then used to estimate the lifetime of each functional unit in the microprocessor system.

The microprocessor system can be broken down into two distinct groups: the storage units and the combinational logic units. The storage units include the data cache, the instruction cache, the two cache units for tag storage, and the register file. The combinational logic units include the memory management unit, the integer unit, the multiplier, and the divider.

We have estimated the lifetime of each microprocessor unit and analyzed the lifetime for every metal layer in the design technology used, as shown in Figs. 8 and 9.

The lifetime of the system under study was clearly limited by the Metal1 layer, as seen in Figs. 8 and 9. As we move up in the metal layer stack, the metal spacing also increases, resulting in an increased time-to-failure. Our analysis shows that the data-cache and the instruction-cache were the lifetime limiting units in the microprocessor. On-line reconfiguration, through redundancy allocation, was not considered here, but could improve the lifetime of these units. Among the combinational blocks, lifetime was limited by the MMU and the IU, while the MUL and the DIV blocks had relatively better lifetimes. Figs. 5 and 8 clearly suggest a strong temperature dependence of the system lifetime.

From Figs. 8 and 9, we also can find that the estimated lifetimes for the “bitcnts” benchmark are longer than the estimated life-

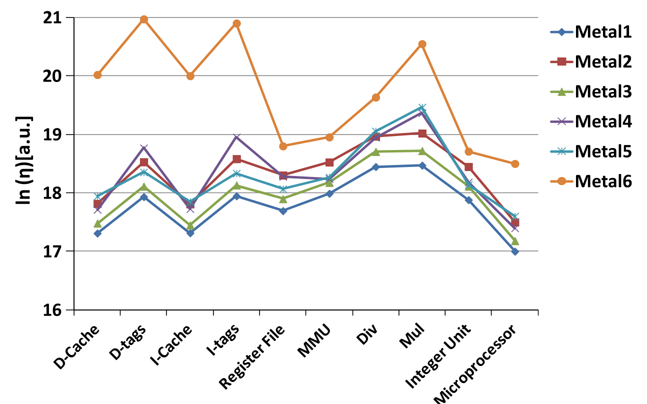

Fig. 8. Characteristic lifetimes for each layer and for each unit of the microprocessor system while running the “bitcnts” benchmark.

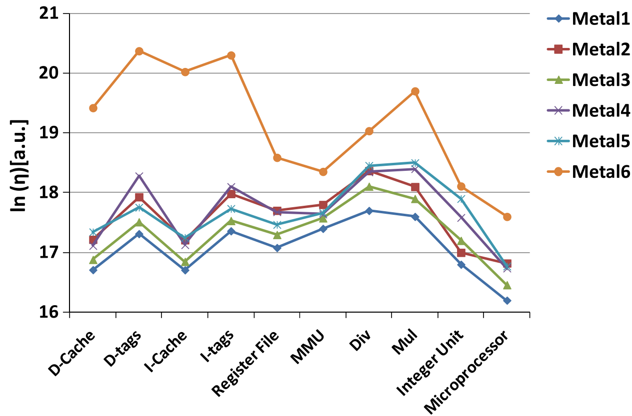

Fig. 9. Characteristic lifetimes for each layer and for each unit of the microprocessor system while running the "basicmath" benchmark.

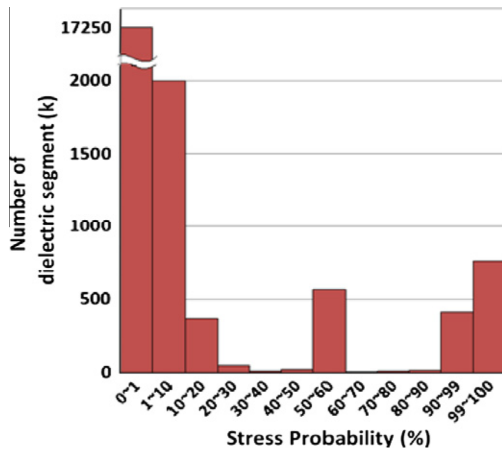

Fig. 10. Stress profile of the nets in the microprocessor while running the "bitcnts" benchmark.

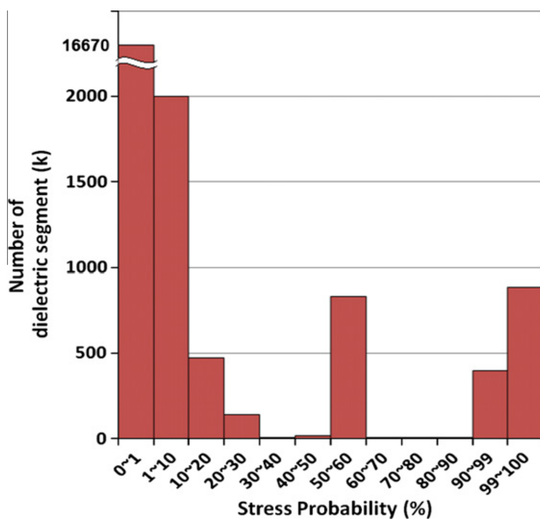

Fig. 11. Stress profile of the nets in the microprocessor while running the "basicmath" benchmark.

times for the "basicmath" benchmark. The reason may be that the stress probability of each dielectric segment is lower when the "bitcnts" benchmark is executed on the system. The stress probability distributions for the "bitcnts" and "basicmath" benchmarks are shown in Figs. 10 and 11, respectively.

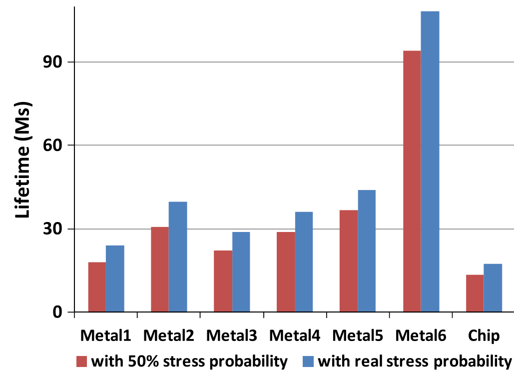

Fig. 12. Characteristic lifetimes for each layer of the microprocessor with 50% stress probability and with the real stress probability while running the "bitcnts" benchmark.

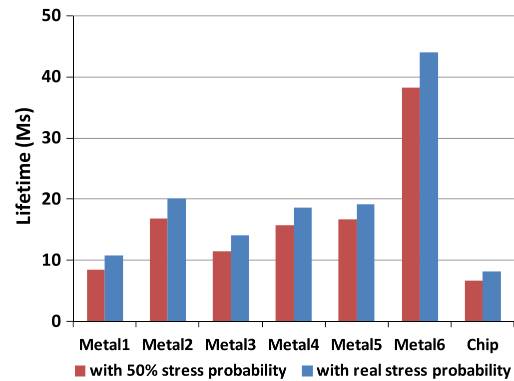

Fig. 13. Characteristic lifetimes for each layer of the microprocessor with 50% stress probability and with the real stress probability while running the "basicmath" benchmark.

However, electrical stress also plays an extremely important role in determining the lifetime. The assumption of a fixed stress probability for each net is inaccurate, as seen in Figs. 10 and 11. Contrary to our earlier assumption of a stress probability of 0.5, most dielectric segments have stress probabilities of ∼0 or ∼1. The use of accurate electrical stress and thermal profiles through the proposed methodology is expected to result in improved system backend lifetime estimates. The new lifetime figures, as shown in Figs. 12 and 13, indicate that the assumption of fixed activity levels [17] might lead to an underestimation in lifetime numbers of up to 35%.

7. Conclusion

This paper presents a flow to obtain the thermal and electrical stress profiles from microprocessor systems while running standard benchmarks. Taking into account the detailed thermal and electrical stress profiles, a methodology was proposed to accurately assess state-of-art microprocessor reliability based on the backend TDDB wearout mechanism. The methodology relies on the link between the device level wearout models and the chip layout. It takes into account the architecture through the temperature and activity profiles. Combining the wearout model, the thermal profile, and the electrical stress profile, this work provides insight

into the backend TDDB-critical microprocessor functional units for the whole system through using standard benchmarks.

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