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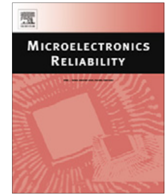

Impact of irregular geometries on low-k dielectric breakdown

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ABSTRACT

Backend geometries on chips contain a wide variety of features. We are developing a full-chip reliability simulator for low-k dielectric breakdown that takes into account the vulnerable area, linewidth, vias, and line edge roughness. The simulator provides a link between test structure results and predictions of chip dielectric lifetime. However, these factors may not be sufficient for large chips with a wider variety of features. In this paper, we analyze data from backend dielectric test structures with irregular geometries to determine if more layout features need to be added to a full-chip reliability simulator for low-k dielectric breakdown.

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1. Introduction

Low-k time-dependent dielectric breakdown (TDDB) is an important reliability issue during Cu/low-k technology development and its qualification. With increasing porosity Cu/low-k interconnect systems are more vulnerable to breakdown, and reduced supply voltage scaling with respect to feature size has led to exponentially increasing electric fields among interconnects every technology generation, aggravating low-k dielectric breakdown.

Low-k dielectric breakdown is typically measured with comb test structures. A voltage difference (V) is applied to the combs, such as shown in Fig. 1, which creates lateral stress, electric field ($E = V/S$), across the dielectric between the fingers of the comb, separated by the line space, S. A cross-section of the dielectric under stress is shown in Fig. 2.

Hence, it is a common assumption that the vulnerable area for backend dielectric breakdown for a full chip is the area between minimum spaced lines. However, in prior work, we have shown that it is necessary to take into account all areas with different line spaces. If only the area between minimum spaced lines is considered, as suggested in [1], lifetime estimates will be inaccurate, as illustrated in Fig. 3 for an example circuit. Instead, the most frequent line space (i.e. the critical line space) provides a better estimate of lifetime for a layer.

In addition to the vulnerable area [4], we have found that lifetime depends on linewidth [5], even when the line space is constant, due to aspect ratio dependent etch (ARDE) [6,7]. Others have demonstrated dependencies on the presence of vias [8] and line edge roughness [9].

In our work, we have integrated all of these factors into a backend dielectric breakdown simulator [5]. The simulator provides a link between test structure results and predictions of chip dielectric lifetime.

As the number of unique features in a layout increases, because of challenges in reducing the wavelength in lithography, the layout geometries that we have considered so far may not be sufficient. In fact, 193 nm lithography has been used for at least five technology generations and the domain of influence of lithography now extends well beyond the nearest feature and the nearest neighboring cell in a standard cell design. The ability to print smaller geometries has been accomplished through a variety of mask engineering techniques. The mask engineering techniques, nevertheless, cannot guarantee that a layout will result in a circuit that yields adequately due to modeling errors and algorithmic inaccuracies. In fact, only lithography (and only the aerial image) and chemical mechanical polishing (CMP) have reasonably accurate process models [10]. Other models are empirical and calibrated to rapidly changing processes. Hence, design rule clean layouts have been known to yield poorly due to unanticipated layout geometries [10]. Therefore, it is important to consider the impact of these irregular geometries on backend dielectric breakdown.

In this paper we analyze data from backend dielectric test structures with irregular geometries to determine if more layout features need to be added to our reliability simulator, beyond area, linewidth, vias, and line edge roughness.

This paper is organized as follows. In the next section, we begin by describing the models that we implemented in our simulator. Section 3 summaries the test structures used in this study and the data collected from the test structures. Section 4 analyzes the data that we have collected to determine if the impact is significant and different than geometries previously considered. Section 5 considers the impact of failures in these irregular geometries for a full chip, and Section 6 concludes the paper with a summary.

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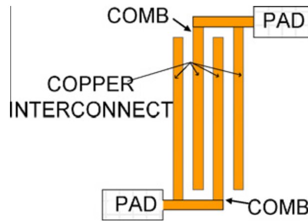

Fig. 1. Top view of a comb test structure.

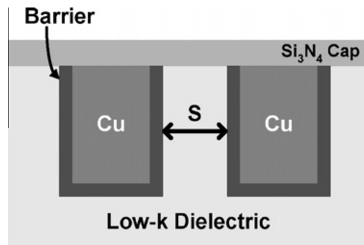

Fig. 2. Cross-section of an example copper/low-k interconnect system.

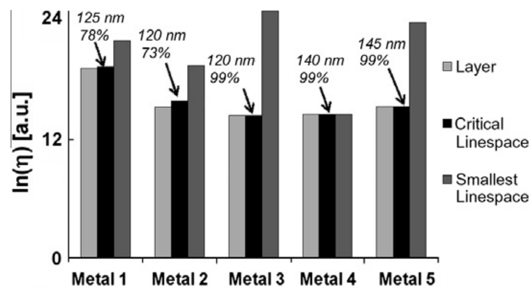

Fig. 3. Lifetime for each layer of an example circuit, taking into account all line spaces, the most frequent line space (critical line space), and the smallest line space. The critical line space and it's percentage in the layout is also given [2,3].

2. The simulator

2.1. Vulnerable area

The simulator operates by determining the vulnerable area of the chip layout. In essence, our simulator extrapolates test structure results to the entire product die. The vulnerable area is defined as the area of a block of dielectric between the two copper lines separated by linespace S_i for length L_i and having an area S_iL_i. The feature that is extracted from layouts is the vulnerable length between two lines L_i associated with a linespace S_i, which is a function of the widths of the two adjacent lines, $W_{i,L}$ and $W_{i,R}$, illustrated in Fig. 4. A given layout is analyzed by determining the pairs ($S_i(W_L, W_R)$, L_i) for each layer for all linespaces surrounded by the linewidths W_L and W_R.

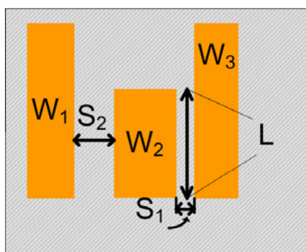

Fig. 4. Vulnerable area associated with a line space. The rectangles are Cu wires and the shaded area is the backend dielectric.

2.2. Computing Weibull parameters by combining feature-level Weibull parameters

Let η_t be the Weibull characteristic lifetime for a test structure with vulnerable linespace S_i of length L_t, and area $A_{it} = L_tS_i$. Then, if the chip has a vulnerable length L_{ij} associated with the same linespace S_i, and area $A_{ij} = L_{ij}S_i$, on the jth layer, the corresponding characteristic lifetime of the portion of the layer with linespace S_i is [2,3]

$$\eta_{ij} = \eta_t (A_{it}/A_{ij})^{1/\beta_{ij}}, \tag{1}$$

which is equivalent to

$$\eta_{ij} = \eta_t (L_t/L_{ij})^{1/\beta_{ij}}, \tag{2}$$

where β_{ij} is the Weibull shape parameter for the ith linespace in the jth layer.

A layer has many different line spacings, S_i. To combine the failure rates for all line spacings, we solve [2,3]

$$1 = \sum_i (\eta_j/\eta_{ij})^{\beta_{ij}}, \tag{3}$$

for the characteristic lifetime of the jth layer η_j. Similarly, the shape parameter for a layer is [3]

$$\beta_j = \sum_i \beta_{ij} (\eta_j/\eta_{ij})^{\beta_{ij}}. \tag{4}$$

The characteristic lifetimes of the layers are then combined together, and the overall characteristic lifetime, η_{chip}, is the solution of [2,3]

$$1 = \sum_j (\eta_{chip}/\eta_j)^{\beta_j}. \tag{5}$$

Similarly [3],

$$\beta_{chip} = \sum_j \beta_j (\eta_{chip}/\eta_j)^{\beta_j}. \tag{6}$$

Temperature is incorporated in the results by linking temperature to the characteristic lifetime [2]. Example simulation results with and without temperature are shown in Fig. 5.

The presence of line edge roughness is included in the simulator since the impact of line edge roughness is included in test structure data. The presence of vias is currently not included, because of the lack of stress test data.

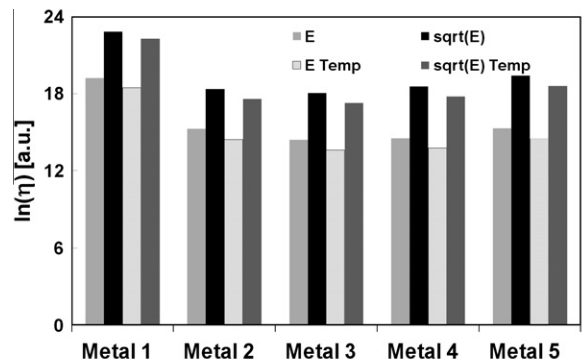

Fig. 5. Characteristic lifetime for all layers of an example circuit with and without temperature modeling and with both the E and $\sqrt{E}$ model.

All results are scaled to use conditions. This is done with one of the two dominant models for dielectric lifetime, the E model [11] and the $\sqrt{E}$ model [12,13].

As can be seen, the simulator does not account for any field enhancement due to non-ideal layout features, induced by imperfect optical proximity correction, and unexpected physical non-idealities that may follow because of this.

3. The test structures and measurement data

3.1. The test structures

In previous work, we have shown that there can be substantial field enhancement at tips and bends of irregular geometries [14]. Some geometries have been shown to increase the electric field within the dielectric by as much as a factor of three. Such field enhancement may lead to reduced lifetimes.

We have designed test structures that have several irregular features in order to determine any impact of field enhancement. Fragments of the test structures are shown in Fig. 6. PTT emphasizes the electric field between parallel routing tracks that end at the same point. TLa and TLb emphasize the electric field between line ends and perpendicular lines. TLb includes additional fringing fields, since the line ends are more widely spaced. TTa and TTb emphasize electric fields between line ends. In TTa, the line ends abut, and in TTb the line ends are in parallel tracks. TLa, TLb, TTa, and TTb have 528 line ends each. The separation between line ends is the same for all test structures.

The test structures were tested like comb structures. A voltage difference was applied to create a stress ranging from 0.75 MV/cm to 2.5 MV/cm and the current between the lines was monitored. A current limit of 10 μA was set to detect dielectric breakdown.

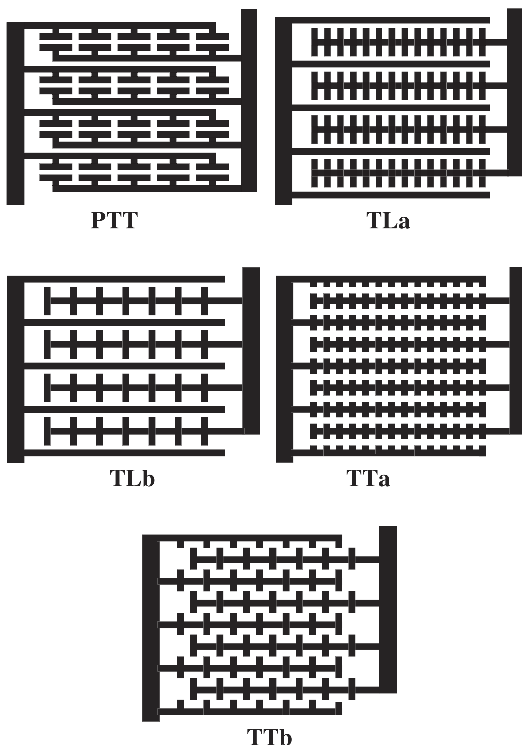

Fig. 6. Test structures to characterize the impact of irregular geometries on backend low-k TDDB.

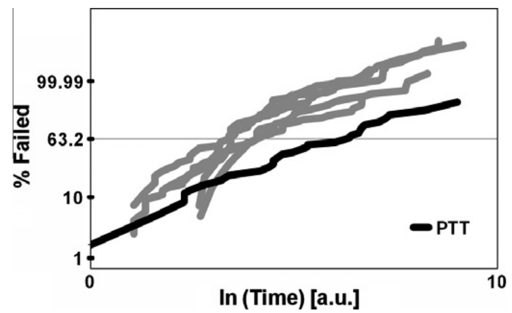

Fig. 7. Data collected from PTT in Fig. 6 showing that PTT has a longer lifetime than the standard distribution.

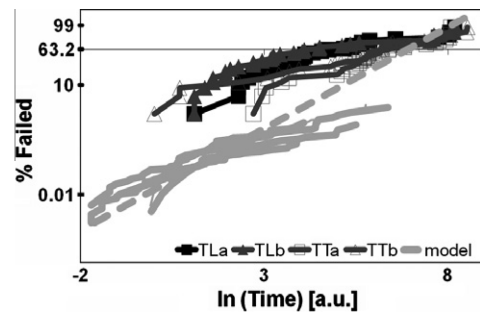

Fig. 8. Failure distributions for test structures in Fig. 6. These structures show worse lifetimes when compared with the standard failure distributions.

3.2. The measurement data

If the test structures provide no new information beyond the "vulnerable area" calculated by the simulator, then the relevant features would not need to be extracted from the layout and included in the simulator. To test if there is additional information, the measured Weibull curves are compared with those from standard comb test structures with the same line space, area scaled – by using the Poisson area scaling invariance of the Weibull distribution – to match the vulnerable length of the test structures in Fig. 6.

The results are shown in Figs. 7 and 8. Each plot compares the Weibull curves for the test structures with area scaled versions of standard comb test structures with the same line space. Adjustments were made for differences in testing conditions, using the $\sqrt{E}$ model. As can be seen from Fig. 7, the data for PTT appears to be better than the reference distribution. It is worse for TLa, TLb, TTa, and TTb than the reference distribution, as can be seen from Fig. 8. The gray curves in Figs. 7 and 8 are the failure distributions for the standard comb test structures.

4. Data analysis

It can be seen that the lifetimes for PTT are better than the equivalent standard structure with the same area. This is most likely due to pull-back at the ends of the lines, increasing the space between the line ends.

In order to understand the expected lifetime of the standard structures in Fig. 8, we note that in prior work we showed that our Weibull curves have curvature due to die-to-die variation [4]. We extract the extent of die-to-die variation by optimizing the fit between the data and model by considering the variation of lifetime with linespace [4]. We found that the 50% probability point of the Weibull curve is not affected by die-to-die variation. Therefore,

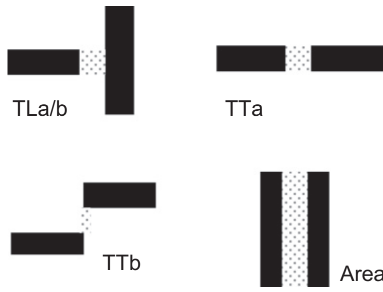

Fig. 9. Vulnerable areas (the dotted pattern between the lines).

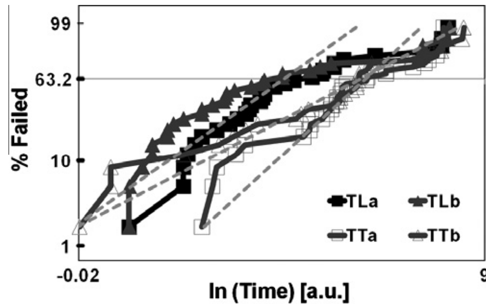

Fig. 10. Data and models for test structures in Fig. 6.

we have used the known die-to-die variation, the lifetime at the 50% point, and the best fit value of β to create a model for the standard Weibull curves. It is shown as the dashed line in Fig. 8. The data indicate that all of the line ends create an increased vulnerability for TLa, TLb, TTa, and TTb. Hence, the simulator needs to include a count of line ends with these geometries when estimating the wearout of a full chip. These geometries are illustrated in Fig. 9.

TLa, TLb, TTa, and TTb have the same number of line ends. TLb has a slightly worse lifetime than TLa. This is due to the larger spacing between the line ends. This difference is not statistically significant. However, TTa has a significantly better lifetime than TLa and TLb. Most likely this is due to pull-back. Specifically, if TLa and TLb experience pull-back, then TTa experiences twice the pull-back.

A model was extracted for TLa/b, TTa, and TTb. To eliminate the impact of die-to-die variation, we used the extracted data of die-to-die variation in [4] and curve fitting to find the best fit for β. The data and models are shown in Fig. 10. The models for TLa and TLb are combined because of the similarity of the geometries involved.

5. Inclusion of line end field enhancement in full chip reliability simulation

The line ends, with the three geometries shown in Fig. 9, each add additional parameters, $\eta_{TLa/b}$, $\beta_{TLa/b}$, η_{TTa}, β_{TTa}, η_{TTb}, and β_{TTb} to (2) and (3). These parameters depend on the number of minimally spaced line ends in each category of the layout.

Let's consider the computation of $\eta_{TLa/b}$ for the sake of illustration. Let's suppose the test structure has N_{test} minimally spaced line ends, from which η_{test} and $\beta_{TLa/b}$ are computed, as shown in Fig. 10. Then, for a layout with N_{chip} similar line ends, by area scaling

$$\eta_{TLa/b} = \eta_{test}(N_{test}/N_{chip})^{1/\beta_{TLa/b}}. \quad (7)$$

It should be noted that only the smallest values of η_{ij} influence the failure rate of a chip. Hence, layout style can significantly influence the vulnerability of a chip to line ends. Our data indicates that the lifetime for 43 line ends of type TLa/b, 162 line ends of type TTa, or 251 line ends of type TTb is equivalent of our minimum area comb test structure used for area scaling analysis in [4]. This indicates that line ends are likely to have a significant impact on chip lifetime.

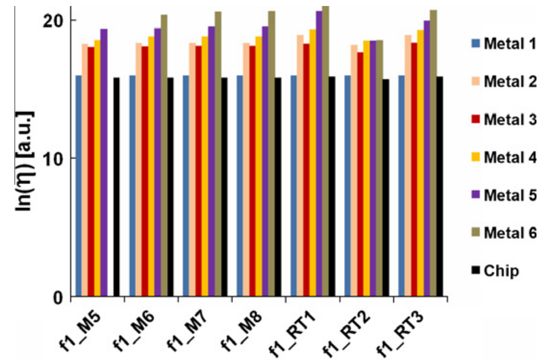

Fig. 11. Backend low-k chip reliability of different instantiations of a 256-pt FFT circuit taking all geometries in Fig. 9 into account.

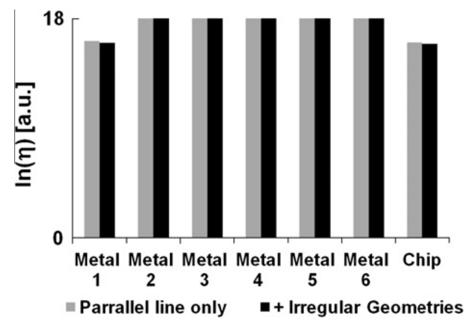

Fig. 12. Reliability for individual metal layers and chip reliability for *f1_RT3* considering only the dielectric between parallel lines (gray) and considering also the dielectric between perpendicular lines (black).

We assess the impact of irregular layout geometries by considering large scale circuits. We use NCSU 45 nm PDK for synthesizing different instantiations of a 256-pt Fast Fourier Transform (FFT) circuit. The minimum linespace and linewidth are 65 nm for Metal 1, 70 nm for Metal 2, 140 nm for Metals 4 through 6, 400 nm for Metals 7 and 8, and 800 nm for Metals 9 and 10. Synopsys Design Compiler was used for synthesis [15]. Cadence SoC Encounter was used for placement, clock-tree synthesis, routing, optimization, and RC extraction [16]. Synopsys PrimeTime was used for timing analysis [17]. We created seven different instantiations of the circuit. Our metrics for layout optimization are the number of layers in a circuit and its timing performance. Circuits *f1_M5*, *f1_M6*, *f1_M7*, and *f1_M8* are used to isolate the impact of the number of layers on reliability. Circuits labeled 'M' use Metal 1 to Metal '*X*' during routing. Circuits *f1_RT1*, *f1_RT2*, and *f1_RT3* are used to analyze the impact of timing performance on reliability. In RT '*Y*', we optimize timing using buffer insertion and gate sizing. M '*X*' does not do this. More aggressive timing optimization with a higher clock frequency is associated with a higher value of '*Y*'. The details of layout processing are given in [5].

The lifetimes for the instantiated circuits, considering all the geometries in Fig. 9, are shown in Fig. 11.

We have also compared the lifetime considering only area vs. all features in Fig. 9. Fig. 12 compares lifetimes of individual layers with and without the inclusion of degradation in lifetime due to TLa/b, TTa, and TTb for the layout of *f1_RT3*. Fig. 12 shows that there is a negligible difference, with Metal 1 showing the biggest difference in lifetime.

For *f1_RT3*, the increase in the vulnerable dielectric area due to irregular geometries is less than 5%. Layers above Metal 2 show less than a 1% increase in the vulnerable area; Metal 2 shows a 7% increase in the vulnerable area; and Metal 1 shows a 33% increase in vulnerable area. Most of this increase in vulnerable area was at large spacings. Similar results were obtained for the other circuits used in the study.

There are numerous TTa type geometries on Metal 1 and above. However, TTb type geometries rarely (or never) occur above Metal 1. TLa/b essentially consists of two perpendicular wires. In general, each metal layer has a preferred routing direction, either horizontal or vertical. Such layers are used for global routing. Therefore, TLa/b-type vulnerable areas above Metal 1 were rare. However, our layout extractor showed that TLa/b was frequently found on Metal 1. Metal 1 is used in cell libraries for internal wiring. Nevertheless, as the ratio between the technology node and the lithographic wavelength continues to shrink, it is likely that TLa/b geometries will not longer be allowed [10].

6. Conclusions

The impact of irregular geometries in backend low-k TDDB was studied and found to be significant. These geometries can potentially impact chip lifetime and need to be separately extracted and included in a backend low-k chip reliability simulator.

These test structures can also prove useful in decoding the mystery of the field dependence of backend low-k TDDB. Since such test structures have small dielectric areas under stressed, the probability of other defects modulating the test results is reduced. Thus, future work will look into additional data collected from these test structures subjected to long term stress tests at low voltages.

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