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Design and Analysis of a Stochastic Flash Analog-to-Digital Converter in 3D IC technology for integration with ultrasound transducer array

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ABSTRACT

This paper presents a stochastic flash analog-to-digital converter (ADC), implemented in a three-dimensional stacked technology. Due to vertical stacking, the 3D technology reduces the ADC footprint area, and a power consumption benefit for the 3D ADC is demonstrated compared with the 2D design. An all digitally synthesized stochastic 3D ADC was implemented using 130 nm GlobalFoundries device technology and Tezzaron through-silicon-vias (TSV) technology. Different TSV insertion methods were used and compared. A 20% improvement in power consumption is observed in the 3D implementation compared with the 2D counterpart. Thanks to the vertical stacking dies, a 40% footprint reduction is achieved in the 3D implementation. Two different integration topologies for 3D ADC and an ultrasound transducer arrays are considered and compared. Either the circuit dies are facing up, resulting in a face-to-face bonding between the transducer arrays and the three dimensional integrated circuit (3D IC), or the 3D IC dies are facing down, resulting a face-to-back connection. The simulation results show that the 3D face-up integration suppresses the TSV coupling noise to the analog input by around 10 dB.

1. Introduction

Three-dimensional integrated circuit technology has offered advantages in miniaturizing the footprint and reducing power consumption [1]. Recently, CMOS imagers [2–4] and ultrasound imaging systems [5,6], have exploited the 3D design by stacking a sensor layer and the analog/digital design layer into two different stacking dies. The system principals for most of these sensors are essentially the same, as each sensor node requires a receive path consisting of some layers of sensors array, low noise amplifiers (LNA), analog to digital converters (ADC), and a processing element unit. In 3D IC design, the layers are distributed and connected vertically via TSVs (See Fig. 1).

Capacitive micro-machined ultrasonic transducers (CMUTs) have emerged as an alternative to piezoelectric transducers for their flexibility and ease of fabrication [5]. The CMUT ultrasound technology offers advantages such as better bandwidth, better integration with electronics with TSV and flip chip bonding [6] or monolithic integration [7]. Some previous works demonstrate the 3D stacking of CMUT flip-chip bonded with the front-end ICs, in which a 2D integrated circuit is connected to a 2D transducers array to perform signal processing. Combining the flip-chip integration of the ultrasound transducers array and the 3D IC, allows better utilization of a large ultrasound array. In this paper, a 3D ADC design is presented for the integration with flip-chip pads of a CMUT transducer array [5].

A digitally synthesized stochastic flash ADC is implemented in 3D stacked technology. In stochastic ADCs, comparator redundancy is used to exploit the large random variation in the comparator offset. This helps to relax the matching requirement for the circuit and yet achieve the performance required. This is highly valued in scaled down CMOS technologies, where the noise and the mismatch start to become a major challenge. In [8–10] the large random variation in the comparator offset was exploited in such a way that the number of comparators evaluating high follows a cumulative density function of a Gaussian comparator offset, which is close enough to an ADC transfer function. This technique has some benefits as first, it eliminates the need for a power consuming offset calibration unit. Second, a high precision resistor ladder is eliminated from the design, which allows the whole design to be implemented using digital synthesis flow.

The 3D stochastic flash ADC implementation brings some benefits as follows: First, the footprint area of a the 3D IC is smaller than the 2D counterpart [11]. This further satisfies the need for a miniaturized design, especially in the front-end circuit receiver system, where large arrays of ultrasound transducers exist. Second, the footprint shrinkage results in much shorter interconnects, which in turn, reduces the power consumption due to smaller

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interconnect parasitics. The power reduction is more significant in the standard-cell based digital design with the minimum sized devices, where the interconnect parasitics power becomes dominant. Lastly, separating the noisy digital and the sensitive analog circuits helps to eliminate the noise coupling via the conductive substrate.

In the 3D IC circuit design, the coupling to/from TSVs must be considered. In analog/mixed signal ICs, the TSV coupling effect causes coupling noise disturbance and degrades the performance of sensitive analog devices [12,13]. In this paper, two different 3D stackings for the integration of the transducers array and the 3D IC electronics are considered. The coupling noises coupled to/from the TSVs and silicon substrate, under different 3D structures are compared [14].

The contributions of this work are as follow: (1) 3D IC integration with ultrasound transducers array was studied for the first time and the implementation flow for the two different 3D stacking schemes in [14] is explained. (2) A scalable stochastic flash ADC was proposed for the variable gain ADC design in an ultrasound signal receive path. (3) A 3D implementation of a stochastic flash ADC was presented using a fully synthesized digital flow using all the standard digital tools. Some additional in-house tools were leveraged to implement the TSV insertion for the 3D IC implementation, where different TSV insertions methods were used and compared.

The rest of this paper is organized as follows: Section 2 presents the stochastic flash ADC concept. A scalable variable gain stochastic ADC was proposed for the ultrasound applications. Section 3 presents and compares the design flow for the implementation of stochastic flash ADC in 2D and 3D technology. Section 4 presents the TSV coupling analysis in two stacking integrations of the transducer arrays with the 3D ADC circuit. The full chip design layout along with the simulation results are presented in Section 5. The conclusion is given in Section 6.

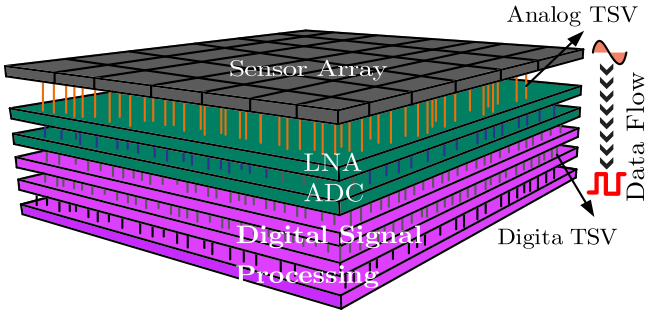

Fig. 1. Conceptual diagram of the 3D ultrasound stacked system.

2. Standard cell based variable gain stochastic flash adc design

2.1. Stochastic flash architecture and operation

In a conventional flash ADC, the input signal is connected to a group of comparators, in which the threshold of each comparators is set precisely to be 1 LSB by a resistor ladder. Similarly, in a stochastic flash ADC, the input signal is connected to a comparator bank. However, the threshold, instead of being precisely set, is allowed to be random, (see Fig. 2). For a given input voltage, some of the comparators evaluate one and the rest stay at zero. The total number of comparators that evaluate high increases with the input voltage. The total number of comparators with output high follows the cumulative distribution function (CDF) of the comparator offset.

2.2. Number of comparators required

In a standard flash ADC, the number of comparators required to obtain n-bit accuracy is 2^n-1. In a stochastic ADC, a large number of minimum sized redundant comparators is used to create a Gaussian CDF transfer function. On the other hand, according to the large number law, the number of comparators in the stochastic flash ADC has to be large enough so that the actual ADC transfer function resembles the ideal one to the desired accuracy. In [8], a study on quantization noise was conducted. The analysis of the quantization noise is repeated, and the input voltage scaling effect is considered in the next sub-section. First, a total N comparators with offset range of 0 to 1 considered. An input voltage with the full-scale value $V_{FS}=1$ is applied to a group of comparators. Assume v is the input voltage, k is the number of comparators that have offset between 0 and v, and $n-k$ is the number of remaining

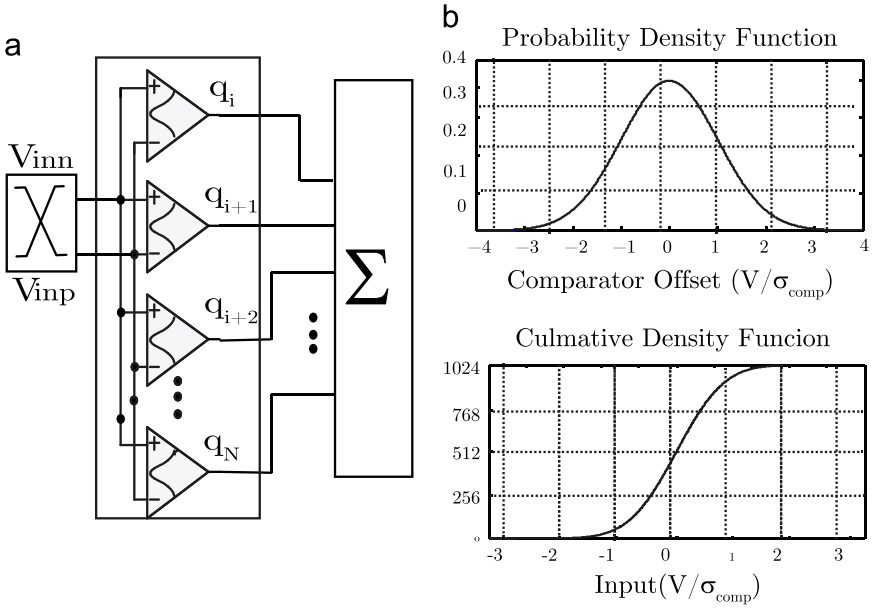

Fig. 2. (a) Block diagram of the stochastic flash ADC (b) ADC transfer function.

comparators with an offset value between v and 1. To calculate the number of comparators, a random uniform threshold with uniform distribution is considered for the comparators. For the total N comparators, the quantization noise power of this ADC as a function of v is equal to:

$$P_{n,Q} = \int_0^1 V_{err}^2 P_{k,v,N}\, dv.$$
$$V_{err} = \frac{k}{N} - v \tag{1}$$

where $P_{k,v,N}$ is the probability mass function and V_{quan} is the error voltage creating the quantization noise. By getting the variance of the quantization error and integrating over the entire v range, the quantization noise power is calculated as follows [8]:

$$P_{n,Q} = \int_0^1 \sum_{i=1}^{N} \left(\frac{k}{N} - v\right)^2 v^k (1-v)^{N-k}\, dv$$
$$= \int_0^1 \frac{v - v^2}{N}\, dv = \frac{1}{6N} \tag{2}$$

The signal to quantization noise ratio (SQNR) is calculated as follows:

$$SQNR = 10\log\left(\frac{P_{sig}}{P_{quan}}\right) = 10\log\left(\frac{\frac{1}{12}}{\frac{1}{6N}}\right) = 10\log(N/2) \tag{3}$$

The number of comparators *(N)* required for n bits is 4^n. In the next sub-section, it is shown that the total number of comparators activated during the ADC operation depends on the input voltage range.

2.3. Input voltage range effect on SQNR

Calculating the SQNR for different input voltage ranges allows us to investigate the effect of input voltage range scaling on the ADC. With a large number of minimum spaced comparators, the input range is limited to $\pm\sigma_{comp}$, which determines the input full-scale voltage. As the input voltage range is scaled from the maximum range, there are fewer comparators that become active during the ADC operation, (See Fig. 3(a)). For example, with the number of comparators equal to N, when applying a sinusoid voltage with the amplitude equal to σ_{comp}, all of the comparators are activated during the ADC operation. However, with an input signal as large as $\sigma_{comp}/2$ applying to the group of comparators, only half of the comparators are involved during the ADC operation, and the rest are always tuned off. Assume N' is defined as the new comparators sets that are activated with the input voltage amplitude of V_{FS}. Also consider a sinusoid input voltage with the amplitude of V_{FS} applied to the ADC. Considering v as the normalized value between 0 and 1 and k as the number of comparators with the offset within the range 0 to v, the quantization noise power is calculated as follows:

$$N' = NV_{FS}$$

$$P_{n,Q(V_{FS})} = V_{FS}^2 \int_0^1 \sum_{i=0}^{N'} \left(\frac{k}{N'} - v\right)^2 v^k (1-v)^{N'-k}\, dv$$

$$= \frac{V_{FS}^2}{6NV_{FS}} = \frac{1}{6NV_{FS}} \tag{4}$$

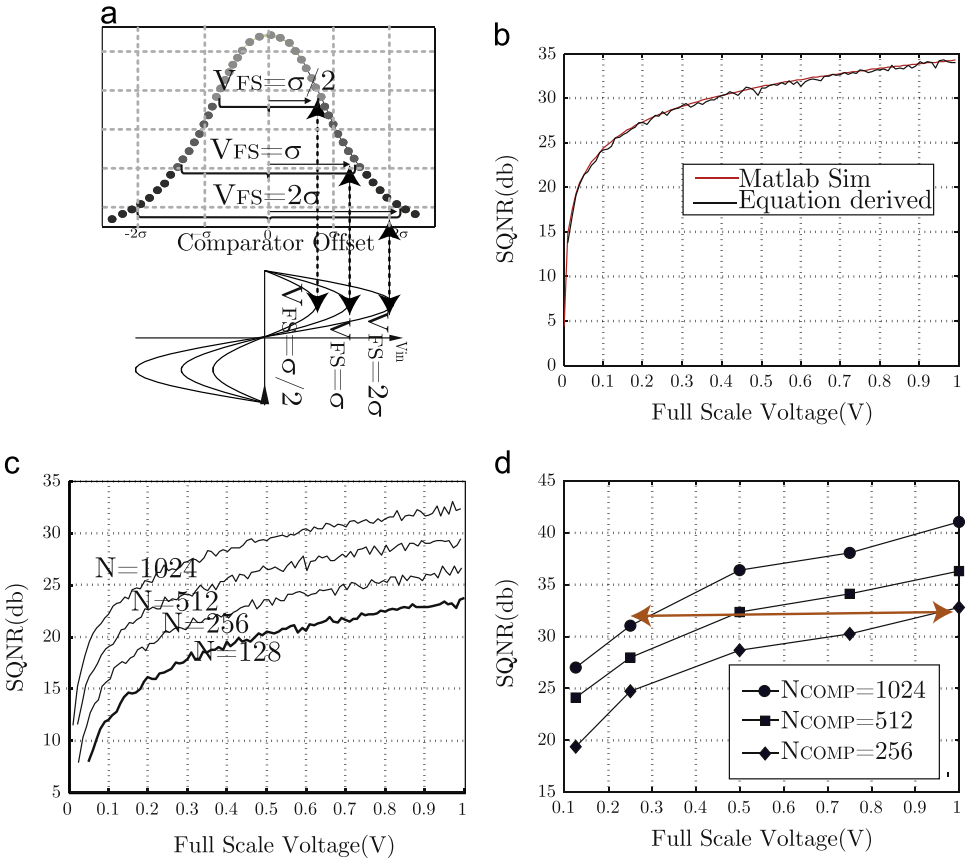

Fig. 3. (a) Comparators involved in ADC operation scaling with input voltage range (b) Calculated SQNR based on (5) and Matlab behavioral simulation as function of the input voltage range (c) calculated SQNR versus input voltage for multiple number of comparators(with Uniform threshold voltage distribution) (d). Simulated SQNR as a function of input range (with Gaussian threshold voltage distribution).

Eq. (4) reveals that the quantization noise power scales down with the V_{FS} almost linearly.

$$SQNR = 10\ \log\left(\frac{P_{sig}}{P_{n,Q}}\right) = 10\log\left(\frac{\frac{1}{12}}{\frac{1}{6NV_{FS}}}\right)$$
$$= 10\log\left(\frac{NV_{FS}}{2}\right) \quad (5)$$

With the signal power being scaled quadratically, the SQNR is scaled almost linearly unlike the non-stochastic ADCs, where the SQNR scales quadratically with the supply voltage. Fig. 3(b) shows the SQNR obtained from (5) which is in a good agreement with the Matlab behavioral simulation.

2.4. Reconfigurable scalable ADC

A constant SNR for different input range is desired in many applications. Fig. 3(c) and (d) depicts the SNQR as a function of the input voltage for different number of comparators. As the number of comparators (N_{comp}) increases, a higher SQNR is obtained. Hence, instead of over-designing the ADC by having a large number of comparators, a smaller number of comparators can be employed for higher input voltage ranges, and as the input voltage weakens, more comparators are involved in the ADC operation to keep the SNR constant. Fig. 4 shows a typical ultrasound receiver which includes a pre-amplifier, a variable gain amplifier (vga), and an ADC. Over the receiving interval, the input signal from the transducer begins to attenuate. A variable gain amplifier is leveraged to increase the gain dynamically to map this signal to the ADC input dynamic range. The proposed reconfigurable ultrasound receiving circuit is shown in Fig. 4. In the proposed system, the variable gain function is performed throughout the ADC itself. This is done by activating different banks of comparators during the ADC operation. With the input voltage attenuated, more comparators banks are activated. The need for the VGA projecting the signal to the ADC input range is eliminated. Hence, an all digital programmable scalable system is obtained by using only the digital standard cell.

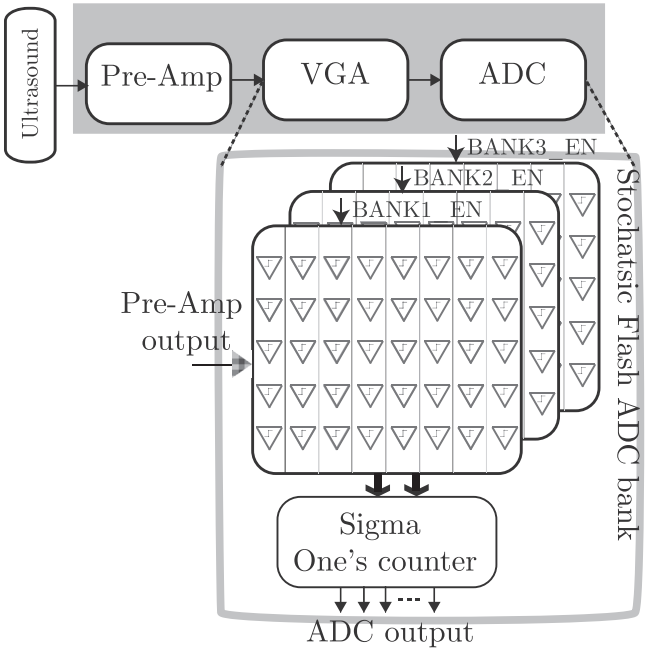

Fig. 4. System block diagram of the reconfigurable variable gain ADC embedded in an ultrasound system.

3. 2D versus 3D fully synthesized stochastic flash adc design flow

3.1. 2D gate level implementation

There are two functional blocks in the stochastic ADC: a group of redundant comparators, and an n-bit ones-counter to count the number of comparators evaluating high during the ADC operation. The whole design was implemented in Verilog code, digitally synthesized, and automatically placed and routed for the final layout. Comparator banks are implemented using the standard library cells in the RTL Verilog code. A comparator is created by cross-coupling two NAND3 gates together as shown in Fig. 5. A sufficiently high common-mode voltage must be applied to ensure the PMOS transistors in cutoff region and make the NMOS fast to meet the target speed. To perform the digital summation of the comparator output voltages, a pipelined Wallace tree adder was implemented. Each comparator output is fed into a full-adder across the nearest neighbors. Adder stages are separated by the flip-flops to pipeline the process and minimize the time required for each adding stage.

3.2. 2D Versus 3D design flow

The 2D implementation of the stochastic ADC design is merely automated through the synthesis and place-and-route. The 3D implementation of the ADC is based on commercial digital design tools which are enhanced with some in-house tools to handle TSVs insertion. The 3D stochastic ADC design and analysis flow from RTL to GDS are summarized in Fig. 6. To implement the target design on the two dies, first the ADC netlist is partitioned manually into die0 and die1 netlist files. Then the Verilog netlist files for each die, along with the TSV technology information file, are fed into an in-house 3D-placer [15,16], where the TSVs assignment and placement are conducted. The 3D-placer optimizes the placement for two dies to minimize inter-die connections for all face-to-back bonding. The Cadence Encounter is used to obtain the final placement and routing of the design. The GDS for the two dies are then fed to the Mentor Calibre for the parasitic extraction separately. Finally, the netlist from each die along with the TSV technology parasitic files are stitched to a unified Spectre netlist, and a Monte-Carlo analysis of the 3D ADC is performed.

3.3. 2D versus 3D floor-planning

The 3D stochastic ADC core netlist is partitioned in two dies, mainly by separating the most front-end and the back-end circuit in the ADC. The front-end circuit is the standard-cell-based comparator bank, and the back-end is the ones-counter. This 3D partitioning is efficient in terms of area balance between dies and the connectivity between them. Fig. 8 depicts the block routing for 2D and 3D designs. For the 2D implementation, a large number of over-the-block wires is required, which increases the total wire-length and hence the interconnect parasitic. In Fig. 8(b), however, the vertical interconnects across dies in 3D technologies are enabled with TSVs. Due to the vertical TSVs, many local wires in the 3D design are connected to nearby TSVs, and this reduces the total wire-length. This also helps to separate the substrate of the digital blocks from the analog sensitive blocks, reducing the substrate coupling noise. Each single TSV is assigned to one nearby comparator. As a result, the number of TSVs scales with the number of comparators.

Fig. 7(a) shows the placement result obtained from the 3D-placer tool. Fig. 7(b) shows a vertical stacking diagram for the face-back die bonding. The TSV cells are recognized by the metal landing pads in TSV formation process. Via-first TSVs, are attached

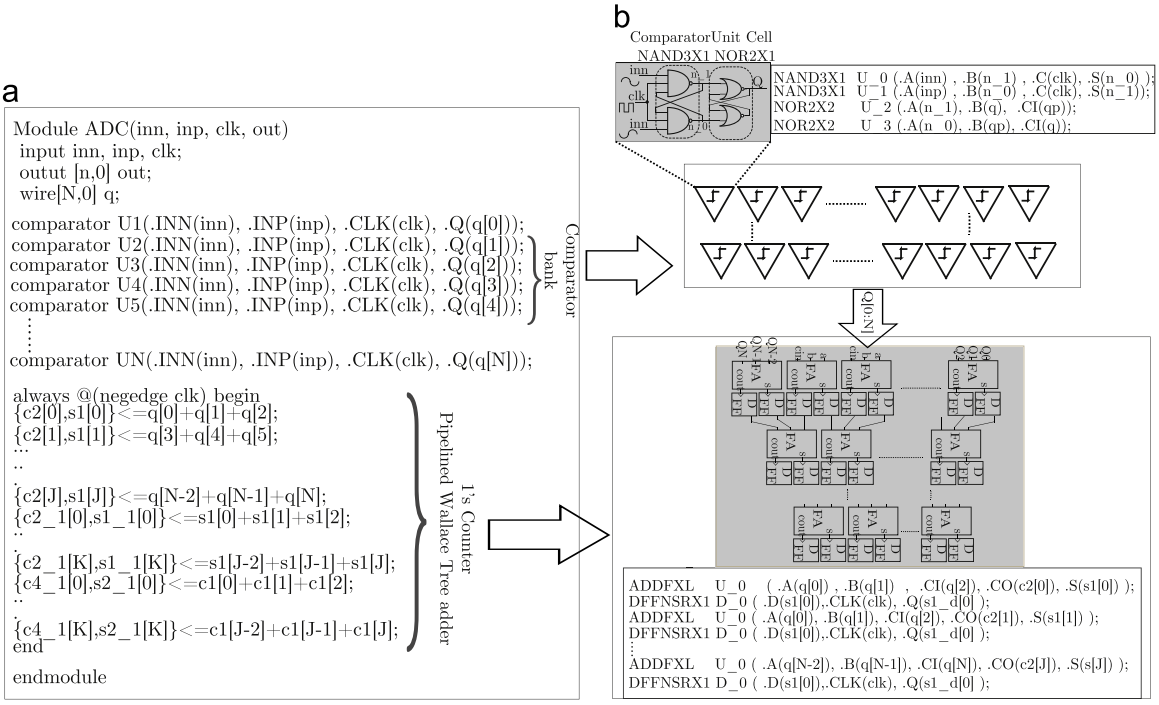

Fig. 5. (a) Verilog module ADC (b) Gate-level implementation.

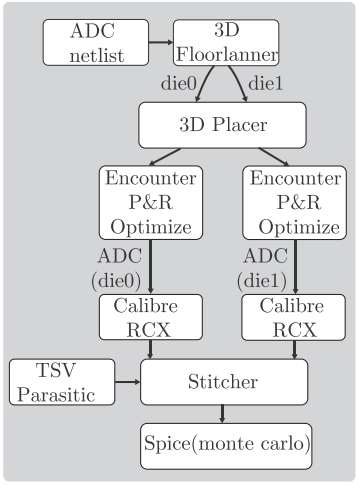

Fig. 6. 3D ADC circuit design and analysis flow.

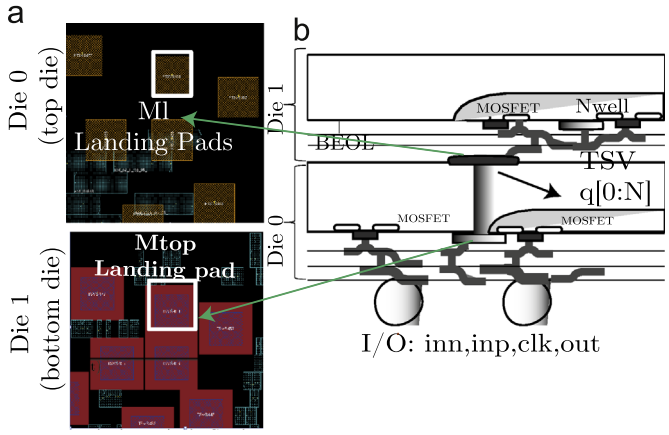

Fig. 7. (a) Die0 and die1 layout obtained from the 3D-placer (red squares denote the M1 TSV landing pad in the bottom and the yellow squares denote M6 TSV landing pad in the top die)(b) 3D stacked vertical diagram.

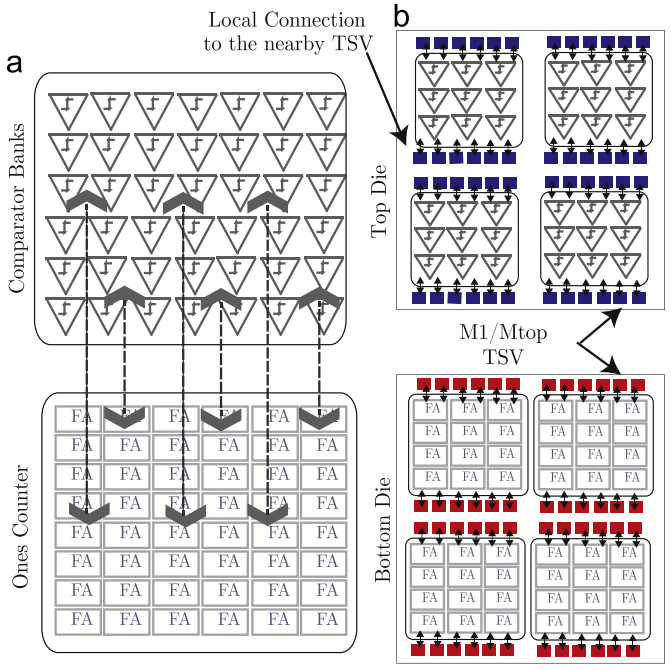

Fig. 8. (a) Inter-block routing block diagram with many long wire between blocks in 2D design (b) Inter-die connections to the nearest TSV in 3D design.

to landing pads in the bottom-most and the topmost metal layers. The TSVs in die0 are attached to M1 and those in die1 are connected to the Mtop metal layer. The I/O c4 bumps are connected to the bottom most dies, where all of the ADC I/O connections, including the analog inputs, (*inn*, *inp*) are made.

3.4. 3D IC ultrasound ADC design flow

A 3D vertical stacking of a 2D-ultrasound transducers array with 2D front-end electronics was first demonstrated in [6,17]. Through-wafer-vias provided the electrical connection between

the 2D CMUT arrays with electronic circuits. In this design, the CMUTs array and the 3D IC front-end circuitry are considered to be manufactured individually and stacked with the help of an intermediate interposer layer and using flip-chip bonding technology.

Two groups of TSVs needs to be formed individually: (1) The through-wafer interconnects for the CMUT array die connecting the transducer elements on the top side with flip-chip bond pads on the back side to the 3D-IC front-end circuity. Due to the higher TSV dimension, usually no wafer thinning is required. The through wafer vias are usually filled with conductive polymers. (2) The though-silicon vias for the 3D IC electronics, where the TSVs diameter are usually very small and thus the aspect ratios are very high. Hence, wafers are usually thinned down to 50 μm. In order to have a higher conductivity, the 3D IC TSVs mostly use copper to fill the tiny vias for 3D silicon integration.

Fig. 9 demonstrates the placement result from the 3D placer. The 3D ADC is to be integrated with a flip chip bonded ultrasound CMUT pads. The ultrasound input is either directly connected to the facing up electronics dies (Fig 9(a)), or a TSV is used for the connection from the transducer output to the facing down electronics (Fig. 9(b)).

The total TSVs in face-up are divided in two groups: the I/O TSVs, which connect the ADC output signals to the C4 bumps and intra-die TSVs which make the connection between two stacked dies. The intra-die TSVs in the top die and bottom die are connected to M1 and Mtop, respectively, and the I/O TSVs are recognized with M1 landing pad in Fig 9(a). In Fig 9(b) the TSVs in face-down are divided in two groups: the Analog TSV, the intra-die TSVs. The intra-die TSVs in the top die and bottom die are assigned to Mtop and M1, and the analog TSV landing pad is attached to be M1.

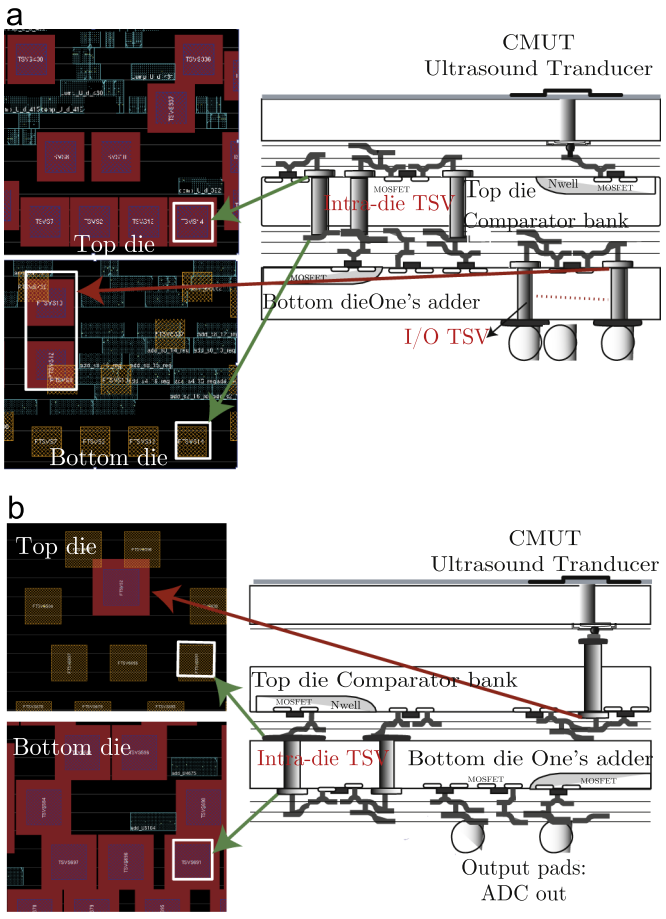

Fig. 9. 3D placement result for the 3D ADC for a (a) face-up (b) face-down integration with the ultrasound transducer array.

4. 3D-ultrasonic-IC coupling noise analysis

TSV is a highly conductive metal that is surrounded by an SiO_2 insulation layer to isolate the dc leakage of TSVs and the highly conductive silicon substrate. This results in a high capacitance between the TSVs and the silicon substrate, which is referred to as C_{TSV}. Therefore, high-frequency noise can be easily coupled from TSV to TSV or TSV to substrate or vice-versa. Coupling noise has major impacts on the circuit performance. In digital circuits, it increases the path delay and it can reduce performance. In mixed signal circuit, it has bigger impact on the sensitive analog signal. In this section, different TSV coupling noise sources are studied first. Then TSV coupling paths are studied for the 3D ADC integrated with the ultrasound array in two different stacking configurations.

4.1. TSV coupling paths

The dc analytical expression for resistance of a TSV (R_{TSV}) is described by using the traditional function of conductivity:

$$R_{TSV} = \frac{l_{TSV}}{\sigma \pi r_{TSV}^2} \tag{6}$$

where l_{TSV}, r_{TSV} are the TSV height and radius, respectively. TSV is isolated from the silicon layer with a dielectric liner, forming metal oxide semiconductor (MOS) structure. Sharing the E-field with only one neighboring TSV, the TSV oxide capacitance C_{ox} is described as follows (Fig. 10(a)) [18]:

$$C_{ox} = \frac{\pi \epsilon_0 \epsilon_{r,sio2} l_{TSV}}{ln\frac{r_{TSV}+t_{ox}}{r_{TSV}}} \tag{7}$$

where t_{ox} is the thickness of the insulator. As the TSV gate bias increases, the depletion region capacitance start to increase, and it acts in series with oxide capacitance. Hence, a TSV capacitor C_{TSV} is modeled with a series connection of the oxide capacitor and a depletion region capacitor [19]:

$$C_{dep} = \frac{\pi \epsilon_0 \epsilon_{r,si} l_{TSV}}{ln\frac{r_{TSV}+w_{dep}+t_{ox}}{r_{TSV}+t_{ox}}} \tag{8}$$

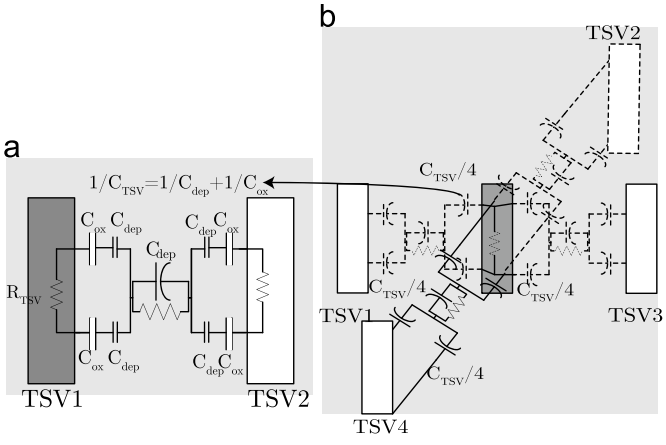

Fig. 10. Figure showing TSV parasitic capacitor with (a) one neighboring TSV (b) four neighboring TSVs. Number 4 in TSV capacitor denominator is due to the TSV Electrical field being shared with four different TSV.

$$C_{TSV} = \frac{C_{dep} C_{ox}}{C_{dep} + C_{ox}} \tag{9}$$

where w_{dep} is the depletion width. In should be noted that the effect of TSV coupling is overestimated if the depletion region is ignored. So taking the C_{dep} into TSV modeling alleviates the TSV coupling effect.

No other objects other than the two TSVs are considered so far to block the E-field around each TSV. However, in this design, four uniform discharge paths around one TSV are considered (See Fig. 10(b)) [20]. As a result the E-field of each TSV is shared with four neighboring TSV, hence, each TSV capacitor share is split by 4 (i.e. $C_{TSV}/4$).

Fig. 11(a) illustrates the two major TSV coupling paths: noise coupling between two TSVs and noise coupling between a TSV and an active circuit(only the 2D shown). A lightly doped bulk type substrate is assumed. By dividing the substrate into several cubes, as proposed in [20], each silicon substrate cube cell is modeled by six (R_{sub}) and (C_{sub}) in parallel in Fig. 11(b)).

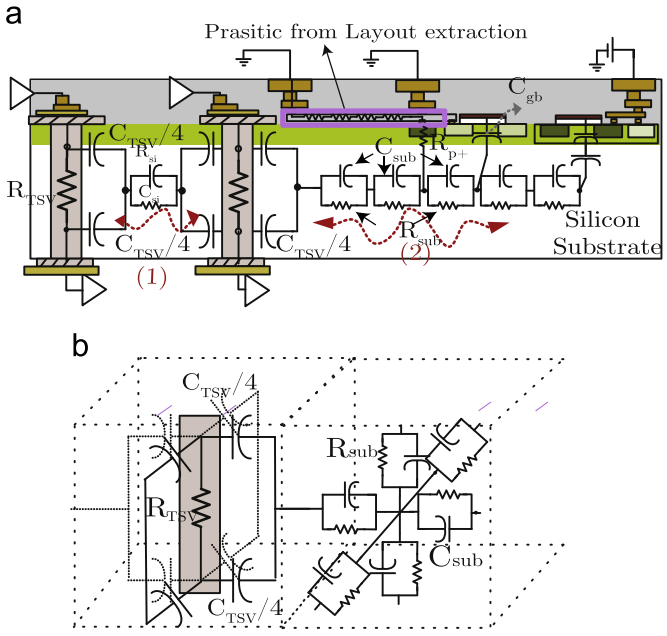

Fig. 11. (a) Figure showing two major paths of TSV noise coupling in 3D IC (only 2D view showed) (b) 3D view of the equivalent circuit model of TSV/substrate unit cell.

$$C_{sub} = \epsilon_{si} \frac{h_{sub} \times l_{sub}}{w_{sub}} \tag{10}$$

$$R_{sub} = \frac{1}{\sigma_{si}} \frac{w_{sub}}{h_{sub} \times l_{sub}} \tag{11}$$

where w_{sub}, l_{sub} and h_{sub}, represent the width, length, and height of the substrate unit.

4.2. Face-up versus face-down dies coupling analysis

The TSV coupling noise behavior of the two 3D stacking integration based on in Fig. 12(a) and (b) are studied in [14]. Calibre RCX is used to extract the wire parasitic as well as the power/ground on-chip network. The thinned substrate parasitic network is modeled by a horizontally constant mesh network. Also, the P+ well contacts are considered in the distributed model. For the TSV active coupling analysis, the TSV, the substrate unit cells and the well contact parasitics are combined together along with the layout parasitic extracted for the power/ground on-chip network to produce a highly distributed mesh based parasitic network.

Fig. 12(a) depicts a 3D IC face-up dies, with the ultrasound signal directly connected to the electronics via the metal stack. The TSV-to-active coupling from the digital TSV is via the substrate RC path to the input analog signal. The substrate noise is directly coupled to the gate substrate contact. The coupling to the CMOS gate metal, is attenuated via the C_{gb}capacitance which is much smaller than the C_{TSV}. As a result, less coupling noise is expected for the face-up configuration. The small circuit equivalent of the transducer is used as the signal source.

In 3D IC face-down dies in Fig. 12(b), the analog ultrasound signal is first delivered to the top tier via a TSV. Meanwhile, a semi-digital output signal from the top tier is fed to the bottom tier via the TSVs. The active-to-TSV coupling from the digital noise source via the substrate RC path to the input analog TSV is depicted in Fig. 12(b).

5. Full chip results and discussion

In this section, different TSV design flows for 3D stochastic ADC implementation are analyzed and compared. Based on post-layout simulation results, several design metrics of the 3D design are compared with the traditional 2D design. The 2D and 3D ADC designs use digital standard cells from GlobalFoundries 130 nm and Tezzaron TSV technology. No custom cells were used in this

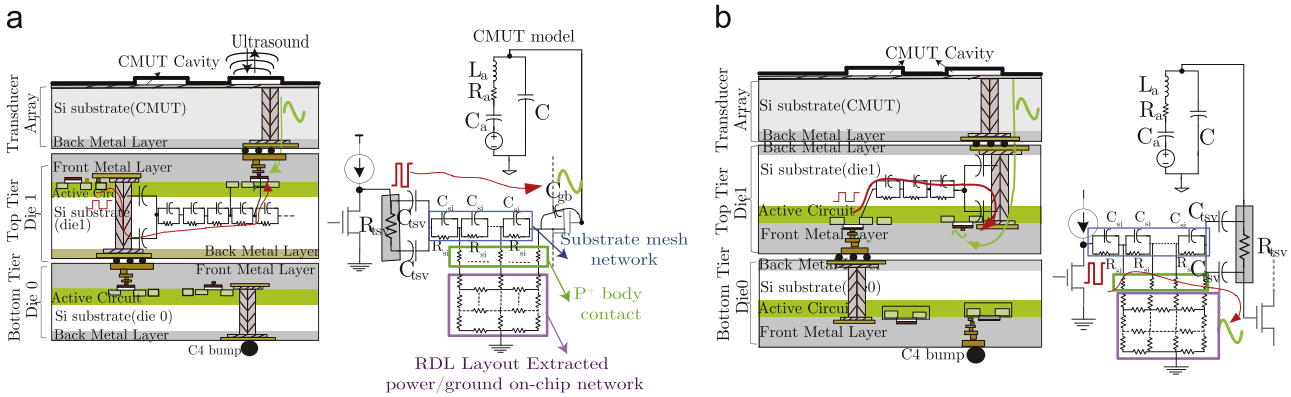

Fig. 12. (a)Noise coupling path between the high frequency digital TSVs to analog input signal in face-up (b)Noise coupling path between the high-frequency digital signal to the analog TSV in face-down dies stacking.

design. The provided simulations uses 1.5 V supply voltage and 100 MHz sampling frequency.

5.1. 2D ADC design versus 3D regular/irregular TSV placement

Fig. 13(a) shows a layout shot for the a 2D-ADC implementation. Fig. 13(b) and (c) depicts the dies shots with regular and irregular TSV placement, respectively. The core netlist is partitioned into two dies of the comparator array and a pipelined Wallace-tree ones-counter. An in-house 3D-placer for TSV/cell placement is used. In the regular TSV placement, the TSVs are preplaced in a regular array style with user defined pitch, and then the cell placement for each die is completed. In the irregular TSV placement scheme, the TSVs are considered as a normal cell. Therefore, the cells and TSVs placements are performed simultaneously to reduce the wiring congestion. Significant inter-block connections in Fig. 13(a) are replaced with the local wires to the nearest TSV. Hence, the 3D IC has a significant impact on reducing the wire-length, which translates to lower power consumption. However, the impact of the TSV capacitance on the design needs to be studied. The parasitic TSV parasitic capacitance is a major source of interconnect power dissipation.

In Fig. 14, the effect of TSV capacitance on the 3D power consumption is studied for two 1024 and 2048 comparators versions. The 3D power consumption increases with the parasitic TSV capacitance. Above a specific TSV parasitic value, there is no advantage in 3D power compared with the 2D design. The 2048 comparators version, exhibits more power improvement for the 3D implementation over the 2D implementation, which is mainly due to a higher power dissipation in the interconnect dominant in the larger design sizes. As a result, more power consumption is saved by reducing the total wire-length in the larger 3D designs.

The comparison between the 2D and 3D based on the post-layout simulation result are as shown in Table 1. A target clock frequency of 100 MHz was considered. First, a footprint area reduction of 40% was achieved. Second, 60% reduction in wire-length was achieved in the 3D IC design compared to the 2D implementation. As a result, the 3D design reduces power consumption over the 2D counterpart by 20%. The TSV diameter, resistance, capacitance and landing pad size are 10 mΩ, 20 fF, and 5 um $\times$ 5 um, respectively. Comparison between the 3D regular versus irregular TSV design is shown in Table 1. The regular TSV placement shows the same performance as the irregular, however, a better manufacturability is guaranteed by ensuring a more regular design.

5.2. Block-level design versus gate-level design

In this design, a gate-level based as well as a block-level based designs for the comparator inside the 3D ADC were implemented and compared. Fig. 15, demonstrates the die shots for the a 3D implementation of a block-level comparator design versus the gate-level design. In the block-level design, the 3D-placer treats the comparator as a macro-block. In the 3D-placer, the TSVs are also treated as blocks so the TSVs are placed outside the comparator macro-blocks. This helps to avoid any overlap between the TSV arrays and the comparator bank array. Comparison between the 3D block-level design versus the gate-level designs is as shown in Table 2. Greater area usage and longer wire-length are observed for the block-level design over the gate-level design. This is mainly because of the intra-block-level routing that affects the routing congestion, (see Fig. 15). However, a higher maximum operating frequency in the block-level design is achieved. The maximum operating frequency is mainly dependent on the most front-end input stages (the NAND gates) driving strength. In the block-level

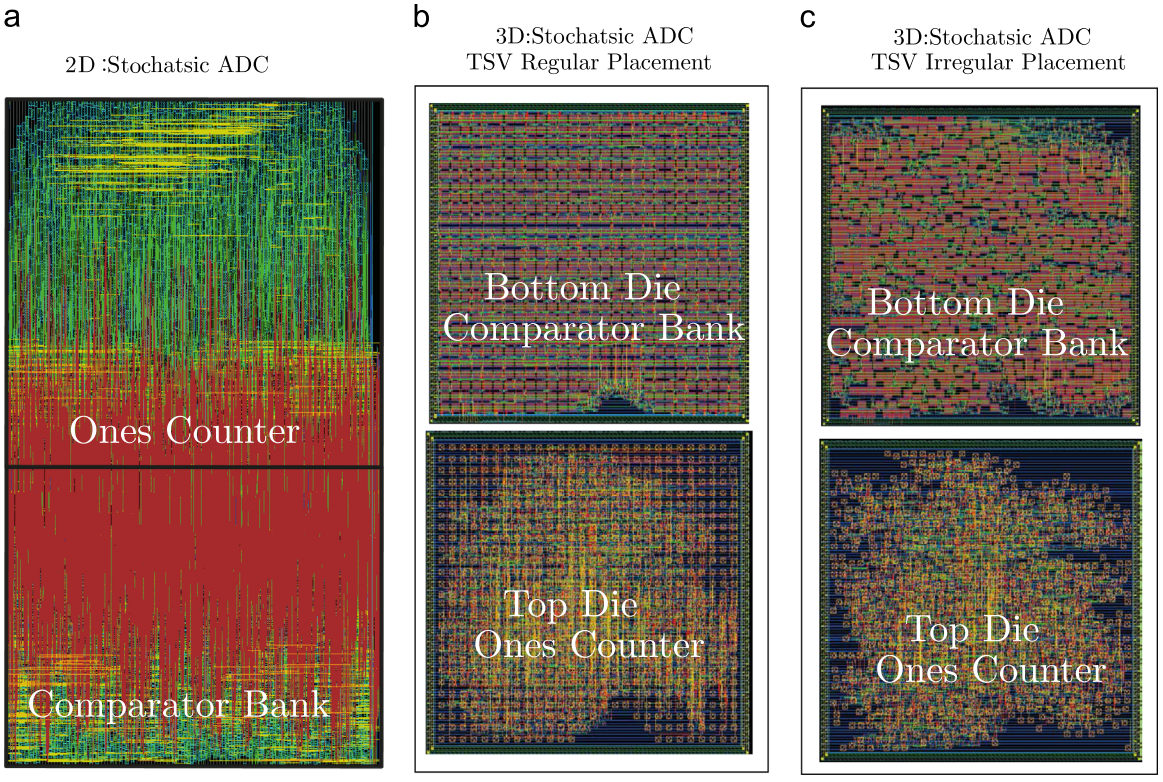

Fig. 13. An SoC Encounter die shot for (a) 2D implementation (b) 3D regular TSV placement implementation (c) 3D irregular TSV placement implementation of a stochastic ADC.

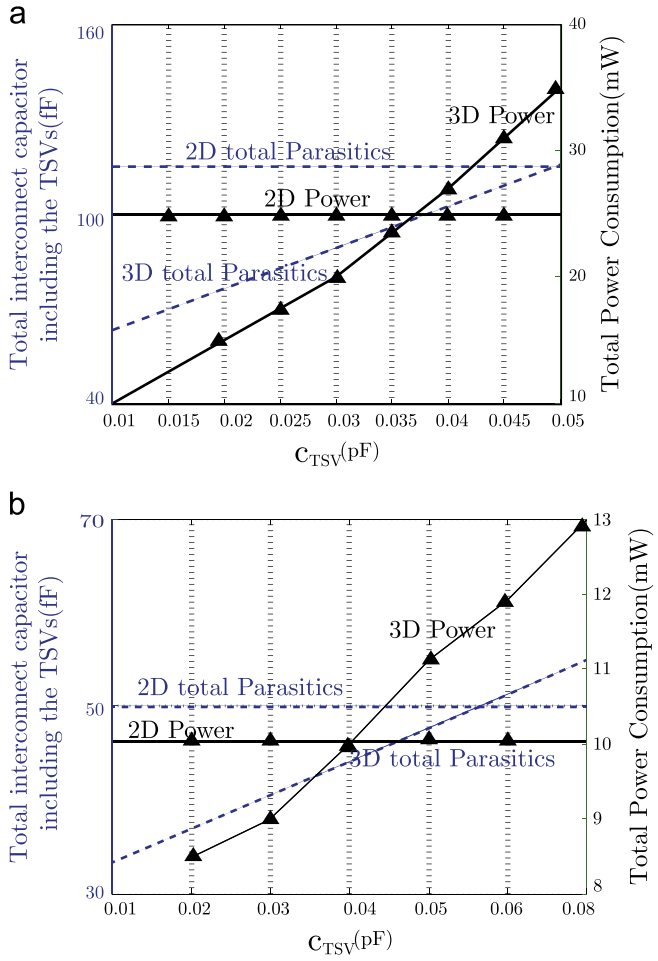

Fig. 14. Power consumption from spice simulation as a function of TSV parasitics for 2D and 3D design implementation for (a) 2048 comparator version (b) 1024 comparator version design.

Table 1
2D vs 3D stochastic ADC power comparison for f_{CLK}=100 MHz, N_{comp} = 1024, and N_{comp} = 2048.

Number of comparators(N)	2D 1024	2048	3D irreg. TSV 1024	2048	3D reg. TSV 1024
Footprint (mm^2)	0.280	0.605	0.176	0.325	0.1765
Total W*L (mm^2)	0.057	0.24	0.097	0.032	0.029
Total wire+TSV parasitic(pF)	50.1	125.24	33	45	32.5
Total power (mW)	10.6	23.7	8.4	14	8.3
Cell power (mW)	6.1	12.2	5.7	9.2	5.7
Interconnect+TSV power (mW)	4.2	11.5	2.7	4.8	2.6

design, the comparator input stage has to drive the minimized parasitic capacitance due to the symmetric fixed configuration. However, in gate-level design, the input stages have to drive large interconnect parasitics, the value of which varies among the comparators in the design. The extracted capacitance seen at the outputs of the NAND gates was shown to have a log-normal distribution [9]. A maximum sampling frequency of 1 GHz is obtained in the block-level design case, which is appealing the applications with a high operational speed.

5.3. 3D IC face-up versus face-down

Fig. 16(a) and (b) depicts die shot for the 3D ADC dies facing-up and facing-down, respectively. In the face-up stacking type, the transducers' flip chip bonded pads are directly bonded to the integrated circuit. In the face-down integration type, however, the connections from the sensor output signal to the front end electronics is made via the TSVs. A less-sufficient footprint is observed in the facing up dies, which is mainly due to the area imbalance between different dies and the different landing pads in different stacking types as discussed in Section(3). The design metrics for the face-up and face-down dies stacking for a 100 MHz clock frequency are compared in Table 3. The coupling noise power to the analog TSV as modeled in Fig. 12 is suppressed by 9.4 dB for face-up integration, and also a 23% reduction in footprint is achieved.

5.4. Performance comparison with stochastic ADCs

Table 4 compares the post-layout simulation results of the proposed 3D stochastic ADC with the measurement results of some recent stochastic flash ADCs. All the designs reported in Table 4, exploit a digital programmable flow for the entire ADC. Regular digital design tools in [9,21], as well as some in-house tools for the TSV insertion in this design were used. In the ADC reported in this work, the maximum signal to noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) of 28.5 dB and 29.6 dB are reported, respectively. Hence, (SNDR) reported is mostly limited by the linearity. Both [9] and [21] employ some linearity enhancement techniques to increase the linearity of the ADC that comes at the expense of increasing the power consumption. Techniques for linearity enhancement include applying inverse CDF function as either, look-up table based inverse CDF function [22], or using a linear piecewise digital mathematical function to implement the inverse CDF [9]. Also, separating the group comparators CDF by some standard deviations value, helps to improve linearity, since the sum of the CDFs demonstrates a linear behavior between the two reference voltages [23]. In [21] both the inverse function and different reference voltages to comparator group are emplyed to enhance the linearity. In [21] a reconfigurable structure is presented by dividing the design into 8 channels, where the SNDR and the input range is reconfigurable. It should be noted that stochastic flash ADCs, with only minimum sized digital gates, favors with the technology scaling, as the power consumption scales with the technology node. Also, an input range enhancement is obtained as the technology scales down and the mismatch between minimum sized transistors increases. In addition low-power digital design techniques, such as body-biasing, and sub-threshold circuit design technique can be applied to the ADC to optimize power consumption.

6. Conclusion

A fully synthesized 3D stacked stochastic ADC for the ultrasound interface application is implemented in 130 nm GlobalFoundries device technology and Tezzaron through-silicon-vias (TSV). Due to the vertical stacking dies, the 3D technology reduces the ADC footprint area and also results in a power efficiency for 3D ADC compared to the 2D design. In analog/mixed signal ICs, however, the TSV coupling effect is a major challenge due to it's high parasitic capacitive. In this paper two different 3D IC face-up and face-down dies stacking for the ultrasound array and the 3D ADC are considered and compared in terms of the TSV coupling noise effect on the analog signal. A medium resolution ADC was implemented in 3D stacked, where different TSV insertion methods. A 20% improvement in power consumption is observed in the 3D implementation, and a 40%

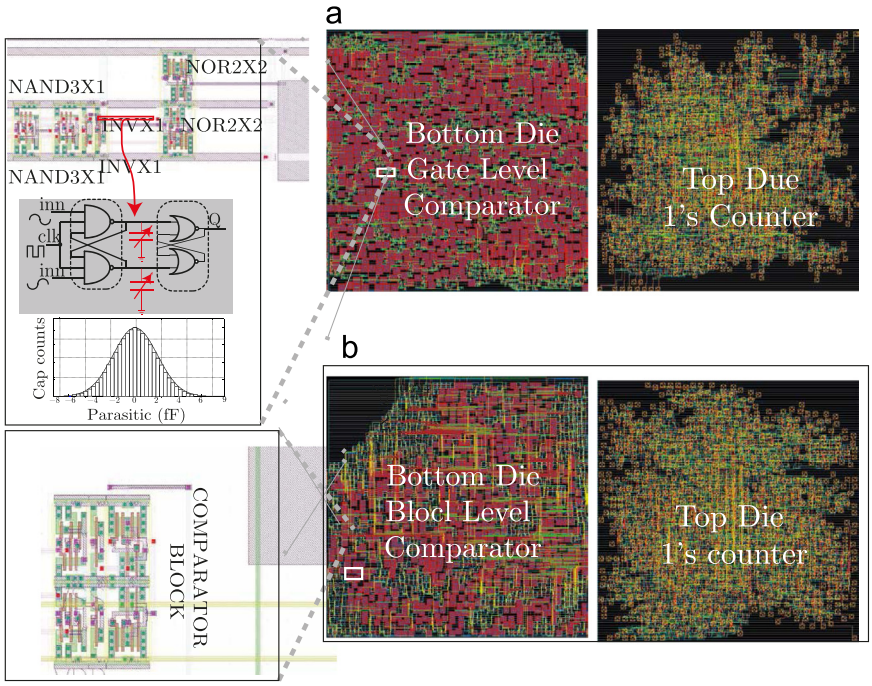

Fig. 15. Dies shots of the 3D stochastic ADC implementation with (a) block-level (b) gate-level comparator array design.

Table 2
Block-level versus Gate-level 3D stochastic ADC design performance comparison for $N_{comp} = 1024$.

	Gate-level	Block-level
Footprint (mm^2)	0.176	0.23
Total wire-length (mm^2)	0.032	0.041
Total Power(mW)	8.4	8.78
Max sampling freq (GHz)	0.51	1.10

Table 3
Performance comparison of 3D IC with dies facing up/down for f_{CLK}=100 MHz and $N_{comp} = 1024$.

	3D IC face-up	3D IC face-down
TSV coupling noise (nw)	0.15	1.3
Footprint (mm^2)	0.13	0.17
Total TSV counts	1034	1025

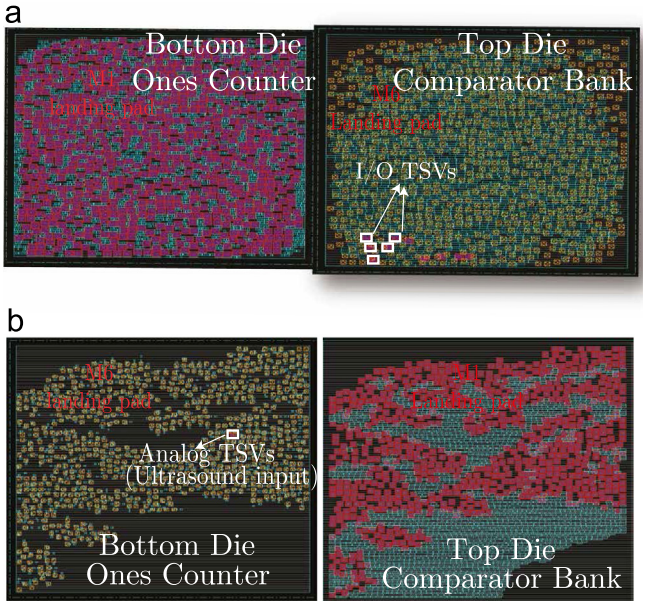

Fig. 16. 3D ADC implementation with the (a) dies facing up (b) dies facing down the transducer array.

Table 4
Performance comparison with other stochastic flash ADCs .

	This work: 3D			This work: 2D	[9]	[21]
Architecture-3D	Gate-level irreg. TSV	Gate-level reg. TSV	Block-level	–	–	–
Footprint (mm^2)	0.176	0.176	0.23	0.28	0.18	0.51
Technology (nm)	130	130	130	130	90	140
Sampling Frequency (MHz)	100	100	100	100	210	140
Number of comparators	1024	1024	1024	1024	2047	2040
Input Frequency (MHz)	20	20	20	20	1	1
Power (mW)	8.4	8.3	8.78	10.6	34.8	17.3
SFDR (dB)	29.6	29.6	29.6	29.6	41.46	37
SNDR (dB)	28.5	28.2	28.5	28.4	35.89	34.5

footprint reduction is achieved, due to the vertical stacking of the 3D technology. The simulations results show that the 3D face-up integration could suppress the TSV coupling noise by 10 dB compared to the face-down integration. Moreover, a 23% reduction in the footprint is achieved in this stacking integration type.

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