Cross-Domain Optimization of Ferroelectric Parameters for Negative Capacitance Transistors—Part I: Constant Supply Voltage

Sai Pentapati, Rakesh Perumal, Sourabh Khandelwal, *Senior Member, IEEE*, Michael Hoffmann, Sung Kyu Lim, *Senior Member, IEEE*, and Asif I. Khan, *Member, IEEE*

***Abstract*—In this two-part article, we propose a framework for selecting ferroelectric oxide material for the design of a negative capacitance field-effect transistor (NCFET). The investigation is based on an exhaustive search of two important ferroelectric material parameters: remnant polarization and coercive field in the context of their negative capacitance properties. The effects of these parameters are first studied at the NCFET device level and systematically extended up to the full-chip level. Based on this search, we arrive at the notion of optimality of ferroelectric parameters for a given "isoperformance full-chip benchmark": The power dissipation in a specific circuit/system is maximally reduced by using optimized NCFETs while meeting the target performance. In Part I, we develop the framework for identifying optimal ferroelectric parameters at a given V_{DD}. This sets the stage for Part II, where we investigate the optimal ferroelectric parameters as V_{DD} is scaled.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS) technology, high-performance, low-power, negative capacitance transistor.**

I. Introduction

THE negative capacitance field-effect transistor (NCFET) with a ferroelectric oxide layer integrated into its gate dielectric stack is an emerging device technology that can significantly reduce power consumption in the complementary metal–oxide–semiconductor (CMOS) electronics by enabling dramatic voltage scaling, thanks to its steep switching characteristics and the enhanced ON-current [1], [2].

Manuscript received September 6, 2019; revised October 24, 2019; accepted November 13, 2019. Date of publication December 16, 2019; date of current version December 30, 2019. This work was supported by the National Science Foundation under Grant 1718671. The review of this article was arranged by Editor B. K. Kaushik. *(Corresponding author: Sai Pentapati.)*

S. Pentapati, S. K. Lim, and A. I. Khan are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: sai.pentapati@gatech.edu; limsk@ece.gatech.edu; asif.khan@ece.gatech.edu).

R. Perumal is with NVIDIA, Santa Clara, CA 95051 USA (e-mail: rakesh18@live.com).

S. Khandelwal is with the Department of Electrical Engineering, University of South Florida, Tampa, FL 33647 USA (e-mail: skhandelwal@usf.edu).

M. Hoffmann is with NaMLab gGmbH, 01187 Dresden, Germany (e-mail: micheal.hoffmann@namlab.com).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2019.2955018

Experimental demonstrations of the fundamental physics of negative capacitance in a wide range of ferroelectric oxides and steep turn-on characteristics in CMOS-compatible ferroelectric-gated NCFETs garnered significant interests into this technology lately [3]–[6]. The design and performance of NCFETs, and, to a lesser extent, NCFET circuits have been investigated through modeling and simulation in [7]–[10]. Krivokapic *et al.* [3], Xuan *et al.* [11], and Kwon Xuan *et al.* [12] experimentally show negative capacitance effects such as steep subthreshold slope, improved power, and ON-current at transistor level and inverter level in ferroelectrics of thickness 1.8–8 nm at the 14-nm CMOS technology node. Most of these works are limited to the transistor and circuit-level results.

In this two-part article, we perform an exhaustive, multiscale investigation of the impact of ferroelectric parameters remnant polarization and the coercive field, on the NCFET performance and power. We start at the transistor-level spice simulations and systematically extend to the gate-level and full-chip implementation. What underpins our study is that ferroelectrics based on widely studied and CMOS compatible fluorite type oxides—Hafnium and its doped/compositional variants—provide a wide range of material parameters allowing for a vast design space for NCFETs [13]–[34]. Based on a comprehensive search through the material-level properties of these ferroelectrics, we arrive at the notion of optimality of ferroelectric parameters for a given "isoperformance full-chip benchmark:" at a given power supply voltage V_{DD}, the power dissipation of a given circuit is maximally reduced by using optimized NCFETs while meeting the target performance. As the full-chip benchmark, we consider low-density parity-check (LDPC) decoder circuit. LDPC decoders are a group of functional modules used to decode the LDPC error correction codes in high-speed communications. The benchmark used here is a decoder for the IEEE 802.3 an standard-based 10-Gbit/s Ethernet networking. In Part I, we develop the framework for optimization by implementing NCFET benchmark designs with a fixed area and power supply voltage (V_{DD} = 0.4 V). This sets the stage for Part II, where we investigate how the ferroelectric parameters should be optimized as V_{DD} is scaled.

0018-9383 © 2019 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on February 21,2020 at 17:25:27 UTC from IEEE Xplore. Restrictions apply.

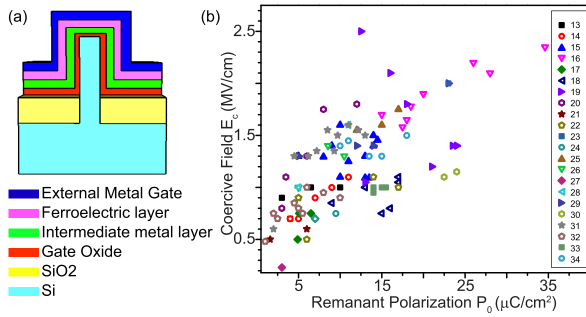

Fig. 1. (a) Schematic of a NCFET. (b) Experimentally reported combinations of spontaneous polarization $P_\circ$ and coercive field E_C in ferroelectric HfO_2 and its doped/compositional variants [13]–[34].

II. Negative Capacitance Field-Effect Transistor

Fig. 1(a) shows the schematic of the NCFET structure, in which a ferroelectric negative capacitance layer is introduced in the gate dielectric stack. The device structure without the ferroelectric layer is referred to as the baseline FET. We use the industry-standard BSIM-CMG [35] to model our baseline FET. The BSIM-CMG model is originally developed as a compact model for multigate FinFET transistors that are used in the advanced technology nodes like the FreePDK 15-nm library [36] used here. The baseline FET is a single-fin transistor with the following dimensions: fin height $H_{\text{fin}} = 42$ nm, fin thickness $T_{\text{fin}} = 7$ nm, fin pitch $P_{\text{fin}} = 48$ nm, equivalent oxide thickness EOT $= 0.8$ nm, and gate length $L_G = 20$ nm. The ferroelectric oxide layer has a thickness of $t_F = 2.5$ nm to be feasible in the 15-nm CMOS fabrication process and is modeled using a second-order Landau–Devonshire relation: $E_F = \alpha Q + \beta Q^3$, where E_F is the electric field across the ferroelectric layer, Q is the polarization/surface charge density, and α and β are anisotropy constants of the ferroelectrics. Hoffmann *et al.* [37] have recently demonstrated that the intrinsic S-shaped polarization-electric field curve fits well to the experimentally measured values of remnant polarization $P_\circ$ and coercive field E_C even in macroscopic capacitors with tens of microns of lateral dimensions much bigger than individual grains/domains. As such, we calculated the values of α and β by fitting the experimentally measured $P_\circ$ and E_C values to the Landau–Devonshire equation i.e., $\alpha = (-3\sqrt{3}/2) \times (E_C/P_\circ)$ and $\beta = (3\sqrt{3}/2) \times (E_C/P_\circ^3)$. Note that the dielectric constant $(=(1/\epsilon_\circ) \times (dP/dE))$ of the ferroelectric is: 1) negative when the ferroelectric is in the negative capacitance state and 2) nonlinear dictated the quiescent point on the S-shaped P-E curve. The simulation methodology of NCFET is described in [8], which includes the short-channel behavior of the baseline. Ferroelectric-domain switching speed is assumed to be faster than device switching speed as shown in recent work [38], [39] , and so, the domain switching speed is not considered. However, further experimental research is needed to truly justify the NCFET speed. It is also worth noting that, the NCFET simulations with the 15-nm transistor model did not show a negative differential output resistance using the BSIM model, similar to that in [4]. This is possible if the natural positive slope of the output conductance is not completely canceled by the ferroelectric gain.

In all these simulations, the OFF-current I_{OFF} (defined as drain current I_D at gate voltage $V_{\text{GS}} = 0.0$ V and drain voltage $V_{\text{DS}} = 0.8$ V) was set at 9.63 nA for the single-fin n-type transitor by shifting the I_D–V_{GS} curves along the V_G axis [2]. HfO_2 and its doped/compositional variants are considered as the ferroelectric material [13]. Ever since the discovery of ferroelectricity in these well-studied material systems, a wide range of key ferroelectric parameters $P_\circ$ and E_C has been reported in the literature. Fig. 1(b) plots experimentally reported ($P_\circ$, E_C) pairs in HfO_2 and its doped/compositional variants by surveying [13]–[34]. Based on these experimental values and the parameters that work the best for the technology node, we use the following range for NCFET parameters: 10 μC/cm$^2 \le P_\circ \le 40$ μC/cm^2 and 1 MV/cm $\le E_C \le 4$ MV/cm. The viscosity parameter and multidomain effects have been explored previously in [40] and [41], respectively. In this article, we do not deal with these effects and assume that the negative effects of viscosity and multidomain are not present. In all our studies, we fix $V_{\text{DS}} = 0.4$ V for NCFETs. In case of the baseline FET, we use either 0.4 V (the voltage under consideration) or 0.8 V (the nominal voltage for the FreePDK 15 nm technology), depending on the experiment.

III. Impact of Materials on NCFET Device

Based on the capacitance matching formalism [2], the criterion for a nonhysteretic operation of an NCFET is that the minimum absolute value of the ferroelectric negative capacitance ($|C_F|$) must be larger than the gate capacitance of the baseline FET (C_{base}) (min $|C_F| \ge$ max C_{base}). The closer the magnitude of the ferroelectric negative capacitance is to the baseline capacitance, the steeper the switching characteristics, and the higher the enhancement in ON-current of the NCFET. The value of min $|C_F|$ is dictated by $P_\circ$, E_C, and t_F: min $|C_F| \approx (2/(3\sqrt{3})) \times (P_\circ/E_C t_F)$ [42]. Fig. 2(a) maps out the region of $(P_\circ, E_C)$ phase space in which the criteria for nonhysteretic operation is met. In this article, we only focus on the nonhysteretic operation, which corresponds to the white region in Fig. 2(a).

To understand the evolution of NCFET characteristics in the $(P_\circ, E_C)$ phase space, we first consider two sets of devices indicated in Fig. 2(a): 1) A, B, and C in which $P_\circ$ varies at a constant E_C and 2) D, B, and E in which E_C varies at a constant $P_\circ$. Fig. 2(b) and (c) plot the drain current I_D versus gate voltage V_{GS} characteristics for NCFET A, B, C and NCFET B, D, E, respectively, along with the baseline FET. For a given t_F, we observe that progressively decreasing $P_\circ$ or increasing E_C leads to progressively steeper turn-on characteristics and higher ON-current due to progressively better capacitance matching. This observation is in agreement with that in [42].

To better visualize the effects of $P_\circ$ and E_C on important device properties, we show the phase maps of the minimum subthreshold swing $S_{\min}$ and ON-current I_{ON} in Fig. 2(d) and (e), respectively. $S_{\min}$ is defined as the change in V_{GS} required to induce one decade change in I_D (from 10^{-7} A to 10^{-6} A) with $V_{\text{DS}} = 0.4$ V. The baseline FET exhibits $S_{\min} = 80$ mV. I_{ON} is defined as the I_D at $V_{\text{GS}} = V_{\text{DS}} = V_{\text{DD}} = 0.4$ V. To generate these phase plots, a total number of 496 NCFETs with different ($P_\circ$, E_C) combinations were simulated.

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on February 21,2020 at 17:25:27 UTC from IEEE Xplore. Restrictions apply.

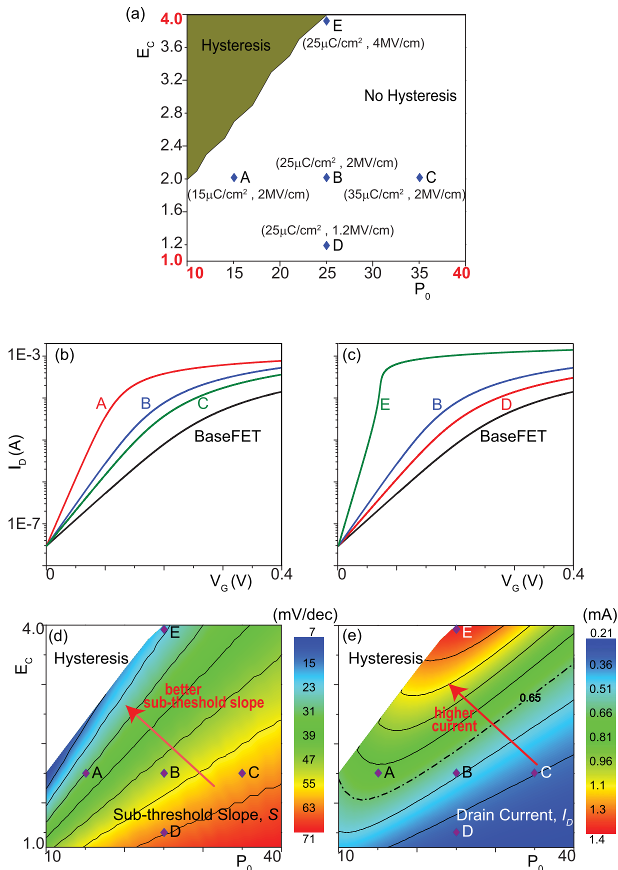

Fig. 2. Analysis of device-level characteristics. We set $V_{DS} = 0.4$ V for both NCFETs and baseline FET. (a) Five ($P_\circ$, E_C) combinations (A, B, C, D, E) studied. (b) I_D–V_{GS} characteristics of NCFET A, B, C, and baseline FET. (c) I_D–V_{GS} characteristics of NCFET B, D, E, and baseline FET. (d) Phase map of the minimum subthreshold slope S_{min}. (e) Phase map of the ON-current I_{ON}.

First, we observe that the lowest S_{min} and the largest I_{ON} are both obtained at the boundary between hysteretic and nonhysteretic operations. Similar observations were also made in [43]. Moreover, we observe that the largest value of I_{ON} corresponds to the upper right end of the boundary line, where E_C and $P_\circ$ are both the largest and on the boundary. On the contrary, the smallest value of S_{min} is obtained at the bottom left end of the boundary line, where E_C and $P_\circ$ are both the smallest. As we move perpendicular to the boundary line toward the right in Fig. 2(d) and (e), the value of min $|C_F|$ being proportional to $P_\circ/E_C$ increases, resulting in progressively increasing difference between min $|C_F|$ and C_{base}. This, in turn, causes both S_{min} and I_{ON} to degrade. From the phase plots, we observe that the maximum ON-current and the minimum subthreshold slope regions lie on the opposite ends of the hysteresis boundary. In devices with very steep subthreshold slope, we observed that the ferroelectric loses its negative capacitive effect quickly and the current starts saturating. This leads to the wide variation in I_{ON} at the hysteresis boundary where the subthreshold slope is minimum.

IV. Impact of Materials on NCFET Inverter

In this section, we study the impact of the ferroelectric parameters on various characteristics of an inverter. We consider inverters comprised of complementary NCFETs A–E and the baseline FET. The inverter model comes from the minimum sized inverter in the FreePDK 15-nm Open Cell Library (OCL). This netlist includes the transistors and the RC-parasitics of the interconnects present in the inverter layout. The transient characteristics are analyzed using an FO-1 inverter where the inverter drives an identical inverter as load.

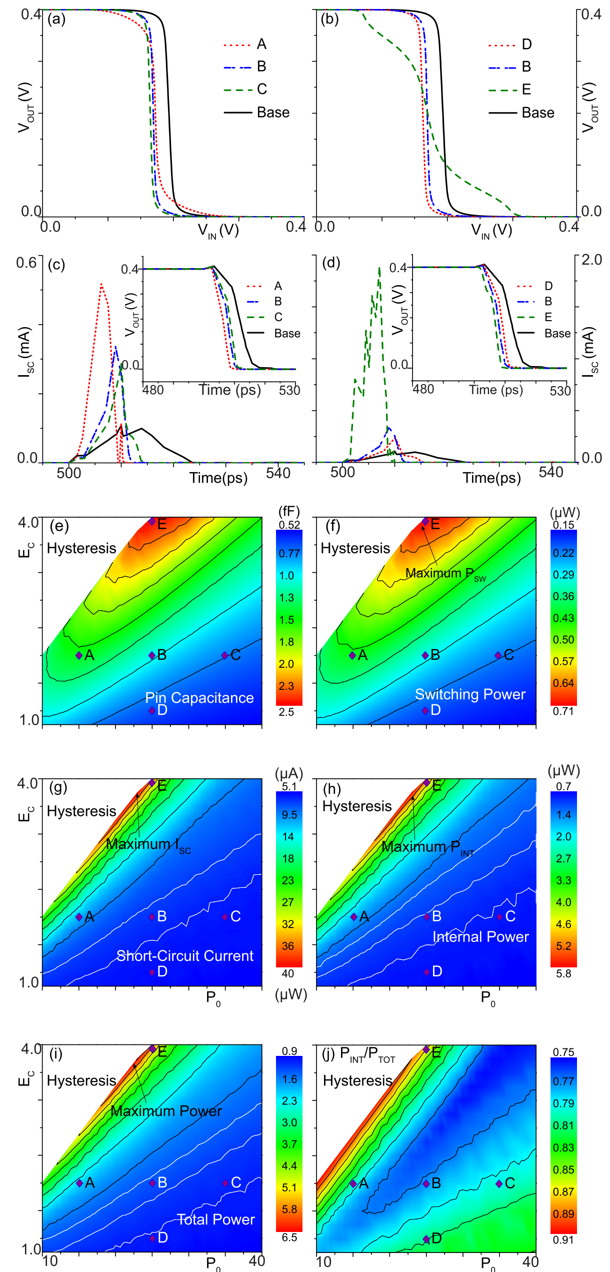

Fig. 3. Analysis of NCFET inverter. (1) Voltage transfer curves of inverters made with (a) NCFETs A, B, and C. (b) NCFETs D, B, and E. (2) Short circuit current transients and output voltage transients of inverters made with (c) NCFETs A, B, and C. (d) NCFETs D, B, and E. (3) Phase maps for: (e) pin capacitance. (f) Switching power. (g) Short circuit current. (h) Internal power. (i) Total power. (j) Ratio of internal to total power.

A. NCFET Inverter Voltage and Current Transients

Fig. 3(a) and (b) shows the voltage transfer characteristics (VTCs), and Fig. 3(c) and (d) shows the corresponding short circuit current I_{SC} transients for these inverters. The insets in Fig. 3(c) and (d) show the corresponding output voltage

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on February 21,2020 at 17:25:27 UTC from IEEE Xplore. Restrictions apply.

V_{OUT} waveforms. Due to the steep switching characteristics, NCFETs A and E exhibit the lowest threshold voltages (V_t). As such, we note that inverters A and E start switching at lower input voltages V_{IN}, and the transition region in the corresponding VTCs is extremely diffused compared with other inverters. These two inverters also show the largest ON-current among A–E and so have large peaks in the short-circuit current, as shown in Fig. 3(c) and (d). As a high ON-current also leads to high drive current to the load, inverters A and E also switch the fastest, which is evident from transient responses of V_{OUT} shown in the insets of Fig. 3(c) and (d).

B. NCFET Inverter Power Analysis

Fig. 3(e)–(j) shows the power-related phase maps of NCFET inverters like pin capacitance $C_{p,\text{inv}}$, switching power $P_{\text{SW,inv}}$, average short-circuit current, internal power, total power, and the ratio of internal power to the total power. The pin capacitance plotted in Fig. 3(e) is the combination of effective gate capacitance of n-FET and p-FET, which contributes to the input pin capacitance of inverter. Switching power is the power consumed in switching all the gate and wire capacitances, whereas the total power is composed of switching power, short-circuit power, and leakage power. To generate these phase plots, a total number of 496 inverters based on n- and p-NCFETs with different ($P_\circ$, E_C) combinations were simulated.

First, we note by comparing Figs. 3(e) and 2(e) that the boost in I_{ON} is associated with a concurrent increase in the pin capacitance. This is because the voltage amplification due to the negative capacitance gate oxide layer—which causes the boost in the ON-current at a given V_{DD}—does so actually by boosting the gate charge and hence, the gate capacitance [44]. Second, the switching power map in Fig. 3(f) resembles that of pin capacitance in Fig. 3(e), which is expected since $P_{\text{SW,inv}} \propto C_{p,\text{inv}} V_{\text{DD}}^2$. Third, in Fig. 3(g) and (h), we observe that the NCFETs at the hysteresis boundary exhibit the largest short-circuit current and the largest internal power, respectively, as the power consumption is closely related to the max-current. Fourth, the total power in Fig. 3(i) resembles that of the short-circuit current, indicating that the total power is dominated by the short-circuit power. This is further confirmed by the ratio of internal to total power shown in Fig. 3(j). Note that the OFF-state leakage power is the same for all the NCFETs due to our threshold voltage adjustment procedure that ensures OFF-current remains equal to the baseline FET OFF-current. Therefore, a high subthreshold slope device that *usually* has high ON-current will lead to a high power consumption in NCFETs and is not very desirable if operated at the same voltage as BaseFET.

C. NCFET Inverter Delay Analysis

Fig. 4(a) plots the phase map of NCFET inverter delay. At $V_{\text{DD}} = [0.4]$ V, the delay of baseline inverter is 6.0 ps, and all the NCFET inverters are faster than the baseline inverter. We note that the minimum delay region in Fig. 4(a) does not coincide with the maximum power region in Fig. 3(i) or the maximum current region in Fig. 2(e): min-delay region is larger than max-power region. This shows that the most

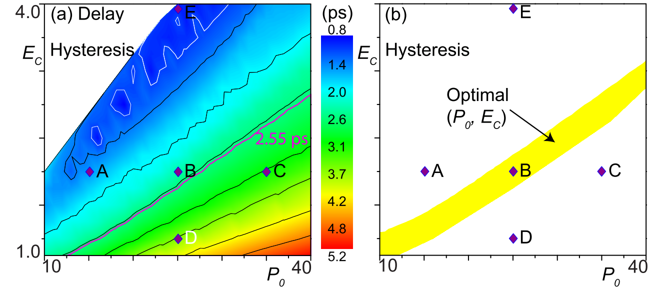

Fig. 4. (a) Delay phase map of NCFET inverters running at 0.4 V. (b) Region in (a), where the delay is 2.55 ps. Any point in this region gives a ($P_\circ$, E_C) parameter pair for an NCFET inverter that runs at 0.4 V and has the same delay as the baseline inverter running at 0.8 V (=2.55 ps). The total power saving of NCFET inverters (0.4 V) compared with baseline inverter (0.8 V) in this region ranges from 73% to 78%.

power-consuming NCFETs do not necessarily correspond to the fastest NCFETs; this point will be further elucidated in Part II of our article.

We now set the supply voltage of baseline FET to 0.8 V. The purpose is to optimize our NCFET transistors running at 0.4 V by selecting the right set of ($P_\circ$, E_C) parameters so that: 1) NCFET inverters running at 0.4 V operate as fast as the baseline inverter at the nominal voltage of 0.8 V and 2) consume the minimum power. At 0.8 V, our baseline inverter delay becomes 2.55 ps. In Fig. 4(b), we extracted the region from Fig. 4(a), where the delay is $\leq$2.55 ps and the power reduction is between 78% (maximum power reduction) and 73% (maximum-5% power reduction). From an isoperformance point of view at a given V_{DD}, an optimal set of ferroelectric parameters ($P_\circ$, E_C) is the one for which the corresponding NCFET maximally reduces the total power dissipation in the circuit while running at the same speed as the baseline FET. The total power dissipated in the baseline inverter at $V_{\text{DD}} = [0.8]$ V is 5.8 μW. Fig. 4(b) shows the ($P_\circ$, E_C) combinations for which the total power in the corresponding NCFET inverters is less than 1.48 μW.

V. Impact of Materials on NCFET Full Chip

Finally, we demonstrate the concept of optimality of ferroelectric parameters using NCFET-based full-chip implementations using LDPC as the full-chip circuit. Using the FreePDK 15-nm OCL as the model, we use the Synopsys Siliconsmart tool for characterizing all the libraries. The benchmark register transfer level (RTL) is synthesized with Synopsys Design Compiler and the placement and routing are done using Cadence Innovus. We use Synopsys PrimeTime for power and static timing analyses. Fig. 5 shows the full-chip placement and routing layouts. Further details of the full-chip design and simulation setup are provided in [10]. For the isoperformance power analysis reported herein, we implemented LDPC using NCFETs with 22 different ($P_\circ$, E_C) combinations at $V_{\text{DD}} =$ 0.4 V and achieve the same performance as the baseline FET implementations at $V_{\text{DD}} = 0.8$ V. In all designs including NCFET and baseline FET full-chip designs, timing is closed at 2.5 GHz.

A. Full-Chip Metric Comparison

Table I compares key full-chip metrics. First, we note that LDPC full-chips built with NCFETs A, B, and E provide up

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on February 21,2020 at 17:25:27 UTC from IEEE Xplore. Restrictions apply.

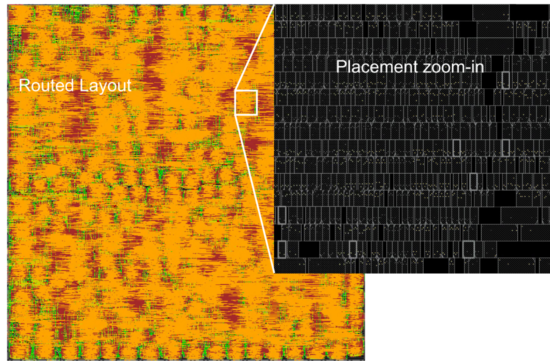

Fig. 5. Full-chip layout using 15-nm NCFET gates.

TABLE I
FULL-CHIP ISOPERFORMANCE RESULTS. THE COLUMNS IN RED FAIL TO MEET THE TARGET FREQUENCY. THE BLUE YIELD THE MAXIMUM POWER REDUCTION. POWER VALUES ARE IN mW, CAPACITANCE IN pF, WIRELENGTH IN mm, CELL AREA IN μm^2, AND SLACK IN ps

Device	LDPC					
	baseline FET (0.8 V)	NCFET A (0.4 V)	NCFET B (0.4 V)	NCFET C (0.4 V)	NCFET D (0.4 V)	NCFET E (0.4 V)
Target Freq	2.5GHz					
Slack	6.2	40.2	23.1	-65.0	-143.6	20.4
Gate Count	55400	49927	54960	64217	74109	52087
Cell Area	18942	17236	18861	23354	26089	17669
Wirelength	1008	962	994	998	1436	975
Pin Cap	260	346	298	291	278	600
Net Cap	201	186	197	200	304	189
Switching Pwr	274	77	74	70	84	113
Internal Pwr	210	85	44	54	62	534
Leakage Pwr	4.4	0.6	0.7	1.0	1.3	0.6
Total Pwr	488	162	118	125	147	648
% Reduction	0	67 %	76 %	74 %	70 %	-33 %

to 40 ps of positive slack, thereby over-achieving the corresponding target frequency. On the other hand, NCFETs C and D still fail to meet the timing goal even after using significantly more buffers and larger gates, which is evident from higher gate count and larger cell area. NCFET B implementation leads to the maximum power reduction (76%), while NCFET E implementation actually worsens power by 33% compared with the baseline FET.

Second, we note that the pin capacitance in all NCFET designs is higher than the baseline, which naturally follows from the conclusion we obtained from inverter designs. In particular, NCFET E design has a significantly larger pin capacitance—which agrees with Fig. 3(e)—and hence, a much larger switching power (P_{SW}) than other NCFET designs. Yet, NCFET E shows smaller switching power than the baseline, thanks to the dramatic supply voltage scaling (0.4 V vs. 0.8 V). The total power for NCFET is still worse than the baseline mainly due to the excessive internal power, which mainly comes from large short-circuit current [see Fig. 3(g)]. Internal power is the dynamic power consumed inside the standard cell (NAND, NOR, INV, BUF, Flip-Flop, etc.). It is a sum of the short-circuit power and the power consumed due to switching the parasitics present inside the standard cell.

Third, the net capacitance does not follow this pin capacitance trend. This is expected as negative capacitance does not directly impact interconnects. An exception is NCFET D, where even the net capacitance (304 pF) is significantly larger than the baseline (201 pF). This is mainly due to the extra nets connecting excessive buffers added to meet the timing. The overall wirelength also increased (1008 mm vs. 1436 mm) due to the excess nets.

TABLE II
NCFET COMPARISON AT THE DEVICE, GATE, AND FULL-CHIP LEVEL AMONG THE FIVE NCFETS A–E

hierarchy	metric	NC-A	NC-B	NC-C	NC-D	NC-E
device	sub-threshold slope	-	-	-	worst	best
	on-current	-	-	-	worst	best
gate	switching power	-	-	-	best	worst
	internal power	-	-	-	best	worst
	total power	-	-	-	best	worst
	delay	-	-	-	worst	best
full-chip	switching power	-	-	best	-	worst
	internal power	-	best	-	-	worst
	total power	-	best	-	-	worst
	delay	-	-	-	worst	best

B. Device, Gate, and Full-Chip Comparison

Table II shows an overall comparison among 5 NCFET types we investigated so far at the device, gate, and full-chip level. We use key metrics at these design hierarchies and select the best NCFET flavor among A, B, C, D, and E. At the device level, NCFET E shows the best quality as it provides the best subthreshold slope and ON-current values, whereas NCFET D is the worst. At the gate level, however, the conclusion splits: NCFET E is the worst in terms of power while being the best in terms of delay. This clearly demonstrates power versus performance tradeoff existing in NCFET gate designs.

At the full-chip level, we observe an interesting trend: NCFET E remains the worst in terms of power and the best in terms of performance. However, the winner in power consumption is no longer NCFET D, but NCFET B this time. The main reason is that, as Table I demonstrates, NCFET D gates are too slow that they require more buffers and larger gates to close timing at the full-chip level. NCFET B offers a good tradeoff between power and performance, where the gates are fast enough for easier timing closure while note consuming high power.

Finally, but most importantly, we observe that NCFET E, although it offers the best subthreshold slope and ON-current values at the device level, is the worst option for power reduction in our isoperformance full-chip study. This again stems from the fact that this NCFET device is primarily optimized for performance but not for power. NCFET B offers the best power saving instead, which we obtain from judiciously tuning the two key device parameters, namely, remnant polarization and the coercive field.

VI. CONCLUSION

We performed a comprehensive analysis of how the ferroelectric parameters—(P_o, E_C)—impact the performance of full-chip implementations with NCFETs. Based on this, we developed a framework for identifying the optimal ferroelectric parameters to achieve the maximal reduction of power dissipation while meeting the performance targets. In Part II, we will investigate how the optimal ferroelectric parameters change as V_{DD} is scaled and provide overall limitations and conclusions of the study.

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on February 21,2020 at 17:25:27 UTC from IEEE Xplore. Restrictions apply.

References

[1] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008, doi: 10.1021/nl071804g.

[2] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 11.3.1–11.3.4, doi: 10.1109/IEDM.2011.6131532.

[3] Z. Krivokapic *et al.*, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEDM Tech. Dig.*, Dec. 2017, pp. 15.1.1–15.1.4, doi: 10.1109/IEDM.2017.8268393.

[4] K.-S. Li *et al.*, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in *IEDM Tech. Dig.*, Dec. 2015, pp. 22.6.1–22.6.4, doi: 10.1109/IEDM.2015.7409760.

[5] W. Chung, M. Si, and P. D. Ye, "Hysteresis-free negative capacitance germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec," in *IEDM Tech. Dig.*, Dec. 2017, pp. 15.3.1–15.3.4, doi: 10.1109/IEDM.2017.8268395.

[6] K.-S. Li *et al.*, "Negative-capacitance FinFET inverter, ring oscillator, SRAM cell, and Ft," in *IEDM Tech. Dig.*, Dec. 2018, pp. 31.7.1–31.7.4, doi: 10.1109/IEDM.2018.8614521.

[7] G. Pahwa *et al.*, "Analysis and compact modeling of negative capacitance transistor with high on-current and negative output differential resistance—Part I: Model description," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4981–4985, Dec. 2016, doi: 10.1109/TED.2016.2614432.

[8] S. Khandelwal, A. I. Khan, J. P. Duarte, A. B. Sachid, S. Salahuddin, and C. Hu, "Circuit performance analysis of negative capacitance FinFETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2016, pp. 1–2, doi: 10.1109/VLSIT.2016.7573446.

[9] T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Lett.*, vol. 38, no. 8, pp. 1161–1164, Aug. 2017, doi: 10.1109/LED.2017.2712365.

[10] S. K. Samal, S. Khandelwal, A. I. Khan, S. Salahuddin, C. Hu, and S. K. Lim, "Full chip power benefits with negative capacitance FETs," in *Proc. IEEE/ACM ISLPED*, Jul. 2017, pp. 1–6, doi: 10.1109/ISLPED.2017.8009170.

[11] X. Tian, S. Shibayama, T. Nishimura, T. Yajima, S. Migita, and A. Toriumi, "Evolution of ferroelectric HfO_2 in ultrathin region down to 3 nm," *Appl. Phys. Lett.*, vol. 112, Feb. 2018, Art. no. 102902, doi: 10.1063/1.5017094.

[12] D. Kwon *et al.*, "Negative capacitance FET with 1.8-nm-thick Zr-doped HfO_2 oxide," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 993–996, Jun. 2019, doi: 10.1109/LED.2019.2912413.

[13] T. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Appl. Phys. Lett.*, vol. 99, Aug. 2011, Art. no. 102903, doi: 10.1063/1.3634052.

[14] T. Olsen *et al.*, "Co-sputtering yttrium into hafnium oxide thin films to produce ferroelectric properties," *Appl. Phys. Lett.*, vol. 101, Aug. 2012, Art. no. 082905, doi: 10.1063/1.4747209.

[15] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, and C. S. Hwanga, "Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature," *Appl. Phys. Lett.*, vol. 102, Jun. 2013, Art. no. 242905, doi: 10.1063/1.4811483.

[16] M. Hoffmann *et al.*, "Stabilizing the ferroelectric phase in doped hafnium oxide," *J. Appl. Phys.*, vol. 118, Feb. 2015, Art. no. 072006, doi: 10.1063/1.4927805.

[17] T. S. Böscke *et al.*, "Phase transitions in ferroelectric silicon doped hafnium oxide," *Appl. Phys. Lett.*, vol. 99, Aug. 2011, Art. no. 112904, doi: 10.1063/1.3636434.

[18] J. Müller *et al.*, "Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications," *Appl. Phys. Lett.*, vol. 99, Aug. 2011, Art. no. 112901, doi: 10.1063/1.3636417.

[19] J. Müller *et al.*, "Ferroelectricity in yttrium-doped hafnium oxide," *J. Appl. Phys.*, vol. 110, Nov. 2011, Art. no. 114113, doi: 10.1063/1.3667205.

[20] S. Mueller, C. Adelmann, A. Singh, S. Van Elshocht, U. Schroeder, and T. Mikolajick, "Ferroelectricity in Gd-doped HfO_2 thin films," *ECS J. Solid State Sci. Technol.*, vol. 1, no. 6, pp. N123–N126, 2012, doi: 10.1149/2.002301jss.

[21] S. Mueller *et al.*, "Incipient ferroelectricity in Al-doped HfO_2 thin films," *Adv. Funct. Mater.*, vol. 22, pp. 2412–2417, Jun. 2012, doi: 10.1002/adfm.201103119.

[22] J. Müller *et al.*, "Ferroelectricity in simple binary ZrO_2 and HfO_2," *Nano Lett.*, vol. 12, no. 8, pp. 4318–4323, 2012, doi: 10.1021/nl302049k.

[23] J. Müller *et al.*, "Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories," in *IEDM Tech. Dig.*, Dec. 2013, pp. 10.8.1–10.8.4, doi: 10.1109/IEDM.2013.6724605.

[24] M. Pešic, M. Hoffmann, C. Richter, T. Mikolajick, and U. Schroeder, "Nonvolatile random access memory and energy storage based on antiferroelectric like hysteresis in ZrO_2," *Adv. Funct. Mater.*, vol. 26, PP. 7486–7494, Nov. 2016, doi: 10.1002/adfm.201603182.

[25] T. Schenk, U. Schroeder, M. Pešic, M. Popovici, Y. V. Pershin, and T. Mikolajick, "Electric field cycling behavior of ferroelectric hafnium oxide," *ACS Appl. Mater. Interfaces*, vol. 6, no. 22, pp. 19744–19751, Nov. 2014, doi: 10.1021/am504837r.

[26] T. C. U. Tromm *et al.*, "Ferroelectricity in Lu doped HfO_2 layers," *Appl. Phys. Lett.*, vol. 111, Sep. 2017, Art. no. 142904, doi: 10.1063/1.4998336.

[27] M. Hoffmann, T. Schenk, M. Pešic, U. Schroeder, and T. Mikolajick, "Insights into antiferroelectrics from first-order reversal curves," *Appl. Phys. Lett.*, vol. 111, Oct. 2017, Art. no. 182902, doi: 10.1063/1.5003612.

[28] G. Karbasian, R. dos Reis, A. K. Yadav, A. J. Tan, C. Hu, and S. Salahuddin, "Stabilization of ferroelectric phase in tungsten capped $Hf_{0.8}Zr_{0.2}O_2$," *Appl. Phys. Lett.*, vol. 111, Jun. 2017, Art. no. 022907, doi: 10.1063/1.4993739.

[29] A. Pal, V. K. Narasimhana, S. Weeks, K. Littau, D. Pramanik, and T. Chiang, "Enhancing ferroelectricity in dopant-free hafnium oxide," *Appl. Phys. Lett.*, vol. 110, Dec. 2016, Art. no. 022903, doi: 10.1063/1.4973928.

[30] S. J. Kim *et al.*, "Large ferroelectric polarization of $TiN/Hf_{0.5}Zr_{0.5}O_2/TiN$ capacitors due to stress-induced crystallization at low thermal budget," *Appl. Phys. Lett.*, vol. 11, Dec. 2017, Art. no. 242901, doi: 10.1063/1.4995619.

[31] S. Starschich and U. Boettger, "An extensive study of the influence of dopants on the ferroelectric properties of HfO_2," *J. Mater. Chem. C*, vol. 5, pp. 333–338, Dec. 2016, doi: 10.1039/C6TC04807B.

[32] Y. H. Lee *et al.*, "Preparation and characterization of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin films grown by reactive sputtering," *Nanotechnology*, vol. 28, no. 30, 2017, Art. no. 305703, doi: 10.1088/1361-6528/aa7624.

[33] P. Polakowski *et al.*, "Ferroelectric deep trench capacitors based on Al: HfO_2 for 3D nonvolatile memory applications," in *Proc. 6th IEEE Memory Workshop (IMW)*, May 2014, pp. 1–4, doi: 10.1109/IMW.2014.6849367.

[34] Y.-C. Lin, F. McGuire, and A. D. Franklin, "Realizing ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ with elemental capping layers," *J. Vac. Sci. Technol. B, Microelectron.*, vol. 36, Nov. 2017, Art. no. 011204, doi: 10.1116/1.5002558.

[35] S. Khandelwal, J. P. Duarte, A. Medury, Y. S. Chauhan, and C. Hu, "New industry standard FinFET compact model for future technology nodes," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2015, pp. T62–T63, doi: 10.1109/VLSIT.2015.7223704.

[36] M. Martins *et al.*, "Open cell library in 15nm FreePDK technology," in *Proc. Int. Symp. Phys. Design*, 2015, pp. 171–178, doi: 10.1145/2717764.2717783.

[37] M. Hoffmann *et al.*, "Unveiling the double-well energy landscape in a ferroelectric layer," *Nature*, vol. 565, pp. 464–467, Jan. 2019, doi: 10.1038/s41586-018-0854-z.

[38] D. Kwon *et al.*, "Response speed of negative capacitance FinFETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2018, pp. 49–50, doi: 10.1109/VLSIT.2018.8510626.

[39] K. Chatterjee, A. J. Rosner, and S. Salahuddin, "Intrinsic speed limit of negative capacitance transistors," *IEEE Electron Device Lett.*, vol. 38, no. 9, pp. 1328–1330, Sep. 2017, doi: 10.1109/LED.2017.2731343.

[40] Z. C. Yuan *et al.*, "Switching-speed limitations of ferroelectric negative-capacitance FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4046–4052, Oct. 2016, doi: 10.1109/TED.2016.2602209.

[41] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Compact model for ferroelectric negative capacitance transistor with MFIS structure," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1366–1374, Mar. 2017, doi: 10.1109/TED.2017.2654066.

[42] C.-I. Lin, A. I. Khan, S. Salahuddin, and C. Hu, "Effects of the variation of ferroelectric properties on negative capacitance FET characteristics," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2197–2199, May 2016, doi: 10.1109/TED.2016.2514783.

[43] M. Kobayashi and T. Hiramoto, "On device design for steep-slope negative-capacitance field-effect-transistor operating at sub-0.2V supply voltage with ferroelectric HfO_2 thin film," *AIP Adv.*, vol. 6, Feb. 2016, Art. no. 025113, doi: 10.1063/1.4942427.

[44] S.-C. Chang, U. E. Avci, D. E. Nikonov, and I. A. Young, "Inversion charge-boost and transient steep-slope induced by free charge-polarization mismatch in a ferroelectric-metal-oxide-semiconductor capacitor," 2018, *arXiv:1804.03125*. [Online]. Available: https://arxiv.org/abs/1804.03125

Authorized licensed use limited to: Georgia Institute of Technology. Downloaded on February 21,2020 at 17:25:27 UTC from IEEE Xplore. Restrictions apply.