On the Design of Energy-Efficient I/O Circuits for Interposer-based 2.5D System-in-Package

M.Lee, J.Kim, A.Singh, H.M.Torun, M.Swaminathan, S. Lim, and S.Mukhopadhyay
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA
Email: minah.lee@gatech.edu

I. Introduction

Interposer-based 2.5D System-in-Package (SiP) allows heterogeneous integration while promising lower cost and higher yield than TSV-based 3D integration [1-3]. Communications between dies in SiP are similar to those in System-on-Chip (SoC), except SiP is using wires in silicon interposers which have larger linewidth and show inductive properties. The total number of input/output (I/O) circuits to drive on-interposer wires is much larger than off-chip I/Os in SoC. Hence, design of lightweight I/O circuits is critical for 2.5D integrations, and digital singled-ended signaling has emerged as a preferred choice.

This paper focus on the design of receiver for single-ended signaling in SiP. A single-ended receiver has small area and energy consumption, but vulnerable to noise and PVT variations. In contrast, differential receiver is robust to noise and PVT variations, but has larger area and energy consumption. In this paper, we analyze the propagation delay, energy, area, and reach (i.e. maximum wire length supported) of I/O circuits with single-ended drivers but single-ended or differential receivers. Given a wire length distribution, we propose a methodology to choose the optimal receiver design for the I/Os connecting different wires in a 2.5D system.

II. Single-Ended and Differential Receivers

Fig. 1a shows bi-directional interposer wire model in 2.5D SiP, driven by I/O circuits at the both ends. Considering a bi-directional signaling, the I/Os at the two ends of the wire must be identical. Driver circuit is a chain of CMOS inverters with constant fan-out (f), so strength of a driver is determined by the size of last inverter (D). Receiver circuit has two options; single-ended (Fig. 1b) and differential (Fig. 1c) receivers. Single-ended receiver is a chain of two CMOS inverters and thus requires full-swing signal as input. On the other hand, differential receiver can have low-swing signal as input. In this paper, we set 90% voltage swing constraint at receiver input for single-ended receiver, and 40% for differential receiver. These constraints cause different tendency of two receivers in propagation delay, energy, and area.

We use an accurate model for the on-interposer wires including micro-bumps that connects the chips to the interposer. Machine learning technique is used to generate package model capturing the impedance and coupling profiles. [4] (Fig. 2). First, training data from a full-wave EM solver, Ansys HFSS using single frequency is collected and stores the RLGC matrices. Then, Additive Gaussian Process is trained from geometric parameters of interconnects and a range of frequency, and generates the frequency dependent RLGC matrices. It is then converted to s-parameter, and generates the SPICE model. In this paper, we use two cases of package models to demonstrate the performance of single-ended and differential receiver for varying package wire dimensions (Fig. 3). Case1 has smaller

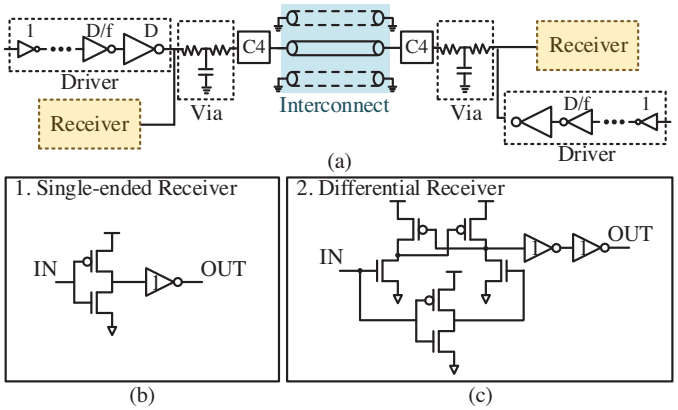


Fig. 1. (a) Bi-directional chip-interposer model and (b) single-ended, (c) Differential reciever circuits

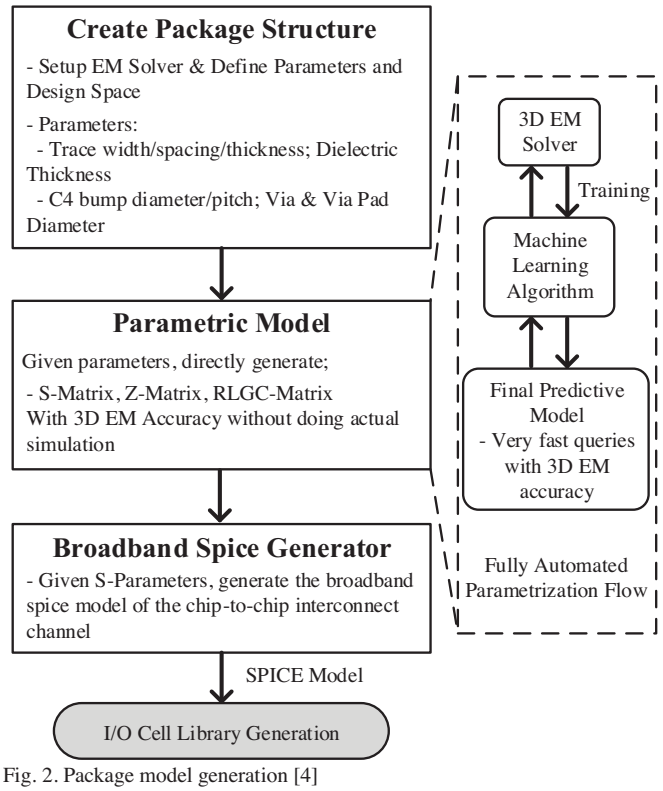
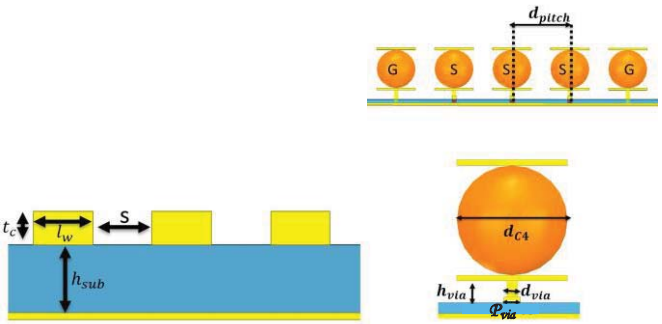


Fig. 2. Package model generation [4]

978-1-5386-7627-1/18/$31.00 ©2018 IEEE

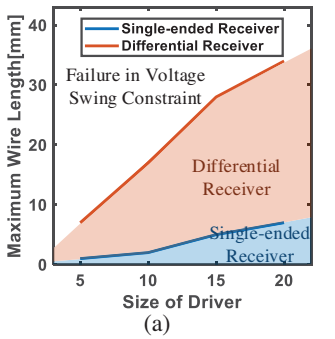


(a) (b)

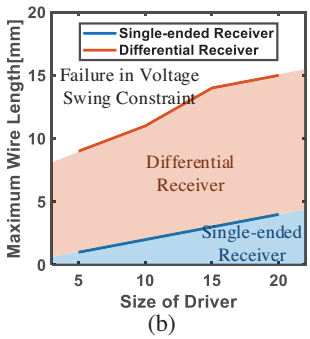
	Case 1	Case 2
Line Width(l_w)/Spacing(S)/Thickness(t_c) [μm]	0.4/0.4/1	1.6/1.6/2.0
C4 Diameter(d_{C_4})/Pitch(d_{pitch}) [μm]	25/50	25/50
Chip to interposer Via Diameter(d_{via})/Pad(P_{via})/Height(h_{via}) [μm]	0.4/0.7/5.0	1.6/2.4/2.0

(c)

Fig. 3. (a) Transmission line [4], (b) C4 bump, and (c) physical dimensions of various package models.



(a)



(b)

	Delay [ps]		Energy [pJ/bit]		Area [μm^2]	
	Single-ended	Differential	Single-ended	Differential	Single-ended	Differential
x5	123	129	0.089	0.093	2.268	4.002
x10	84	84	0.088	0.093	2.898	4.632
x15	71	71	0.096	0.101	4.914	6.648
x20	64	61	0.095	0.103	5.418	7.152

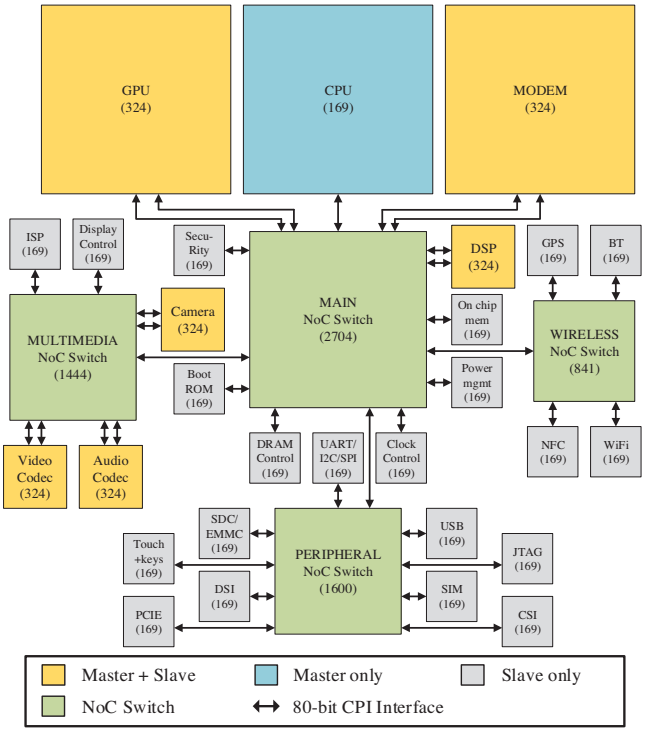
(c)

Fig. 4. (a,b) Maximum wire length that single-ended/differential receiver can drive (case2, case1 package respectively) (c) delay/energy/area of I/O with single-ended/differential receiver for given driver size

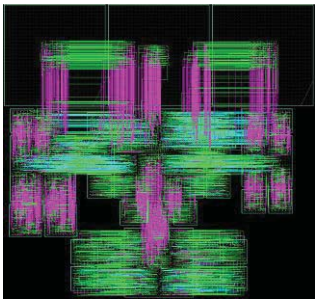
wire dimension then the case2, so interposer wires in case1 are more resistive.

A. *I/O with Fixed Driver Size*

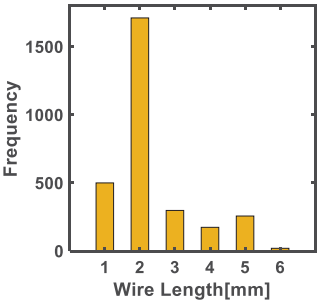
We first consider a design where the size of the driver is fixed for all I/O cells. However, a fixed size driver can only drive single-ended signal through a maximum wire length, as voltage swing of the signal at the input of the receiver reduces as wires get longer. The I/O circuits with differential receivers can correctly detect input signals with much lower voltage swing than the I/Os with single-ended receivers. Hence, for a given size of driver, the I/O circuits with differential receivers can drive much longer wires than the I/Os with single-ended receiver (Fig. 4a,b). Maximum wire length of both single-ended and



(a)



(b)



(c)

Fig. 5. (a) Floor plan, (b) Interposer routing layout, (c) wire length distribution of a chipletized generic SoC

differential receiver changes by package property. Case1 package is more resistive than case2, so for a given driver size, the maximum drivable wire length for case1 interposer is smaller than the same for the interposer case2. Delay and energy of I/O with single-ended/differential receiver for given driver size/wire length is nearly same. (0-4.8%, 4-7.5% difference respectively) (Fig. 4c). Therefore, we can use I/Os with single-ended receiver for shorter wires (up to a maximum wire length), and differential receiver for longer wires.

Fig. 5 shows a chipletized design of a generic SoC including CPU and GPU. Maximum wire length of differential receiver with x5 driver (7mm) is longer than longest length of the distribution(6mm), so x5 driver can be used for all wire lengths. Maximum wire length of single-ended receiver with x5 driver is 1mm, so single-ended receiver is used for 1mm wire and differential receiver is used for 2-6mm. This set of I/Os has 306ps worst delay, 0.115pJ/bit average energy consumption, and 22.3μm^2 area.

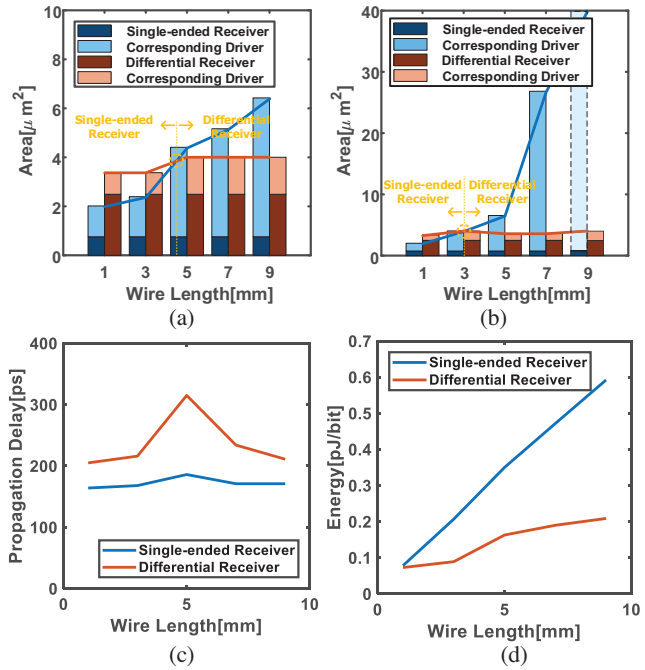


Fig. 6. (a,b) Area of driver and receiver for case2 package, case1 package respectively. (c) propagation delay, (d) energy of I/O with single-ended and differential receiver for several wire lengths

Table 1. I/O with all single-ended, all differential, and mix of single-ended and differential receiver for a wire length distribution

	All Single-ended	All Differential	Single-ended & Differential
Driver sizes	x3-x16	x2-x5	x3-x5
Worst delay [ps]	**189**	315	315
Average Energy [pJ/bit]	0.170	**0.107**	0.152
Area [μm^2]	18.1	21.9	**18.0**

B. Energy Minimized I/O

Energy consumption of I/O for a given wire length is proportional to the size of driver, so minimum size of driver that satisfies the voltage swing constraint at receiver input may achieve both energy and area minimization. Fig. 6a,b shows the area of energy minimized I/O (driver and receiver) for each given length of wires.

When the wire is short, I/O with single-ended receiver is smaller than I/O with differential receiver. This is because area of a differential receiver (dark red) is bigger than the area of a single-ended receiver (dark blue). However, as wire becomes longer, the size of driver for single-ended receiver (light blue) grows faster than for differential receiver (light red) because of larger voltage swing constraint. Therefore, I/O with single-ended receiver occupies larger area than I/O with differential receiver for long wire. On the other hand, for all wire length, I/O with differential receiver has longer delay (25-105%) and less energy consumption (6-70%) compared to I/O with single-ended receiver (Fig. 6c,d). This is because I/O with differential receivers always have smaller driver size resulting in longer delay and smaller energy consumption.

The critical wire length after which I/O with single-ended receiver become larger than I/O with differential receiver varies by the interposer design. (Fig. 6a, b) Due to the higher wire resistance, the critical wire length for the interposer in case 1 is shorter than the same in case 2.

Consider the wire length distribution in Fig. 5c again. Given a wire length distribution, we now have three approaches to design energy-minimized I/O circuits: (Table 1)

(1) All I/Os with single-ended receivers and corresponding energy minimized driver. This set of I/Os decrease worst delay, because single-ended receiver always have smaller delay than differential.

(2) All I/Os with differential receivers and corresponding energy minimized driver. In this case, average energy is reduced because differential receiver always have smaller energy consumption.

(3) A mix of I/Os with single-ended and I/Os with differential receivers, each with corresponding energy minimized drivers. I/Os can have single-ended receiver for a range of short wires and have differential receiver for longer wires, which leads to the area reduction.

In summary, worst delay, average energy, or area can be decreased by choosing single-ended or differential receiver for each length of wires.

III. Conclusion

This paper presents the impact of single-ended and differential receivers in SiP and how to choose these receivers for various situations. I/O can have one size of driver whose maximum wire length with differential receiver is longer than the longest wire it drives. Area of I/O can be reduced by using single-ended receiver for short wires and differential receiver for long wires. Energy minimized I/Os have different size of drivers for each wire length, and single-ended/differential receivers can be chosen to reduce delay, energy, or area.

ACKNOWLEDGEMENT: This research is funded by the DARPA CHIPS project under Award N00014-17-1-2950.

References

[1] K. Saban, “Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency”, Xilinx WP380.

[2] L. England and I. Arsovski, "Advanced packaging saves the day! — How TSV technology will enable continued scaling," 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, 2017, pp. 3.5.1-3.5.4.

[3] I. Bolsens, “2.5D ICs: Just a stepping stone or a long term alternative to 3D?”, Keynote Talk at 3-D Architectures for Semiconductor Integration and Packaging Conference (2011).

[4] H. M. Torun, M. Larbi, and M. Swaminathan, "A Bayesian Framework for Optimizing Interconnects in High Speed Channels," IEEE International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization (NEMO), 2018.