Parameter Extraction and Power/Performance Analysis of Monolithic 3-D Inverter (M3INV)

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***Abstract*— An equivalent circuit model of monolithic 3-D inverter (M3INV) considering the electrical coupling between the stacked metal–oxide–semiconductor field-effect transistors (MOSFETs) is proposed. We conduct the parameter extraction with technology computer-aided design (TCAD) simulations, where LETI-UTSOI model in HSPICE is used for the bottom PFET and the top NFETs. Their parameters are extracted by fitting their current–voltage (for dc analysis) and capacitance–voltage (for transient ac analysis) characteristics. The parameters extracted from the LETI-UTSOI model contain the electrical coupling at the gate of the bottom MOSFET. In order to extract external capacitances such as monolithic intertier via (MIV)-to-MIV and MIV-to-contact in M3INV, we use two structures, the first that contains MIVs and metal lines and the second that does not. We observe that the dc and transient characteristics of M3INVs built using our extracted parameters match the TCAD mixed-mode circuit simulation results considerably well. Finally, we build and analyze ring oscillators using our M3INV to demonstrate the coupling impact on power and performance.**

***Index Terms*— Circuit simulation, compact modeling, coupling, monolithic 3-D integrated circuit (IC), parameter extraction.**

I. Introduction

MONOLITHIC 3-D integration, where each layer is stacked vertically and sequentially over the previously fabricated layers, is an emerging and promising technology that enables ultrafine-grained vertical integration of devices and interconnections. This technology can offer a convincing pathway to lower power consumption, higher operating frequency, multifunction, and potential cost reduction in integrated circuits (ICs) [1]–[9].

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There have been extensive studies of process and device technologies for monolithic 3-D ICs (M3ICs) [2]–[10], but most of them have ignored the electrical coupling between stacked devices in M3IC. It has been recently reported that when the interlayer dielectric (ILD) distance T_{ILD} of the monolithic 3-D inverter (M3INV) is very thin (<50 nm in the case of SiO_2 for ILD material), the SPICE model for the metal–oxide–semiconductor field-effect-transistor (MOSFET) devices in the stack [11] cannot be used directly due to their electrical coupling [12], [13]. In order to simulate the M3INVs (or M3ICs) consisting of coupled devices, an accurate electrical model that includes the coupling between the stacked devices is essential. This goal cannot be achieved unless key electrical parameters are accurately extracted, because they are used as initial parameters when modeling the transistor behavior. The correct extraction of the M3INV electrical parameters is thus extremely important for the adoption of the technology.

In this paper, we propose an equivalent circuit of the M3INV with coupled MOSFETs. Our parameter extraction method for the equivalent circuit of M3INV is described (Section II). Next, dc and ac transient parameters are extracted (Sections III and IV). We compare the extraction results with the technology computer-aided design (TCAD) mixed-mode circuit simulation results (Section III). We also provide the power and delay impact study of the parasitics in ring oscillators (ROs) (Section IV). Finally, Section V concludes this paper.

II. Parameter Extraction Method

Fig. 1 shows the schematics of our M3INV structure [12]. Fig. 1(a) and (b) shows the 3-D structures of M3INV with and without monolithic intertier vias (MIVs) and metal lines (MLs), respectively. Fig. 1(c) shows the cross section of A–A' cutline shown in Fig. 1(a). We use both the structures to extract internal and external capacitances more accurately. Our M3INV consists of nMOSFET and pMOSFET in the upper and lower tiers, respectively. The channel width of pMOSFET is larger than that of nMOSFET in accordance with their mobility differences [7]: the channel widths of nMOSFET and pMOSFET are 200 and 290 nm, respectively. The doping concentration of source (S)/drain (D), lightly-doped drain under the side-wall, the channel, and the substrate in each MOSFET are 10^{21}, 10^{18}, 10^{15}, and 10^{17} cm^{-3}, respectively.

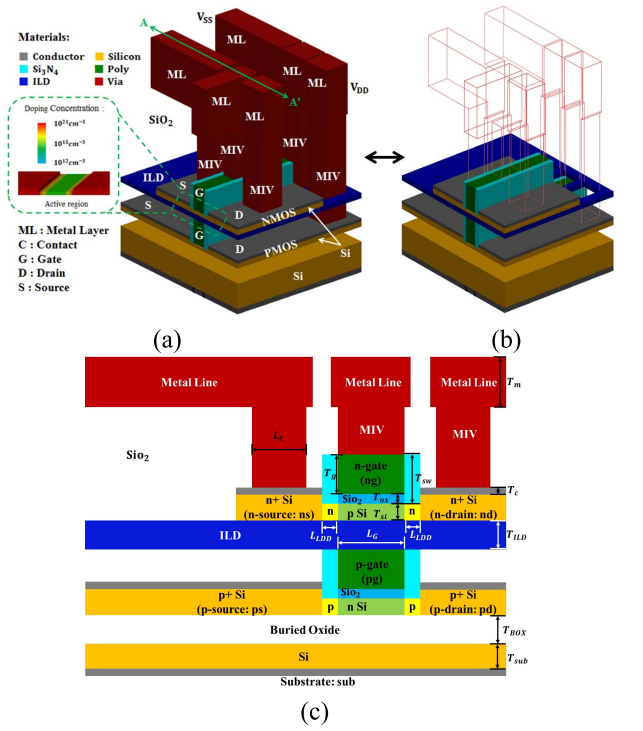

Fig. 1. Schematics of our M3INV cell structure. (a) Structure with MIVs and MLs. (b) Structure without MIVs and MLs. (c) 2-D cross section of A–A' cutline in (a). The materials used and doping concentration in silicon body are shown with different colors.

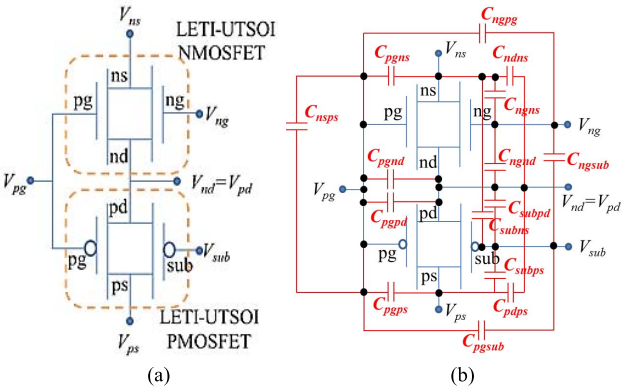

Fig. 2. Equivalent circuit of M3INV. (a) Internal capacitance only, where the MOSFET models are used. (b) Both internal and external capacitances, where the coupling capacitance caused by MIVs and MLs are added. C_{ndpd}, C_{nsps}, C_{subns}, and C_{subps} are negligible because n-drain (nd) and p-drain (pd) are common and sources (ns and ps) and substrate (sub) are biased as dc.

Detailed length and thickness of the M3INV structure are shown in Table I. SiO_2 is used for all insulators at the gate, ILD, and Box. N-poly and P-poly silicon are used for the gate material of nMOSFET and pMOSFET, respectively.

Fig. 2 shows an equivalent circuit of our M3INV. Fig. 2(a) shows an equivalent circuit of M3INV without MIVs and MLs. Because the top nMOSFET has an asymmetric and independent double-gate SOI MOSFET structure, BSIM-IMG (version 102.8) [11] or LETI-UTSOI MOSFET (version 2.1) [11], [14] models can be used for the top nMOSFETs in M3INV. The

TABLE I
DEVICE/ELECTRICAL PARAMETER DESCRIPTIONS AND DIMENSIONS [12]

Symbols	Description	Value/Unit
L_G	Gate length	30 nm
L_{LDD}	Lightly-doped drain length	10 nm
L_c	Contact length	50 nm
T_g	Gate thickness	30 nm
T_{ox}	Gate-oxide thickness	1 nm
T_{si}	Silicon-channel thickness	6 nm
T_{sw}	Sidewall thickness	31 nm
T_{BOX}	Buried-oxide thickness	30 nm
T_{sub}	Silicon substrate thickness	50 nm
T_c	Contact thickness	6 nm
T_{ILD}	ILD thickness	10 nm
T_m	ML thickness	100 nm
ε_{ox}	Oxide dielectric constant	3.9
ε_{si}	Silicon dielectric constant	11.8
ε_{ILD}	ILD dielectric constant	3.9
V_{ngs}/V_{pgs}	Gate-source voltages of top/bottom MOSFETs	V
V_{nds}/V_{pds}	Drain-source voltages of top/bottom MOSFETs	V
V_{sub}	Substrate voltage	V
I_{nds}/I_{pds}	Drain-source currents of top/bottom MOSFETs	A
g_m	Transconductance ($g_m = dI_{nds}/dV_{ngs}$ or dI_{pds}/dV_{pgs})	S
C_{ngng}/C_{pgpg}	Gate capacitances of top/bottom MOSFETs	F
C_{ngns}/C_{pgps}	Gate-source capacitances of top/bottom MOSFETs	F
C_{ngnd}/C_{pgpd}	Gate-drain capacitances of top/bottom MOSFETs	F
C_{ndns}/C_{pdps}	Drain-source capacitances of top/bottom MOSFETs	F
C_{ngpg}	Gate-gate capacitance between top and bottom MOSFETs	F
V_{IN}	Input voltage of M3INV	V
V_{OUT}	Output voltage of M3INV	V
t_d	Propagation delay of M3INV	s
t_r/t_f	Rising/falling times of M3INV	s

bottom transistor of M3INV is a well-known SOI structure with a Si substrate, and the BSIM-SOI and LETI-SOI models are generally used for the SOI structure. However, because p-type BSIM-SOI model has one problem that the positive bulk–source bias is negatively applied and M3INV has the ultrathin body SOI of below 10 nm, the LETI-UTSOI MOSFET model [11], [16] is suitable for the bottom pMOSFET. Instead of using two different models (LETI-UTSOI and BSIM-IMG) for the bottom pMOSFET and top nMOSFET, a single model (LETI-UTSOI MOSFET model) for both pMOSFET and nMOSFET is used.

Fig. 2(b) shows the equivalent circuit including both internal capacitances (by the bottom and top MOSFETs) and external capacitances (by MIVs and MLs). These reference data are used in our TCAD simulation using ATLAS [15]. The models used for TCAD simulation are CVT, SRH, AUGER, and FERMI. The circuit parameters of M3INV used in our HSPICE simulation [11] are extracted from the reference data using the following parameter extraction procedure: first, the SPICE dc/transient parameters of each stacked MOSFET are extracted by fitting the TCAD device simulation results of M3INV without MIVs and MLs. Second, dc/transient response of M3INV obtained with HSPICE using the extracted parameters is verified with TCAD mixed-mode circuit simulations of M3INV. Finally, using TCAD simulation, the external

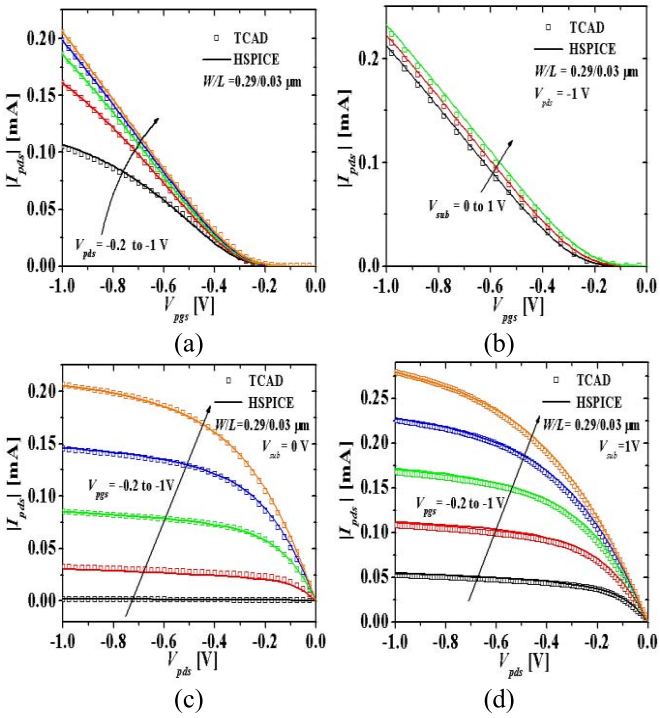

Fig. 3. Current–voltage characteristics of the bottom pMOSFET. (a) I_{pds}–V_{pgs} characteristics at different V_{pds} and V_{sub} = 0 V. (b) I_{pds}–V_{pgs} characteristics at different V_{sub} and V_{pds} = −1 V. (c) I_{pds}–V_{pds} characteristics at different V_{pgs} and V_{sub} = 0 V. (d) I_{pds}–V_{pds} characteristics at different V_{pgs} and V_{sub} = 1 V. The squares and lines denote TCAD and HSPICE simulation results, respectively. We use $W/L = 0.29/0.03$ μm.

capacitances are extracted from the capacitance differences between the case with versus without MIVs and MLs, where a gate–source voltage is applied under the subthreshold region of MOSFET operation.

III. DC Parameter Extraction

Fig. 3 shows the current–voltage characteristics of the bottom pMOSFET. We show the following four simulation results. Fig. 3(a) I_{pds}–V_{pgs} characteristics under V_{pds} (=−0.2, −0.4, −0.6, −0.8 and −1 V) and V_{sub} = 0 V. Fig. 3(b) I_{pds}–V_{pgs} characteristics under V_{sub} (=0, −0.5, and −1 V) and V_{pds} = −1 V. Fig. 3(c) I_{pds}–V_{pds} characteristics under V_{pgs} (=−0.2, −0.4, −0.6, −0.8, and −1 V) and V_{sub} = 0 V. Fig. 3(d) I_{pds}–V_{pds} characteristics under V_{pgs} (=−0.2, −0.4, −0.6, −0.8, and −1 V) and V_{sub} = 1 V. The squares and lines denote our TCAD and HSPICE simulation results, respectively. Following the parameter extraction procedure in [16], we extract the parameters of LETI-UTSOI MOSFET model as shown in Table II. We observe that HSPICE simulation results match those of TCAD simulation accurately.

Fig. 4 shows the current–voltage characteristics of the top nMOSFET. We show the following four simulation results. Fig. 4(a) I_{nds}–V_{ngs} characteristics under V_{nds} (=0.2, 0.4, 0.6, 0.8, and 1 V) and V_{pgs} = 0 V Fig. 4(b) I_{nds}–V_{ngs} characteristics under V_{pgs} (=0, 0.5, and 1 V) and V_{nds} = 1 V. Fig. 4(c) I_{nds}–V_{nds} characteristics under V_{ngs} (=0.2, 0.4, 0.6, 0.8, and 1 V) and V_{pgs} = 0 V. Fig. 4(d) I_{nds}–V_{nds} characteristics under V_{ngs} (=0.2, 0.4, 0.6, 0.8, and 1 V) and V_{pgs} = V_{ngs}, respectively. In Fig. 4(d), the gates in both tiers are applied

TABLE II
Summary of the Extracted Parameter of LETI-UTSOI Model for the Bottom PMOSFET

Parameter	Unit	Description	Value
DLQ	m	Effective channel length offset CV	$4e^{-8}$
LAP	m	Effective channel length reduction per side	$1e^{-9}$
VFBO	V	Geometry-independent flat-band voltage	0.26
CICO	-	Geometry-independent part of substrate bias dependence factor of interface coupling	0.65
CFL	V^{-1}	Length dependence of DIBL	1.3
UO	$m^2/V/s$	Zero-field mobility	$2.1e^{-2}$
MUEO	m/V	Mobility reduction coefficient	2.6
THEMUO	-	Mobility reduction exponent	1.22
FETAO	-	Effective field parameter	5.1
PSCEL	-	Length dependence of short channel effect above threshold	0.18
THESATO	V^{-1}	Geometry-independent velocity saturation parameter	4.2
AXO	-	Geometry-independent of linear/saturation transition factor	1.6
ALPL1	-	Length dependence of CLM pre-factor ALP	0.0005
VPO	V	CLM logarithm dependence factor	0.04
CGBOVL	F	Oxide capacitance for gate-substrate overlap	$9e^{-16}$
CFRW	F	Outer fringe capacitance	$2.2e^{-16}$

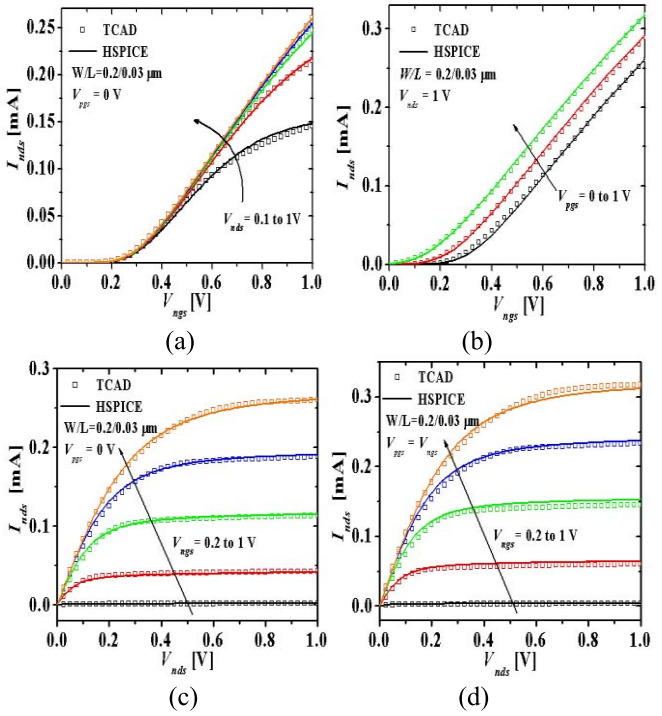

Fig. 4. Current–voltage characteristics of the top nMOSFET. (a) I_{nds}–V_{ngs} characteristics at different V_{nds} and V_{pgs} = 0 V. (b) I_{nds}–V_{ngs} characteristics at different V_{pgs} and V_{nds} = 1 V. (c) I_{nds}–V_{nds} characteristics at different V_{ngs} and V_{pgs} = 0 V. (d) I_{nds}–V_{nds} characteristics at different V_{ngs} when V_{pgs} = V_{ngs}. The squares and lines denote TCAD and HSPICE simulation results, respectively. We use $W/L = 0.2/0.03$ μm.

TABLE III
SUMMARY OF THE EXTRACTED PARAMETER OF LETI-UTSOI MODEL FOR THE TOP NMOSFET

Parameter	Unit	Description	Value
DLQ	m	Effective channel length offset CV	$4e^{-8}$
LAP	m	Effective channel length reduction per side	$1e^{-9}$
VFBO	V	Geometry-independent flat-band voltage	-0.31
CICO	-	Geometry-independent part of substrate bias dependence factor of interface coupling	0.7
CFL	V^{-1}	Length dependence of DIBL	0.4
UO	$m^2/V/s$	Zero-field mobility	$5.77e^{-2}$
MUEO	m/V	Mobility reduction coefficient	2.52
THEMUO	-	Mobility reduction exponent	1.8
FETAO	-	Effective field parameter	2.6
PSCEL	-	Length dependence of short channel effect above threshold	0.09
THESATO	V^{-1}	Geometry-independent velocity saturation parameter	6.75
AXO	-	Geometry-independent of linear/saturation transition factor	1.8
ALPL1	-	Length dependence of CLM pre-factor ALP	0.0002
VPO	V	CLM logarithm dependence factor	0.04
CGBOVL	F	Oxide capacitance for gate-substrate overlap	0
CFRW	F	Outer fringe capacitance	$2.2e^{-16}$

as common ($V_{ngs} = V_{pgs}$) because they are used as one input in the inverter. The drains in both MOSFETs are common ($V_{nds} = V_{pds}$) and can be operated as the output. The squares and lines denote our TCAD and HSPICE simulation results, respectively. Following the parameter extraction procedure in [16], we extract the parameters of LETI-UTSOI model as shown in Table III. We observe that HSPICE simulation results match those of TCAD simulation accurately.

In order to verify the validity of the extracted dc parameters, the M3INV coupled between the stacked MOSFETs, voltage transfer characteristics (VTCs) of M3INV are obtained with TCAD mixed-mode circuit simulations in ATLAS [15]. In TCAD mixed-mode simulation, the dc/transient analysis of M3INV without any MIVs and MLs was performed. This simulation provides a viable way to obtain accurate descriptions of the electrical coupling effects between the stacked MOSFETs in M3INV because there exist no compact models of the M3INV [12]. Fig. 5 shows VTCs of the M3INV for two different substrate voltages ($V_{sub} = 1$ and 0 V). Squares (and solid lines) and circles (and dashed lines) denote the substrate biased with V_{dd} (=1 V) and ground, respectively. We observe that HSPICE simulation results match TCAD simulation results considerably well. It shows that the HSPICE model of M3INV reflects well the dependence on the substrate bias.

IV. AC/TRANSIENT PARAMETER EXTRACTION

In order to accurately perform ac/transient analysis of M3INV, transconductance g_m ($= dI_{nds}/dV_{ngs}$ or dI_{pds}/dV_{pgs}), and capacitances obtained from TCAD simulations are fitted with HSPICE simulations at a frequency of 1 MHz. TCAD simulations of M3INV with and without MIVs and MLs can be used to calculate both the internal and external capacitances.

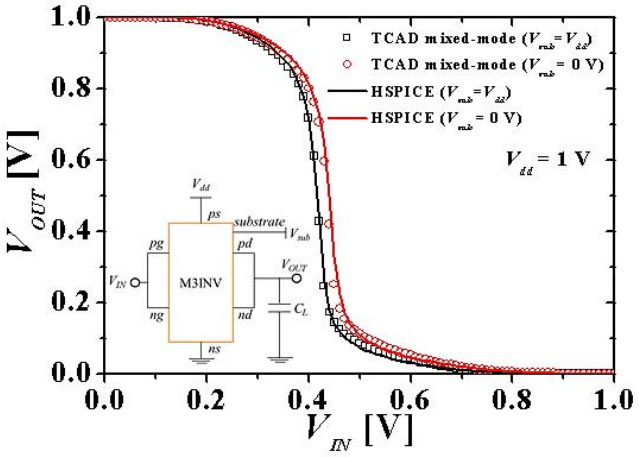

Fig. 5. VTCs of M3INV. The symbols and lines denote TCAD mixed-mode and HSPICE simulation results, respectively. Squares (and solid lines) and circles (and dashed lines) denote $V_{sub} = V_{dd}$ and 0 V (grounded), respectively. V_{dd} (=1 V) is the dc bias of M3INV. Inset: external bias of M3INV.

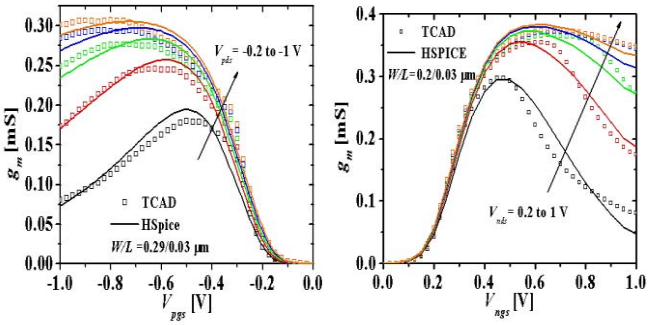

Fig. 6. (a) Transconductance–voltage characteristics at different drain–source voltages. (a) Bottom pMOSFET when $V_{sub} = 0$ V. (b) Top nMOSFET when $V_{pgs} = 0$ V. The squares and lines denote TCAD and HSPICE simulation results, respectively.

First, the internal capacitances in each stacked MOSFET are extracted using TCAD simulation results, where MIVs and MLs are excluded as shown in Fig. 1(b). The external capacitances are extracted using TCAD simulations, where both MIVs and MLs are included as shown in Fig. 1(a). Thus, we obtain the external capacitance value from the difference between the two structures: with MIVs/MLs versus without MIVs/MLs.

Fig. 6(a) and (b) shows the g_m-gate voltage characteristics of the top and bottom MOSFETs in M3INV, respectively. When the drain–source voltage is 0.2 V for the top MOSFET and −0.2 V for the bottom, we observe a minor mismatch at high gate–source voltage values. However, we observe that our HSPICE simulation results match closely with those of TCAD simulations in overall.

Fig. 7(a) shows the total gate capacitance (C_{pgpg}) of the bottom pMOSFET in M3INV. Fig. 7(b) shows the total gate capacitance (C_{ngng}) of the top nMOSFET in M3INV. The symbols and lines denote TCAD and HSPICE simulation results, respectively. The blank and filled symbols denote

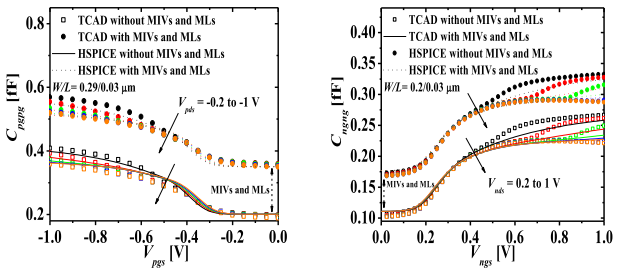

Fig. 7. (a) Gate capacitance (C_{pgpg}) of bottom pMOSFET at different V_{pds}s and $V_{sub} = 0$ V. (b) Gate capacitance (C_{ngng}) of the top nMOSFET at different V_{nds} and $V_{pgs} = 0$ V. The symbols and lines denote TCAD and HSPICE simulation results, respectively. The filled symbols (and dashed lines) and blank symbols (and solid lines) denote TCAD (and HSPICE) simulation results of M3INV with and without MIVs and MLs, respectively. The parameters (for capacitances) of M3INV with MIVs and MLs are extracted from HSPICE simulations.

TABLE IV
SUMMARY OF EXTERNAL CAPACITANCES. C_{NDNS}, C_{NGSUB}, C_{PGSUB}, AND C_{PDPS} ARE NOT SHOWN BECAUSE THEY ARE NEGLIGIBLE SMALL

Capacitances	Values [fF]	Capacitances	Values [fF]
C_{ngnd}	0.0325	C_{ndps}	0.0001
C_{ngns}	0.0316	C_{pgpd}	0.08
C_{ngpd}	0.0018	C_{pgps}	0.08
C_{ngps}	0.0006	C_{pgnd}	0.0007
C_{ngpg}	0.006	C_{pgns}	0.0007
C_{nspd}	0.0002	C_{subpd}	0.0011
C_{nsps}	0.0002	C_{subps}	0.0045
C_{ndpd}	0.009		

TCAD simulation results of M3INV with and without MIVs and MLs, respectively.

The external capacitance is extracted from the capacitance differences between including versus excluding MIVs and MLs. We use $V_{pgs} = 0.5$ V (or $V_{ngs} = -0.5$ V) as a bias point in the subthreshold region because the external capacitances are independent of the bias, which are shown in Table IV.

Fig. 8 shows the transient response of M3INV shown in Fig. 5 (inset). Load capacitance $C_L = 1$ fF is used. Symbols and lines denote TCAD mixed-mode circuit simulation and HSPICE simulation results of M3INV, respectively. Black squares (and solid lines), red circles (and solid lines), and blue triangles (and solid lines) denote the input voltage V_{IN}, output voltages V_{OUT}s of M3INV with and without MIVs and MLs, respectively. The HSPICE simulation results match closely with those of TCAD mixed-mode. Error of the propagation delay for the high-to-low transition $t_{d(HL)}$ is 0.9 $\sim$ 1.9%, and error of falling time t_f, and rising time t_r is 3.2 $\sim$ 7.2% between the HSPICE results and the TCAD mixed-mode. In the M3INV structure that includes MIVs and MLs, the propagation delay for the high-to-low transition $t_{d(HL)}$, falling time t_f, and rising time t_r is larger than those in the M3INV without MIVs and MLs, as shown in Table V. This is due to the additional coupling capacitances introduced by MIVs and MLs.

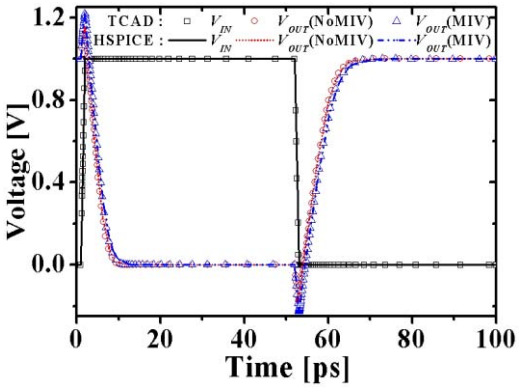

Fig. 8. Transient response of M3INV. Symbols and lines denote TCAD mixed-mode circuit simulation and HSPICE simulation results of M3INV, respectively, and black squares (and solid lines), red circles (and solid lines), and blue triangles (and solid lines) denote the input voltage V_{IN}, output voltages V_{OUT}s of M3INV with and without MIVs and MLs, respectively. Load capacitance $C_L = 1$ fF.

TABLE V
INVERTER TRANSIENT ANALYSIS

Symbols	TCAD		Hspice	
	W/O MIVs and MLs	With MIVs and MLs	W/O MIVs and MLs	With MIVs and MLs
$t_{d(HL)}$	3.29 ps	3.7 ps	3.32 ps (0.9%)	3.77 ps (1.9%)
t_f	4.38 ps	4.56 ps	4.55 ps (3.8%)	4.89 ps (7.2%)
t_r	7 ps	7.42 ps	7.23 ps (3.2%)	7.92 ps (6.7%)

TABLE VI
FO3 RO PERFORMANCE USING M3INV MODELS WITHOUT MIV AND MLS

Stages	Power (μW)	Frequency (GHz)	Delay per stage (ps)
3	283	17	8.1
19	283	2.61	8.29
101	284	0.49	8.9

TABLE VII
FO3 RO PERFORMANCE USING M3INV MODELS WITH MIV AND MLS

Stages	Power (μW)	Frequency (GHz)	Delay per stage (ps)
3	298	11.96	12.6
19	297	1.81	13.3
101	301	0.34	13.7

Tables VI and VII show the power consumption and performance of fan-out-3 (FO3) RO built using our M3INV. The ROs in Table VI do not contain parasitics originated from MIVs and MLs, whereas the ones in Table VII do. Thus, the comparison between Tables VI and VII reveals the impact of these parasitics on the power and performance of RO-based circuits. First, we note that the parasitic impact on power is minimal, where the degradation is only 15 μW

roughly for all three ROs. However, the impact on delay is significant: the increase is almost 55% in all three ROs. This reduces the operating frequency of our 101-stage RO from 0.49 to 0.34 GHz. This calls for more rigorous approaches in reducing MIV and ML-related parasitics.

V. Conclusion

In this paper, we studied the parameter extraction of M3INV considering the electrical coupling between the stacked MOSFETs. We targeted both the parasitics internal and external to the stacked MOSFETs in this paper and focused on how the neighboring vias and MLs affect the dc and ac behaviors of our devices, inverter, and RO. The accuracy of our models is fully verified with the comparison to TCAD device and mixed-mode circuit simulations. Our simulations showed that the impact of these parasitics on delay is significant.

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