Chip/Package Co-Analysis and Inductance Extraction for Fan-Out Wafer-Level-Packaging

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***Abstract*—Advanced packaging technology integrates multiple dies closely with package routing for higher performance and lower power. However, electrical and magnetic field interaction between chip wires and package requires careful parasitic extraction. For the first time, we provide comprehensive CAD flows for extracting parasitic inductance elements in the package-to-die (P2D) interface layers. We propose new full-chip loop-based inductance extraction methodologies using halo ground and bundle creation. This extraction engine is integrated in our P2D flow to extract chip/package inductive coupling elements efficiently and accurately. Our extraction engine needs only 0.63s computing time with an average self and mutual inductance error of 2.8% and 5.3%.**

I. Introduction

Fan-out wafer-level-packaging (FOWLP) is a low-cost multi-die packaging solution with excellent thermal and high frequency properties, and extremely thin layer thicknesses using the back-end-of-line (BEOL) technology. It provides a low-cost 2.5D solution and overcomes some disadvantages of 3D ICs. Because chips are spread out in a wider area, heat dissipation is much easier in FOWLP, and the power supply can also be more reliable, since additional PG bumps can fit into the die footprint.

To further increase the IO density, aluminum pads must be fabricated with a much smaller pitch, which requires further scaling of the package-to-die(P2D) distance. A recent announcement from Amkor Technology showed a 2μm P2D distance using a BEOL technology to fabricate redistribution layers (RDLs).

Existing works, whether from the chip [2] or package side [1], [4], either ignore the other side completely, or make assumptions that the chip (or package) layers can be approximated as ground planes or power delivery networks (PDNs). We demonstrate that these methods are insufficient for signal integrity analysis without using actual chip layout and detailed signal routing. Using a pure ground plane significantly overestimates P2D coupling while removing signals routing underestimates the coupling. Therefore, P2D extraction, especially within those interface layers, is still an open problem.

In this paper, we provide a first-of-its-kind comprehensive CAD methodology for fast and accurate inductance extraction of both chip and package layers. First, to reduce circuit simulation time complexity, loop-based inductance extraction methodology is used to significantly reduce number of elements extracted from the layout. Second, a novel halo ground approximation methodology is proposed based on the observation of skin effects and proximity effects on package layers. In addition, we fully verify our methods against commercial tools for accuracy and apply them on 2.5D designs with detailed chip and package layouts.

II. Field Solver Analysis

To demonstrate P2D coupling impacts, we generate several sample structures and use field solvers to obtain parasitic elements. Further, we create several FOWLP benchmark designs to demonstrate our methodologies with large-scale multi-die systems. We use a 45nm technology with seven metal layers for the chip, in which the top metal (M7) is similar to the aluminum pad (AP) layer in a traditional 2D design. Our base circuit for the chip is an FFTx1 design that contains 1.15 million cells with a footprint of 1.5×1.5mm. Then a 2.5D design named as FFTx4 is created by mounting four FFTx1 chips on the same package, forming a 2-by-2 array. The FFTx4 layout shot is shown in Figure 1.

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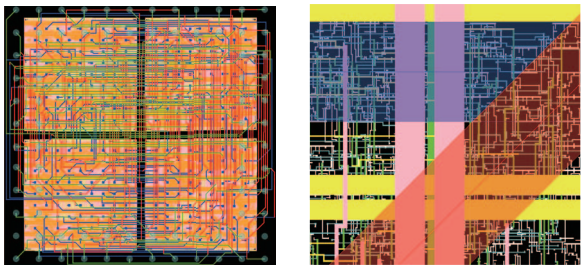

Fig. 1. FOWLP FFTx4 design layout.

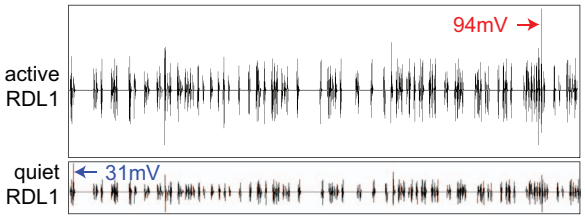

Fig. 2. Inductance-induced noise on the M7 victim from package aggressors.

A. P2D Interface Inductance Analysis

On the other hand, magnetic coupling becomes important in high frequency range. We build a sample structure with five ports and use full-wave solver Hyperlynx to obtain the extracted netlist. We select one wire on M7 as victim, which couples to all five aggressors on RDL1 as well as other wires on M7. Figure 2 compares the noise waveform on M7 victim whether RDL1 aggressors are active or not. With quiet RDL1 aggressors, the victim is only receiving intra-die coupling noise with a maximum voltage of 31mV. However, if RDL1 aggressors are turned on, the worst case noise on the victim is 94mV which is more than three times as mush as the intra-die coupling.

With active RDL aggressors, we further analyze signal waveforms with netlists containing different parasitic elements. Figure 3 shows eye diagrams of aggressor nets and noise waveforms on victim nets. As results show, with only RC elements, there is a significant underestimation of noises on victim and aggressor nets, because the signal oscillation is ignored. The inductance results in a much

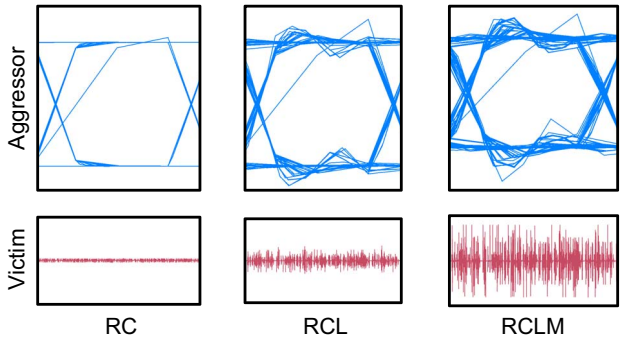

Fig. 3. Eye diagram comparison with various parasitic elements.

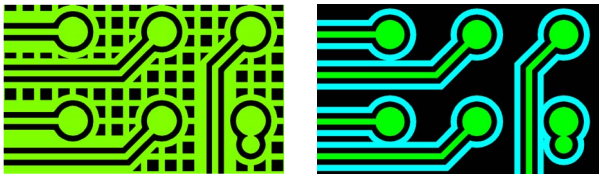

Fig. 4. RDL1 layout with (a) original ground plane, (b) halo ground approximation.

higher signal noise than the capacitance for interface layers. This case validates our motivation that package-induced noise on chip wires is significant in high frequencies, and we need accurate extraction tools that extracts inductance elements within interface layers.

III. P2D Extraction Methodology

A. Halo Ground Approximation

One challenge for the chip tools in handling package routing is the large dimension ratio between package and chip wires. The package routing layer is generally covered by power and ground planes to protect package routing signals. These planes fully cover the empty space between wires and contain hatches for manufacturability. One example is shown in Figure 4(a), where the RDL1 layer is covered by the ground. These ground planes further shield capacitive coupling to the package routing, and serve as return paths to package signals.

Our halo ground is based on the observation of both skin effects and proximity effects. Current tends to concentrate in a small area close to the surface of the wire because of the skin effect. Currents in neighboring conductors going in opposite direction are drawn closer to each other due to the proximity effect. These well-known effects are critical in high frequency ranges. If the signal frequency is low, current return is determined by the resistance and current will return everywhere on the ground plane. However, inductance coupling elements are not important in low frequency ranges, so our inductance extraction focuses solely on high frequency ranges, where current is congested in a small area close to signal wires on the ground plane.

B. Bundle Creation Technique

For inductance extraction, we adopt a loop-based inductance extraction methodology [5], [2] to reduce the final output netlist. We only consider wires in the same direction as wires located in orthogonal directions have zero mutual inductance. Since short wires will not create large current loops, and do not have large mutual inductance, we ignore any wires that are less than 30μm in our calculations. We then round all chip wires to 10μm in the target direction.

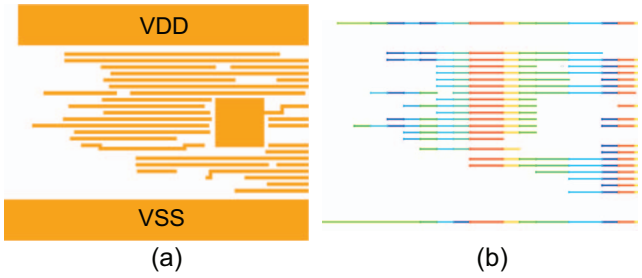

Fig. 5. (a) sample layout. (b) bundles created. Wires in each bundle share the same color.

One example of our bundle creation is shown in Figure 5(a), where the original layout is part of the FFT256 top layer. There are VDD and GND wires around several signal wires while the PDN wires are return paths for surrounding signals. After bundle creation, wires survived filtering are divided into segments, and multiple segments are grouped into a single bundle for further calculation. By using the bundle creation technique, the original 3D layout is divided into multiple bundles, and since the wire length is the same for all segments in each bundle, the layout is simplified into 2D configurations.

To create bundles, we use a search line from left to right scanning all terminal points of signal wires. These terminal points are propagated to neighbour wires, until no additional neighbour wires are found or the propagation reaches a return path. During terminal prorogation, this process creates new nodes on neighbour wires and partitions these wires into segments. All segments created by the same prorogated terminal point are grouped into a single bundle. The bundle creation results are shown in Figure 5(b).

C. Loop-based Inductance Calculation

After the bundle creation, we calculate the loop inductance for each bundle. We then divide all wires in the bundle into filaments so we can accurately determine the current density for each wire and model the skin effects and proximity effects.

Between any pair of wires, we calculate the partial inductance using the following equation [3]:

$$L_{l,k} = \frac{\mu_0 l}{2\pi}\left[\ln(\sqrt{k^2+1}+k) - \sqrt{k^{-2}+1} + \frac{0.9054}{k} + 0.25\right]. \quad (1)$$

For partial self inductance, $k = l/r$, where l is the length of the signal wire and r is the radius of the signal wire. For partial mutual inductance between a pair of parallel signal wires, we divide the total length into three parts: δ denotes the overlapping length between two wires, while m and n denote the non-overlapping length on each wire. We use the following equation to calculate partial mutual inductance:

$$M_{\delta,m,n,k} = (L_{\delta+m+n,k} + L_{\delta,k} - L_{\delta+m,k} - L_{\delta+n,k})/2. \quad (2)$$

Each sum term is calculated using (1), where $k = l/d$, and d is the center-to-center distance between two wires. After partial self inductance and mutual inductance are calculated, we divide the values into each bundles to calculate the loop inductance and resistance considering skin effects and proximity effects.

For a bundle with k signal wires, we search for all close-by return paths and then partition wires into a total of m filaments. We form a m-by-m partial impedance matrix **P** where P(i,i) is the partial self-impedance, and P(i,j) is the partial mutual impedance between

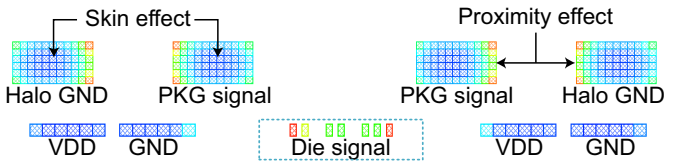

Fig. 6. Current density computation using our inductance extraction.

TABLE I
MULTI-THREADING ACCELERATION WITH TIME UNITS IN SECOND.

# Threads	1	2	4	8	12
Read GDS			2.0		
Create Bundle			0.15		
Compute	0.48	0.241	0.138	0.088	0.063
Speed Up	1X	1.99X	3.48X	5.45X	7.62X

filaments i and j. Only diagonal elements of **P**, have the real part, which is the DC resistance of the filament. We then form a column vector **u** with m rows of one, and an m-by-k mesh matrix **M**, where M(i,j) is 1 if i belongs to signal j, and 0 otherwise.

We solve two linear systems **Pa=u** and **PB=M** and normalize **a** to have a norm sum of 1. We use this unified vector to obtain the m-by-k current matrix **I**, whose j-th column vector I(j) is calculated from the j-th column of **B**:

$$I(j) = B(j) - \Sigma B(i,j) \times a, \text{where i=1..m.} \quad (3)$$

This current matrix can further be used to derive the current of each filament by performing a row-wise sum, shown in Figure 6. After the current is obtained, we calculate the k-by-k loop impendence matrix **Z** by: $Z = (M^T \times I)^{-1}$. We ignore the mutual resistance and only use the real part of the diagonal elements of **Z** as the AC resistance of each signal, and divide the imaginary part of **Z** by the angular frequency to obtain the loop inductance matrix. The total time complexity of our algorithm is O($N \times M^3$), where N is the number of bundles, and M is the average number of filaments in a bundle.

IV. Experiment Results

A. Performance and Accuracy

To test the performance, we implement the inductance tool using C++. We run our tool on an Intel XEON E5 server with 16 physical cores using the FFTx1 benchmark with 1528 interface wires after length filtering. The runtime analysis is shown in Table I. As results show, our method is extremely efficient and well-suited for full system-level P2D extraction by using ground plane approximation and bundle creation techniques. It also can be easily scaled so there is virtually no limit on the size of the layout it handles.

Since it is impossible to extract the full-chip with commercial tools, we select a few wires from the layout, create equivalent simulation structures and compare our results against the FastHenry inductance solver. Results are shown in Table II. Generally, our method is highly accurate on both loop resistance and self inductance with a small underestimation on mutual inductance since we ignore the inter-bundle mutual inductance. Further, though shorter wires (#3) tend to have larger errors on mutual inductance, because equation (1) is less accurate when l is not much larger than r, the impact on the full-chip level is small because the inductance is dominated by longer wires.

B. Full-System P2D Extraction

We run our inductance extraction engine on all benchmarks and obtain the inductance result. Part of the layout with inductance annotated is shown in Figure 7(a), with return paths located on the top and bottom of the signal channel. Total self and mutual inductance extraction results of the selected region are shown Figure 7(b) and (c), respectively. in Note that based on our loop inductance calculation. As results show, signals closer to the return paths have smaller loop inductance, as their current return loops are small. Also, signals with more neighbours have larger total mutual inductance extracted, as there is more coupling between current loops formed by these signals.

TABLE II
VERIFICATION AGAINST FASTHENRY ON R (IN Ω) AND LM (IN PH).

	Fast Henry			Our method					
#	R	TotL	TotM	R	ERR%	TotL	ERR%	TotM	ERR%
1	0.52	34.3	94.8	0.52	-0.7%	35.3	2.8%	89.8	-5.3%
2	0.52	34.5	109.2	0.52	-0.6%	35.5	2.9%	104.6	-4.3%
3	0.42	27.5	106.3	0.41	-1.3%	26.8	-2.6%	96.4	-9.4%
4	0.52	34.8	121.1	0.51	-0.6%	35.8	3.0%	116.5	-3.8%
5	0.52	34.8	120.9	0.51	-0.6%	35.9	3.0%	116.3	-3.8%

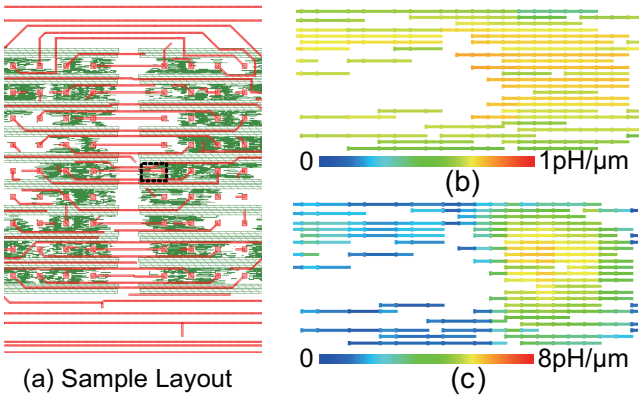

Fig. 7. P2D inductance extraction result on chip wires. (a) shows the layout with (b) self and (c) total P2D mutual inductance of the highlighted region.

V. Conclusion

In this paper, we performed a comprehensive study on P2D interface parasitic extraction with detailed signal integrity analysis. We observed that inductive coupling is the major portion of field interaction within P2D interface layers, and it contributes significantly to package-induced noises on chip wires. We proposed novel inductance extraction methodologies based on halo ground, bundle creation, and loop-inductance calculation. We showed that our methods are extremely fast and accurate against industry-standard tools. We demonstrated that P2D coupling is critical for accurate P2D co-design and signal integrity co-analysis.

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