Entropy Production-Based Full-Chip Fatigue Analysis: From Theory to Mobile Applications

Tianchen Wang, *Student Member, IEEE*, Sandeep Kumar Samal, *Member, IEEE*, Sung Kyu Lim, *Senior Member, IEEE*, and Yiyu Shi, *Senior Member, IEEE*

***Abstract*— Through-silicon vias (TSVs) are subject to thermal fatigue due to stress over time, no matter how small the stress is. Existing works on TSV fatigue all rely on measurement-based parameters to estimate the lifetime, and cannot consider detailed thermal profiles. In this paper, we propose a new method for TSV fatigue prediction using entropy production during thermal cycles, which is validated by theoretical analysis and measurement results. By combining thermodynamics and mechanics laws, the fatigue process can be quantitatively evaluated with detailed thermal profiles. Experimental results show that interestingly, the landing pad possesses the most easy-to-fail region, which generates up to 50% more entropy compared with the TSV body. The impact of landing pad dimension and TSV geometries are also studied, providing guidance for reliability enhancement. Full-chip fatigue analysis is performed based on stress superposition. Based on the developed theory, we study the interesting problem of fatigue lifetime of 3-D microprocessors in smartphones and its dependence on user task profile. Finally the lifetime of 3D IC TSV in smartphone is researched with selected apps and user profiles. To the best of the authors' knowledge, this is the first TSV fatigue model that is free of measurement data fitting, the first that is capable of considering detailed thermal profiles, and the first framework for efficient full-chip TSV fatigue analysis, and the first study on fatigue lifetime of mobile chips.**

***Index Terms*—3-D integrated circuit (IC), entropy, fatigue.**

I. Introduction

With the rapid growing requirements on the performance, speed, and power of integrated circuits, tremendous efforts have been made toward the successful development of the 3-D integrated circuit (3D IC). The higher performance and smaller footprint brought by 3D ICs has resulted in their wide adoption in mobile devices [1]. Guillou and Dutron [2] presented an industrial perspective of 3D ICs in smart phones, where better electrical performance is achieved by new partitioning and architectures, higher flexibility and better integration. However, the limited number of through-silicon-vias (TSVs), which serve as the main vertical channel for heat dissipation, along with the limited cooling capability in mobile platforms, still subject mobile devices to heavy thermal loadings. TSVs play an important role in 3D ICs as vertical signal and power interconnects, new vertical inductors [3]–[5] and facilitating heat transfer between different tiers.

Due to excessive thermal loading, all mobile devices have limited lifetime restricted by thermal failures. Specifically, in 3D ICs, the mismatch of coefficients of thermal expansion (CTE) between copper, silicon dioxide, and silicon leads to thermo-mechanical stress and strain at the interfaces. If the stress applied on a material is higher than its yield strength, it will start plastic deformation. Various literature have thus studied the algorithms to capture stress hotspots in a 3D IC (e.g., [6]). A less known and studied problem, on the other hand, is the thermal fatigue when the stress is below yield strength. With cyclic thermal loading, the stress and strain will cause elastic deformation, accumulating fatigue over time. Such fatigue will result in interfacial cracks between liner, substrate, landing pad, and TSV body, as shown in Fig. 1. The electrical characteristics of TSVs (the mutual capacitance between the TSVs) are reported largely effected after only 1000 cycles of thermal shock test due to crack [7]. Okoro *et al.* [8] found that the electrical resistance of TSV daisy chains increase with the number of thermal cycles due to thermally induced damage leading to the formation and growth of defects. Moreover based on FIB-SEM and TEM results, six different damage types were observed in the TSV daisy chain: sidewall cracks, TSV voids, M1 oxidation, TSV-M1 interface cracks, TSV-bottom metallization crack, and cracks at the bottom metallization-damascene silicon dioxide interface. Under accelerated thermal cycle loading, the lifetime of TSVs can be as short as 500 cycles [9]. Therefore, it is essential to understand and investigate the mechanics of TSV fatigue and optimize chip designs for better performance, reliability and robustness.

Many works exist in literature on TSV fatigue, ranging from thermal-mechanical fatigue cracking mechanisms to the related optimization in various aspects. By using a representative fabricated silicon interposer test chip, Banijamali *et al.* [11] investigated the effect of TSV interposer subjected to thermal cycles on the stress of the die and low-k layers in 3-D thermo-mechanical modeling and simulation. In [12], the nonlinear stresses and strains in the microbumps between the silicon chip

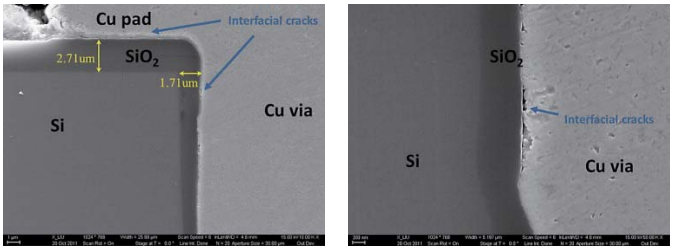
Manuscript received February 24, 2017; revised May 18, 2017, July 26, 2017, and November 5, 2017; accepted January 10, 2018. Date of publication February 7, 2018; date of current version December 19, 2018. This paper was recommended by Associate Editor Y. Cao. *(Corresponding author: Tianchen Wang.)*

T. Wang and Y. Shi are with the Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, IN 46556 USA (e-mail: twang9@nd.edu; yshi4@nd.edu).

S. K. Samal and S. K. Lim are with the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: sandeep.samal@gatech.edu; limsk@ece.gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCAD.2018.2803623



(a) (b)

Fig. 1. SEM images of interfacial cracks (a) under Cu pad and (b) on the TSV side wall [10].

and copper filled TSV interposer have been determined for a wide-range of via sizes and pitches, and various temperature conditions. The study claimed to be helpful to decide if underfill is necessary for the reliability of microbumps and selecting underfill materials to minimize the stresses and strains in the microbumps. Auersperg *et al.* [13] investigated the copper properties in TSV during back end of line (BEoL)-built-up by extracting coefficients from nanoIndentation experiments, which are used accordingly to investigate the pumping and protrusion of copper-TSVs during thermal cycling. The cracking and delamination risks caused by the elevated temperature variation during BEoL ILD deposition is investigated. Frank *et al.* [14] focused on researching the influence of reliability in different TSV process sequences: TSV-last and TSV-middle. The concerns of thermal cycle, electromigration, and impact of TSV on adjacent BEoL dielectric reliability are addressed in experimental analysis. Zeng *et al.* [15] studied on the thermo-mechanical reliability of a 3D-TSV MEMS in which cap layer and MEMS micro-structure layer is vertically interconnected and bonded by TSVs/micro-bumps and a seal ring. The feasibility of the 3D TSV MEMS is also verified with quarter circular arc implemented in optimized structure.

However, all these works on TSV thermal fatigue are mainly based on the Coffin-Manson model, the details of which will be discussed in Section II-B. For example, Choa *et al.* [16] studied the durability of TSV using the model by analyzing the plastic strain due to repetitive temperature cycling and investigated the impact of TSV design parameters. Ladani [17] applied the model in the reliability analysis of TSVs and solder joints as well as in the impact study of underfill thickness and stiffness. A few limitations exist for the Coffin-Mason model and thus all these methods. They require measurement data fitting, and cannot consider any thermal profile details during thermal cycling.

In this paper, we propose a novel model based on entropy production, which does not need any measurement data fitting, to quantitatively predict TSV fatigue during thermal cycles. The model takes detailed transient thermal profile into consideration. In addition, we show that the classic Coffin-Manson fatigue model can be deduced from our model. We also validate our model against measurement data which clearly indicates that our model can yield much more accurate estimation than Coffin-Manson method. We then further study the impact of TSV structures and locations on fatigue using our model. An efficient framework for full-chip fatigue analysis based on stress superposition is presented as well. Finally, we applied the framework to smartphone applications and investigate how different user profiles (usage of apps) can affect fatigue lifetime.

The main contribution of our paper is that we have proposed: 1) the first TSV fatigue model that is free of measurement data fitting, and the first capable of considering detailed thermal profiles; 2) a few interesting observations on the impact of TSV structures and locations on fatigue; 3) the first framework for full-chip TSV fatigue analysis. This method will help designers to fully understand the weakest points in 3D IC structures subject to thermal fatigue; and 4) the first exploration of the impact of mobile apps on fatigue lifetime.

The remainder of this paper is organized as follows. Section II reviews two models for mechanical reliability and thermal fatigue analysis, with their shortcomings. Section III theoretically introduces the novel entropy production fatigue analysis and measurement data-based validation. Section IV investigates the impact of TSV structures and locations, and Section V presents the full-chip TSV fatigue analysis framework. Section VI applies the framework to smartphone applications and investigate how different user profiles can affect fatigue lifetime. Concluding remarks are given in Section VII.

II. Preliminaries

A. Von Mises Stress Criterion

When stress exceeds the yield strength, materials start to experience irreversible plastic deformation. The von Mises yield criterion is most widely used to determine whether an isotropic and ductile metal will yield when it is subject to a complex loading condition [18].

The von Mises stress is derived from stress tensor, a combination of normal and shear stresses that has nine components and completely describes the state of a stress applied on an object at a point. The equation of stress tensor is shown in (1) and the related von Mises stress is shown in (2). The indices (i, j) in (2) refer to the normal and tangential directions of the stress, respectively. When i equals j, σ_{ij} is called normal stress and when i does not equal j, σ_{ij} is called shear stress

$$\sigma = \sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix} \tag{1}$$

$$\sigma_v = \left[\frac{1}{2}(\sigma_{xx} - \sigma_{yy})^2 + \frac{1}{2}(\sigma_{yy} - \sigma_{zz})^2 + \frac{1}{2}(\sigma_{zz} - \sigma_{xx})^2 + 3\left(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{xz}^2\right) \right]^{\frac{1}{2}}. \tag{2}$$

The von Mises criterion only shows whether a material starts plastic deformation during operation at a specific time. Therefore, stress analysis does not apply to long-term material fatigue prediction (especially when the stress does not exceed the yield strength).

B. Existing Fatigue Models

Researchers have attempted to quantify material fatigue under various circumstances for many years. Miner *et al.* [19]

proposed the first idea about quantifying the fatigue damage under the assumption that the life fractions of individual amplitudes sum up to unity. From then on, various models for fatigue lifetime prediction were developed on different variables such as strain, stress, energy, damage, temperature, frequency, etc. Among them, the Coffin-Manson model is the most widely used one, which is based on plastic strain. Depending on the strain amplitude ($\Delta\varepsilon$), the total number of cycles to failure (N_f) is depicted, with the empirical constants (C and n) that are adopted for various materials by specific measurement data fitting. The equation is shown in

$$N_f = C\left(\frac{\Delta\varepsilon}{2}\right)^n. \tag{3}$$

Two significant limitations exist this model. First, they rely on measurement data, which are valid only under specific environmental conditions such as thermal shock and thermal cycles, to fit various parameters. As such, the fitted parameters are not suitable for all the complex conditions. Second, they only consider the effects of maximum temperature, temperature change, and cycling frequency, and are thus semi-empirical. For example, they cannot tell the difference between temperature cycle and thermal shock, where the ramp rate is the key difference. Thermal shock has much higher ramp rate, and results in more damage [20].

In this paper, we will propose a new model for TSV fatigue analysis that addresses both issues.

III. Entropy Production Modeling

A. Concept of Modeling

The theory of fatigue prediction using entropy production is developed based on the degradation-entropy generation theorem. According to the second law of the thermodynamics, entropy is generated when the permanent degradation is presented through an irreversible process, which leads to a monotonic increase of disorder in a system. Therefore, the component of material degradation can be measured by entropy and thermodynamics energy [21], [22].

As for experimental validation, Naderi *et al.* [23] validated the sufficient and necessary condition for the entropy production of a metal which takes cyclic loading before reaching the final fracture. In the experiment, it is observed that the metal specimen breaks during operation when its entropy production through thermal deformation cycles reaches a critical value. The behavior is independent of the loading type, the size and the geometry of the specimen. Furthermore, by applying the entropy degradation theory related thermodynamic forces, Amiri *et al.* [24] experimentally determined the critical damage value of specimens subjected to different operations based on the entropy flow. However, this method has only been applied to large scale analysis (in scale of meters), not to micro structure.

In this paper, we propose the concept of entropy generation in the context of 3D IC fatigue, especially TSVs. Based on previous theories, when expressing the fact that the volumetric entropy production is positive, the Clausius-Duhem inequality (second law of thermodynamics) can be used a

$$\dot{\gamma}(t) = \sigma(t) : \frac{\dot{\varepsilon_p}(t)}{T(t)} - J_q\frac{\mathrm{grad}T(t)}{T^2(t)} \geq 0 \tag{4}$$

where J_q is the heat flux through the boundary, $\sigma(t)$ is the symmetric stress tensor, $\dot{\gamma}(t)$ is the entropy production, $\dot{\varepsilon_p}(t)$ is the strain rate, and $\sigma(t) : \dot{\varepsilon_p}(t) = \sigma_{ij}(t)\dot{\varepsilon}_{p(ij)}(t)$ is the tensor multiplication.

The heat flow and the work within an arbitrary control volume contribute to the total energy of a system, which describes the conservation of energy in thermodynamics. By introducing temperature and total strain, the coupling of thermodynamics and continuum mechanics can lead to an energy balance as shown in (5), made by heat conduction ($k\nabla^2 T(t)$), thermal inertia retardation effect ($\rho C\dot{T}$), internal heat generation through plastic deformation ($\sigma(t) : \dot{\varepsilon_p}(t)$) and thermo-elastic coupling ($T(t)\partial\sigma/\partial T(t) : \dot{\varepsilon_e}(t)$)

$$k\nabla^2 T(t) = \rho C\dot{T} - \sigma(t) : \dot{\varepsilon_p}(t) - \frac{T(t)\partial\sigma}{\partial T(t)} : \dot{\varepsilon_e}(t). \tag{5}$$

Then the entropy production during a certain period of time (γ_c) can be obtained by combining (4) and (5) with time integration, shown in (6), where $W(t)$ means the work done by deformation

$$\gamma_c = \int_0^t \left(\frac{W(t)}{T(t)} - \frac{J_q \cdot \mathrm{grad}T(t)}{T^2(t)}\right)\mathrm{d}t. \tag{6}$$

Subsequently, the material fatigue status of TSV is obtained based on entropy production. Therefore, if we have the inputs of thermal profile($T(t)$), heat flux(J_q), work done by deformation ($W(t)$), and time(t), the entropy production could be generated. A larger entropy production means shorter lifetime due to fatigue. Apparently, the above model does not have any parameter that needs to be fitted, and considers the detailed thermal profile $T(t)$.

To conclude, comparisons between the von Mises stress, the Coffin-Manson model and our entropy production model are summarized in Table I.

TABLE I
Comparisons Between the Von Mises Stress, the Coffin-Manson Model and the Entropy Production Model

	Von Mises stress	Coffin-Manson model	Entropy production
Fatigue life prediction		√	√
Consider detailed thermal profiles	√		√
No measurement data needed	√		√
Stress analysis	√		
Fatigue analysis		√	√

B. Relationship to Coffin-Manson Model

To partially validate our entropy production model, we will show in this section that the widely used Coffin-Manson model [i.e., (3)] can be deduced from (6) by making reasonable assumptions.

As the Coffin-Manson model applies the condition that plastic deformation dominates the fatigue of a material, we only consider the entropy production due to plastic deformation. First, we introduce the model from Morrow [25], in which the plastic strain energy per cycle keeps approximately constant during the fully reversed experimental fatigue tests. The related equation is

$$\Delta w_p = \frac{4\sigma_f'\left(\frac{1-n'}{1+n'}\right)}{\varepsilon_f'}\left(\frac{\Delta\varepsilon_p}{2}\right)^{1+n'}. \tag{7}$$

Assuming that we are dealing with low-cycle fatigue in small volume with heat conduction neglected, (6) leads to

$$\gamma_f = \int_0^t \left(\frac{f(t)\Delta w_p}{T(t)}\right) \mathrm{d}t \tag{8}$$

where $f(t)$ is the fraction of work done by plastic deformation during thermal cycles.

Then, by assuming the plastic energy dissipation Δw_p and the temperature $T(t)$ are constants throughout the thermal cycles, (8) leads to

$$\gamma_f = \frac{\Delta w_p}{T} N_f. \tag{9}$$

Therefore, the number of cycles to failure N_f is obtained by employing (7), which is

$$N_f = \frac{T\gamma_f(\varepsilon_f')^{n'}}{4\sigma_f'\left(\frac{1-n'}{1+n'}\right)}\left(\frac{\Delta\varepsilon_p}{2}\right)^{-(1+n')}. \tag{10}$$

Compared with Coffin-Mason model, we get

$$c = -\frac{1}{1+n'}, \varepsilon_f' = \left(\frac{2\sigma_f'\left(\frac{1-n'}{1+n'}\right)}{T\gamma_f\left(\varepsilon_f'\right)^{n'}}\right)^{-\frac{1}{1+n'}}. \tag{11}$$

This leads to the conclusion that Coffin-Manson model is a special case of our entropy generation model under specific assumptions and simplifications, which partially validates the correctness of our model. In the future, we will validate our model directly with measurement data.

C. Experimental Validation of Entropy Production

In the previous section, we have demonstrate that our entropy production method is more generalized than Coffin-Manson model. To validate it experimentally, we use the via chain test structures, which form part of 3D ICs [26] with measurement data for silicon correlation. As shown in Fig. 2(a), the stacked via chadin structure is made of two SiLK levels and two SiO_2 levels stacked on the top, with three metal levels (MC, M1, and M2) connected by two levels of vias (V1 and V2). In the experiment, the chain has 50 links repeatedly, alternating between M2 and MC, which are local interconnects linking to other stacks. Therefore, this unsymmetrical structure would lead to a nonhomogeneous stress on vias. In Fig. 2(b), the SEM cross section view clearly shows the typical fail at the stress condition of certain thermal cycles, which occurs along the (111) plane.

To model the via structure, the geometry of the structures applied in the experimental test were adopted from [27]. The entropy production result of the via with cross section view is shown in Fig. 2(c). The normalized value is calculated from (6). The highest entropy production occurs on upper-left and bottom-right corners, leading to the crack shears through the entire via. The nonsymmetrical crack is due to the stacked via test structure with a nonsymmetrical configuration. This result agrees well with the crack plane in Fig. 2(b), showing a precise fatigue prediction of the entropy production method.

To compare entropy production with Coffin-Manson prediction, three different thermal profiles are used. The parameters of Coffin-Manson equation vary due to various experimental environments [16], [28], [29] and yield multiple results. The resulting cycles to failure from measurement, entropy production and Coffin-Manson equation are shown in Fig. 2(d). ΔT means the temperature difference in thermal cycles, while cycles to failure in y-axis is in log scale. Note that the measurement data uses N_{50} median number extracted from the chart, and the entropy production prediction is determined based on the threshold obtained at 215 °C.

As shown in the figure, the curves of Coffin-Manson exhibit a large range of uncertainties (cycles to failure) with various parameter values. In practical application, it is hard to decide which parameter values should be used, which depend on specific working environment. On the other hand, entropy production does not have uncertainties problem since it only depends on the type of material, which provides a very close estimation to the measurements.

IV. Simulation and Analysis

A. Impact of Thermal Cycles

In this section, TSV cells are modeled in Abaqus to calculate the entropy production of TSV for fatigue prediction. For the first part of the simulation, a single TSV cell with a copper TSV body and two landing pads attached is built as shown in Fig. 3(a) and (b). Unless specified, the geometries are the same as in [18]. The parameters of materials applied are listed in Table II. In this model, we have simplified the bottom part of the TSV by ignoring the solder joint attached. The top part is modeled accurately for fatigue analysis. The interfaces between different parts are assumed to be perfectly adhesive. The thermal cycles range from 20 °C to 70 °C, as shown in Fig. 3(c). Note that this temperature profile is derived from actual operating conditions of a chip.

It needs to be clarified that since entropy production has only been experimentally proved on metals, our fatigue analysis only focuses on the TSV body and the attached landing pad. In other words, it is limited to copper. In addition, in all the figures afterwards, we use a single color bar for all the parts in the same figure for better comparison.

We simulate the TSV structure for five thermal cycles. It takes about 20 h of computation with a cluster of 60 nodes, each has 256 GB memory and 12 cores, 2.4 GHz CPU frequency. The high computation time is due to the denser mesh structure for higher accuracy. The resulting entropy production distributions on the top and bottom surfaces of the

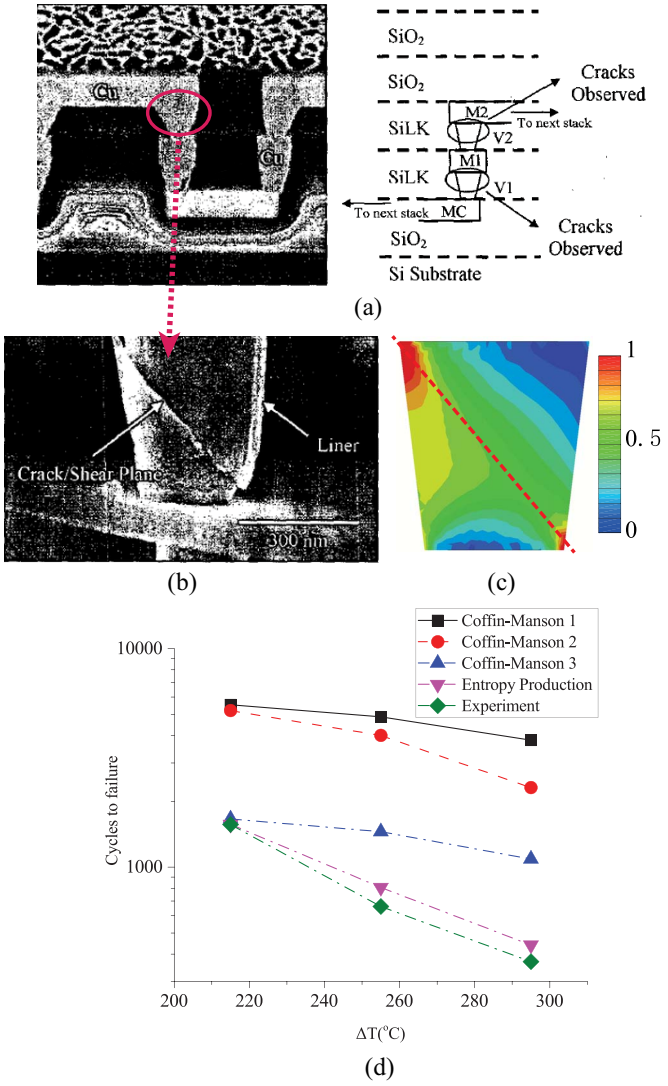


Fig. 2. (a) SEM micrograph (left, with labels removed) and schematic cross section (right) of stacked via structure [26]. (b) SEM image showing shearing and cracking in via after thermal cycles. (c) Cross-sectional view of via in entropy production modeling (normalized). (d) Cycles to failure of experiment test, entropy production and Coffin-Manson prediction.

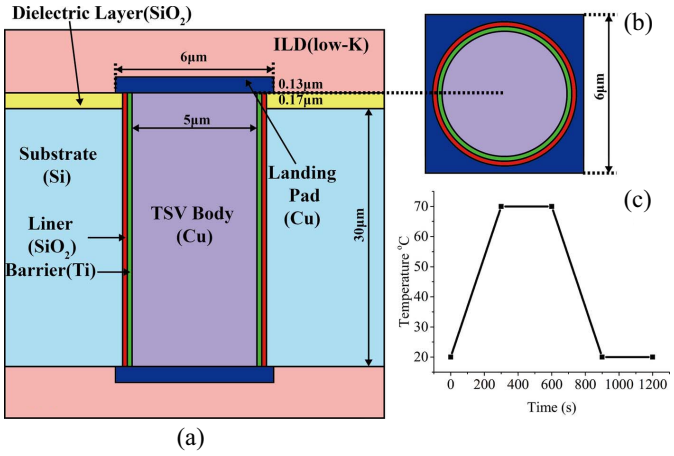


Fig. 3. Illustration of (a) side view and (b) top view of the TSV structure, and the (c) profile of a thermal cycle.

TABLE II
MATERIAL PROPERTIES

Material	CTE (ppm/K)	Young's Modulus(GPa)	Poisson's ratio
Cu	17	110	0.35
Si	2.3	130	0.28
SiO_2	0.5	71	0.16
Low K	20	9.5	0.3
BCB	40	3	0.34
Ti	8.6	116	0.32

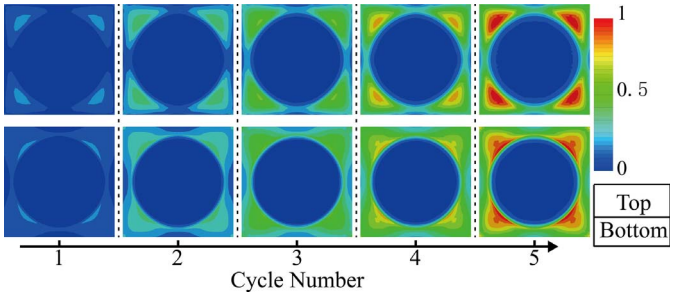


Fig. 4. Entropy production distributions on the top and bottom surfaces of the landing pad through five thermal cycles (normalized).

landing pad attached to the top surface of the TSV are shown in Fig. 4. It is clear that after five thermal cycles, the entropy production at the four corners of the landing pad increases much faster than that at the center. The reason is that the expansion and contraction of the TSV body has little axial effect on the attached area between the TSV body and the landing pad, since they have the same CTE. However, the corners of the landing pad located between the dielectric layer and ILD have larger moments during deformation, thus leading to higher entropy production.

The results of the TSV body are shown in Fig. 5, with its inner surface, outer surface and top surface displayed. After the thermal cycles, the outer edge of the top surface has the maximum entropy production. This is again due to the CTE mismatch between the TSV body and the barrier, which causes large stress and strain on the top interface. In addition, the minimum entropy production area can be found in the middle part of the top surface, as it is attached to the landing pad with the same CTE. Finally, due to the radial effect of stress, the entropy production also concentrates in the middle of the TSV body, which increases at about 50% higher rate than the neighboring parts. This suggests that the middle part of a TSV body can be a new reliability concern in the presence of fatigue.

In the simulations, we also discover that the rate of entropy production increase in the landing pad and the TSV body through cycles remain the same. Thus, single cycle modeling is sufficient for TSV fatigue analysis using entropy production, which will be used in the remaining of the paper.

We summarize the important findings from the above study as follows.

Observation 1: Landing pads have maximum entropy production located at corners.

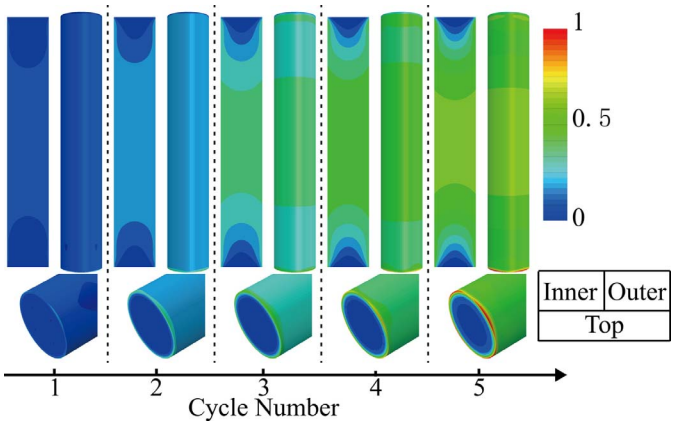


Fig. 5. Entropy production distributions on the inner surface, outer surface, and top surface of the TSV body through five thermal cycles (normalized).

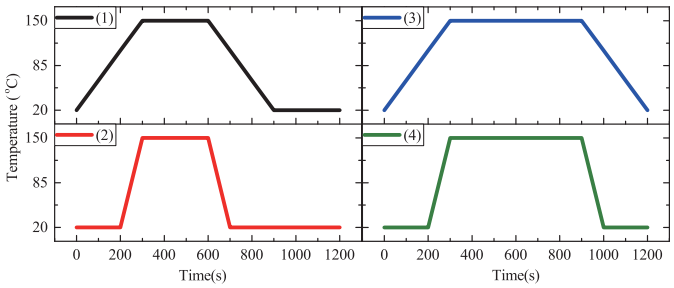


Fig. 6. Four groups of thermal profiles for validation, with the same temperature range, cycle time, different rate of temperature change, and different distribution.

Observation 2: The middle part of a TSV body shows concentrated entropy production, leading to a new reliability concern.

As illustrated in the previous section, the Coffin-Manson method only considers the maximum strain amplitude during the thermal cycles and does not consider the rate of temperature change. On the other hand, our entropy production method can take that into consideration. To show the difference, the TSV models with four different thermal profiles are built for comparison, as shown in Fig. 6. The four thermal profiles have the same cycle time (1200 s) and temperature range (20 °C to 150 °C), leading to the same Coffin-Manson fatigue prediction results. The difference between the four durations is the rate of temperature change and distribution. Groups 1 and 2, 3 and 4 have the same high temperature duration, while groups 1 and 3, 2 and 4 have the same rates of temperature change.

The results are shown in Table III, which clearly illustrate that the duration of high temperature does not influence the fatigue, while the rate of temperature change does. It is observed that the results of groups 2 and 4 with a higher temperature change rate have higher entropy production, in both landing pad and TSV body. This is caused by the nonlinear increasing of entropy production in plastic deformation at high stress. The higher temperature change rate, the higher entropy production leading to easier fatigue of material. Therefore, the entropy production fatigue method is applicable in the fatigue analysis considering the details of thermal cycles.

TABLE III
ENTROPY PRODUCTION OF TSV BODY AND LANDING PAD WITH DIFFERENT THERMAL PROFILES

Thermal Profile Groups		1	2	3	4
Landing Pad	Max Entropy	45.4	46.6	45.4	46.6
TSV Body	Production($\times 10^8$J/m^{3}K)	28.0	28.9	28.0	28.9

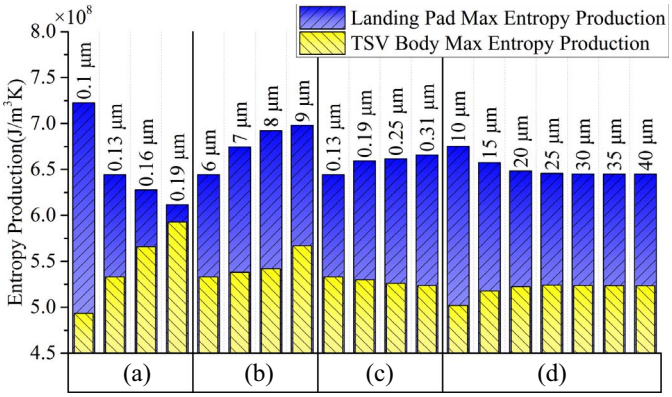


Fig. 7. Maximum entropy production values of the landing pad and the TSV body, with various (a) thickness and (b) width of the landing pad, (c) thickness of the liner, and (d) length of the TSV body.

B. Impact of TSV Structure Parameters

In this section, we study the impact of TSV structure parameters on the entropy production in a single TSV cell, hoping to establish guidelines for reliability optimization. We only focus on the maximum entropy production values of the TSV body and the landing pad, respectively, which provide information about the most dangerous areas.

The results of entropy production of the landing pad and the TSV body with different thickness and width of the landing pad, thickness of the liner and length of the TSV body are shown in Fig. 7.

First of all, from Fig. 7 we can first see that in all the cases, the landing pad always has a much higher maximum entropy production compared with the TSV body. This is because the landing pad takes stress from TSV body during expansion and reduction, which causes higher strain rate that leads to higher maximum entropy production. For example, when the landing pad thickness is 0.1 μm, the maximum entropy production of the landing pad is approximately 50% higher than that of the TSV body.

Observation 3: More attention should be paid to the landing pad than the TSV body in terms of thermal fatigue during TSV cell designs.

In addition, from Fig. 7(a) we can see that when the thickness of the landing pad increases, the maximum entropy production value of the landing pad decreases while that of the TSV body increases. This is because with the increase of thickness the landing pad gets stronger to hold against the deformation from the TSV body along the axial direction. As such, the strain rate gets smaller and the entropy production becomes smaller. As for the TSV body, a stronger landing pad leads to more stress on the surface, resulting in higher entropy production.

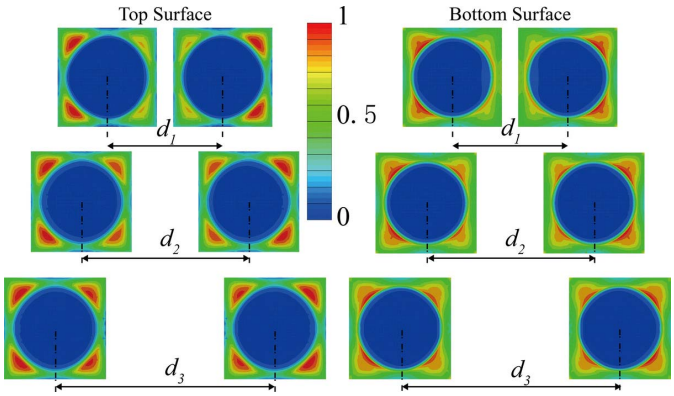


Fig. 8. Entropy production distribution on the top and bottom surfaces of the landing pads in a TSV pair ($d_1 = 7$ μm, $d_2 = 10$ μm, $d_3 = 13$ μm, normalized).

Observation 4: Increasing the thickness of the landing pad is helpful for the landing pad to reduce fatigue, but harmful for the TSV body.

Moreover, from Fig. 7(b) we can see that as the width of the landing pad increases from 6 μm to 9 μm, the maximum entropy production values of both the landing pad and the TSV body increase. For the landing pad, this is because a wider landing pad introduces larger strain rate due to longer distance. For the TSV body, the stress acted on it remains the same while the strain rate increases. Therefore, increasing the width of the landing pad is not preferred for fatigue reduction.

Observation 5: Increasing the width of the landing pad is harmful for both the landing pad and the TSV body.

Furthermore, from Fig. 7(c) we can see that as the thickness of the liner increases, the maximum entropy production value of the landing pad increases while that of the TSV body decreases, with very small differences. This is because the liner is made of silicon dioxide, which has a much lower CTE than copper. When the liner thickness increases, a more rigid wall is built around the TSV body, which holds against the landing pad. This causes the landing pad harder to deform, thus an increased stress on the interface between the liner and the landing pad. For the TSV body, the outer edge of the top surface has less strain rate than before, which leads to a slightly decreased maximum entropy production value.

Observation 6: The thickness of the liner has limited impact on the fatigue of both the landing pad and the TSV body.

Finally, from Fig. 7(d) we can see that when the length of the TSV body is below 20 μm or aspect ratio 4:1, the maximum entropy production value of the landing pad decreases and that of the TSV body increases with the increase of the TSV body length. Both stop changing afterwards. This is because when the TSV body is long enough, the stress from expansion and contraction along the axial direction at the top surface does not change any more.

Observation 7: Aspect ratio of the TSV body only matters when it is small. In such scenarios, increasing the aspect ratio is helpful for the landing pad to reduce fatigue, but harmful for the TSV body.

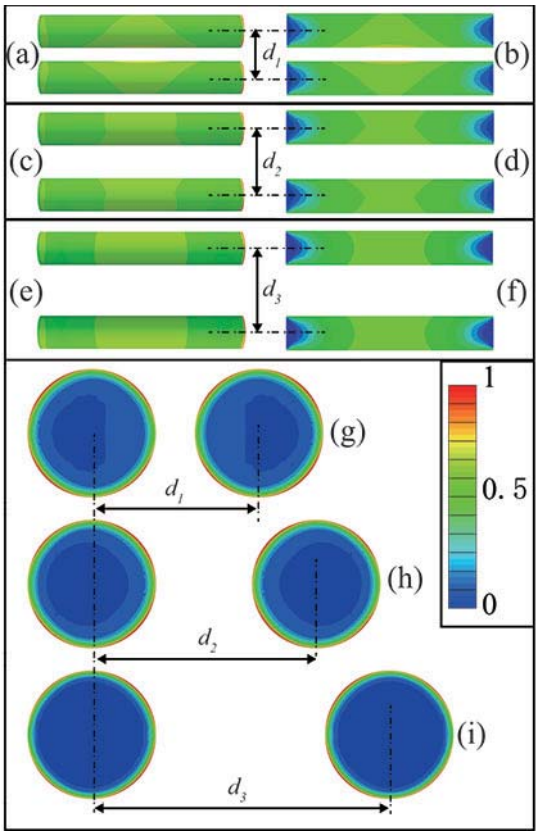


Fig. 9. Entropy production distribution on the (a), (c), (e) outer surface, (b), (d), (f) inner surface and (g), (h), (i) top surface of the TSV body in a TSV pair ($d_1 = 7$ μm, $d_2 = 10$ μm, $d_3 = 13$ μm, normalized).

C. Impact of the Pitch in TSV Pair

In this section, we study the impact of the pitch in a TSV pair. The entropy production distributions on the landing pads with different pitches are shown in Fig. 8. From the figure, it is clear that the pitch affects the entropy production on both surfaces of the landing pad. When the TSVs get closer, the two inner corners on each landing pad have lower entropy production. This difference is caused by the silicon between the two TSVs. Small volume has less restricted power and since copper has a much higher CTE, the stress applied on the inner sides would decrease. Meanwhile on the contrary, the outer sides of both landing pads would be subject to more stress from the TSV body, leading to a higher entropy production.

The corresponding entropy production distributions on the inner surface, outer surface and top surface of the TSV body are shown in Fig. 9. From the figure we can tell that when the TSVs get closer, there is an easy-to-fail area in the middle part of the TSV body. Unlike the landing pad, the area closer to the other TSV body shows a higher entropy production. However, when the pitch increases, the distribution of entropy production becomes uniform, which is similar as the result of the single TSV model. TSVs with small pitch will affect each other and generate more entropy at the neighbor sides, both at inner surface and outer surface of TSV body. The top surface of the TSV also shows the trend that the smaller pitch, the larger entropy production.

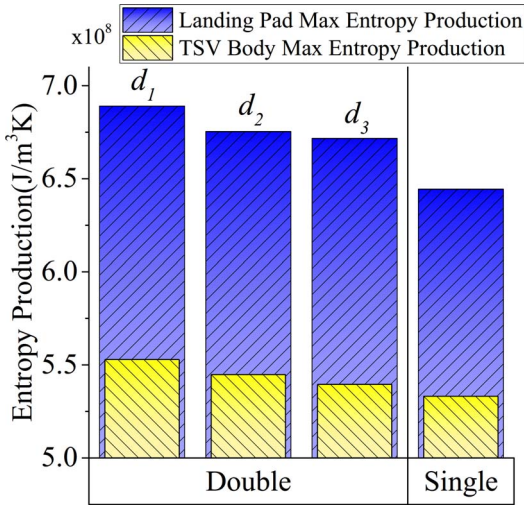


Fig. 10. Maximum entropy production of the landing pad and the TSV body, with various pitches (d_1 = 7 μm, d_2 = 10 μm, and d_3 = 13 μm).

Finally, Fig. 10 presents the maximum entropy production value of both the landing pad and the TSV body for various pitches. From the figure we can see that with the increase of the pitch, the maximum entropy production value of both the landing pad and the TSV body reduces.

Observation 8: Increasing the TSV pitch is helpful for both the landing pad and the TSV body to reduce fatigue.

D. Impact of Landing Pad Orientation in Arrays

The entropy production distribution depends on the configuration of TSV arrays. The TSV fatigue with various TSV array configurations while retaining the same TSV density has been studied by [30].

However, the impact of TSV array configuration on landing pad fatigue has not been investigated before. As the previous section shows, the landing pad always has a higher entropy production compared with TSV body during thermal cycles. Accordingly, it should attract more attention on fatigue reduction/prevention. To study the impact, two arrays with different landing pad orientations (0° and 45°) are modeled for comparison, as shown in Fig. 11(a) and (b). We further vary the TSV pitch in each topology from 10 μm to 20 μm. The angles of the landing pad in two groups have a difference of 45°. Models with various pitch sizes are built for comparison.

The results are shown in Fig. 11(c) with five different pitch size groups. It is observed that the maximum entropy production of landing pad is higher than that of TSV body, same as before. The larger pitch size results in lower entropy production for both TSV body and landing pad. In most cases, the entropy productions of TSV body and landing pad in group (b) is lower than those in group (a). Accordingly, the TSV layout with landing pad orientation as Fig. 11(b) is preferred. The only exception is the TSV body entropy production when the pitch size is 10 μm and the distance between two landing pads is 1.5 μm. This is caused by the close interaction between each landing pad, which yields a high stress effect on other TSV bodies. Therefore, the fatigue tradeoff between

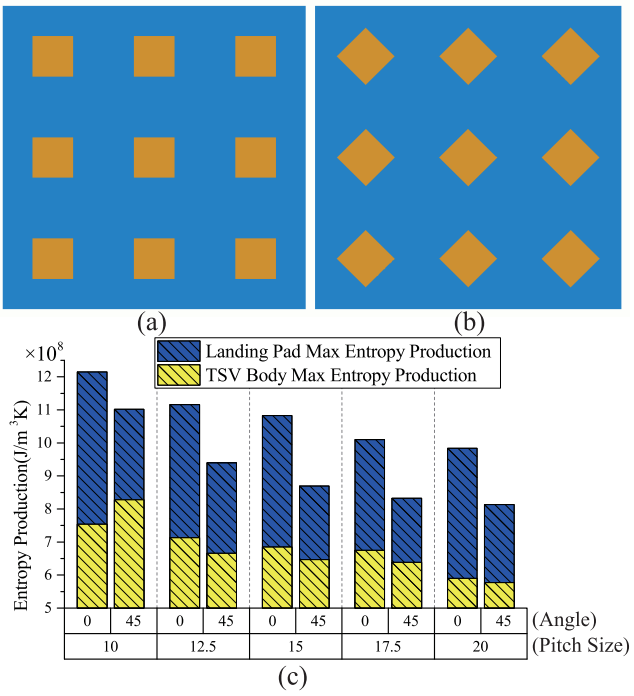


Fig. 11. Two landing pad orientations of TSV arrays with (a) 0°, (b) 45°, and the (c) corresponding results.

landing pad and TSV body needs to be made when TSV pitch is small enough.

V. Full Chip Analysis

FEA analysis of TSV fatigue using entropy production for a single TSV and a TSV pair has been investigated in the previous section. However, FEA is limited to small scale simulation due to the computational complexity. Therefore, it is necessary to develop a fast and accurate framework to analyze the fatigue of TSVs at full-chip scale. Superposition is the best approach in this context, but unfortunately, the entropy production as can be seen from (6) is nonlinear and cannot be superposed. Accordingly, we propose to use stress tensor superposition to achieve this target. The validity of stress tensor superposition has been verified in [18]. With the full-chip stress obtained from superposition, the strain can be obtained by fitting Hooke's law and the strain-stress curve of copper. The entropy production can then be readily derived.

To validate the correctness of our framework, the layout of a TSV pair is simulated by both FEA and our framework, with results shown in Fig. 12. Note that the landing pads are not included in the analysis. Our solution is to roughly estimate the hotspots from the full-chip analysis first, and then zoom in with landing pad included. It can be clearly seen that the patterns from both exactly match. The meshes in Fig. 12(b) is the computation grid used to perform the superposition of stress.

Before applying our framework to full-chip analysis, we apply two TSV placement styles in a small scale on the same design with the same TSV cell size. Multiple TSVs are placed

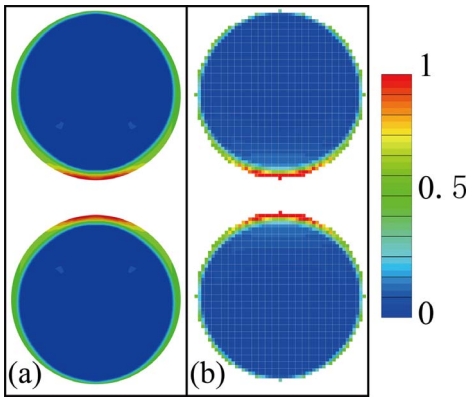


Fig. 12. Entropy production distributions on the top surfaces of a TSV pair using (a) FEA and (b) our framework (normalized).

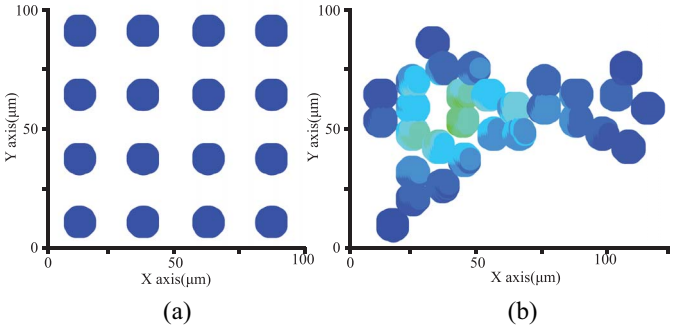


Fig. 13. Entropy production distributions of small scale TSVs in (a) regular and (b) irregular layouts (normalized).

in a chip area of 100 μm $\times$ 100 μm for regular placement, and 125 μm $\times$ 100 μm for irregular placement. In the regular placement the TSVs are uniformly placed with 25 μm pitch as shown in Fig. 13(a). The irregular placement, as shown in Fig. 13(b), results in shorter wire length. Comparing the two maps, the irregular TSV placement results in 6.5$\times$ higher maximum entropy production during thermal cycles. In addition, in the irregular placement, the hotspots are mainly located at places where the TSVs have small pitches. Meanwhile in the regular placement with larger pitches, almost identical entropy production occurs at each TSV. It can be concluded that TSV placement needs to consider the tradeoff between wire length and TSV fatigue.

Now we are ready to apply our framework to full-chip analysis to further verify the previous conclusion. As similar in previous smaller scale experiment, a total of 1472 TSVs are placed in a chip area of 1 mm $\times$ 1 mm. In the regular placement the TSVs are uniformly placed with 25 μm pitch as shown in Fig. 14(a). The irregular placement, as shown in Fig. 14(b), results in shorter wire length. The minimum TSV pitch is 20 μm. Comparing the two full-chip maps, the irregular TSV placement results in 17.3$\times$ higher maximum entropy production during thermal cycles, and the TSVs in regular placement lead to almost identical entropy production. Therefore the conclusion from small scale experiments can be successfully verified.

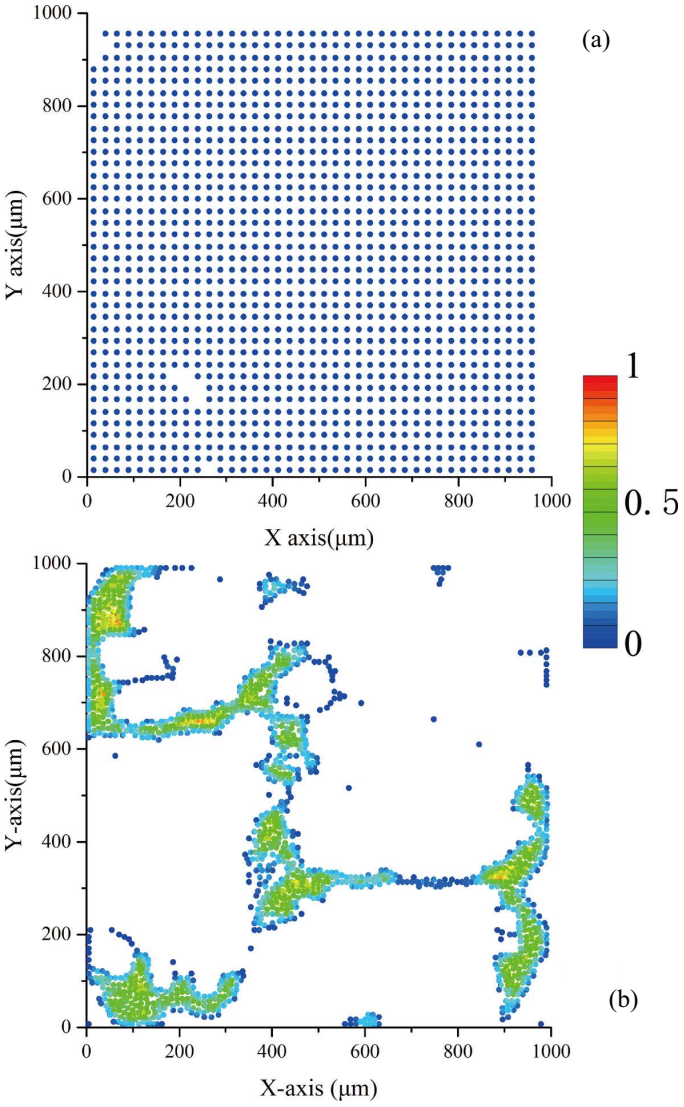


Fig. 14. Entropy production distributions of full-chip TSVs in (a) regular and (b) irregular layouts (normalized).

VI. Application to Smartphones

3D IC brings more computational potential to smartphones, which meet the requirement of large and complicated applications on mobile devices and the small footprint budget. On the other hand, compared with PCs or other large hardware platforms, limited cooling capabilities in smartphones make thermal stress a prominent issue. Interestingly, little prior work has been reported on the thermal fatigue in mobile platforms. Therefore, we choose smartphone as a vehicle to demonstrate the impact of our framework.

To build the experiment, the power consumptions of seven apps in an ASUS Android smartphone are selected and profiled: mobile advanced driver assistant system (ADAS) [31], Google Maps, YouTube, Chrome, Gmail, and two games, Pokemon Go and Fruit Ninja [32]. The apps are selected based on their high popularity among users. Note that the different user input when the apps are running (for example, when Google Maps are calculating different routes based on two different destinations) will generate slightly different

power consumption. Accordingly, we take the average power consumption while the apps are running. The power profiles are collected in a 240 min thermal cycle with four phases. In the first hour, the smartphone stays in normal running mode of Android system with a cold start. In the second hour, we start the particular app and record the power consumption for each component of the smartphone using the app. In the third hour, we close the app and let the smartphone cool down. In the last hour, the smartphone is shutdown for a continuous cooling down to ambient temperature.

The power profiles are then sent to the heat transfer model of smartphone based on [33], where we assume the source of heat generation from power consumption are chips and keyboard (LCD). We take the reference from [33] for the parameters of materials and radiation coefficient of the case for cooling. To simplify the 3D IC structure in the smartphone, the layer with TSV is placed at the middle of the sample chip. Since one of the heat generation sources is set to the TSV layer where the power density is larger than that in [33], the temperature of the chip is expected to be higher than the original structure. The pitch size of TSVs in the layer is set to 10 μm for the following simulations.

In the simulations, the power consumption of the smartphone chips vary depending on the power profiles extracted, and the power of LCD (keyboard) remains the same. The temperature profiles collected from the seven apps are shown in Fig. 15. The peak temperature is recorded when running Pokemon Go, which yields a temperature that is 2× higher than the idle case. This aligns well with the observation that Pokemon Go has the highest power among all apps.

The resulting entropy production of each thermal cycle under seven apps, the idle case where no apps are running during the entire cycle, and the corresponding normalized lifetimes are obtained based on the method discussed in Section III and shown in Table IV. Note that we treat the idle scenario as the baseline case in the comparison. From the table we can see that the larger the thermal stress is, the lower the fatigue lifetime is.

With the same power applied on the TSV in smartphone, the highest temperature of the chip in selected apps could achieve as high as 162 °C, which is even higher than the upper limit temperature of normal thermal cycle experiment [34]. It is observed that the rates of entropy production increase in the landing pad and the TSV body are similar. From the table we can see that Pokemon Go results in a severely shortened fatigue lifetime on the TSV. Compared with the idle case, the lifetimes of TSV body and landing pad have been reduced by 89.53% and 89.68%, respectively. Running other apps can result in a lifetime decrease from 81.9% to 55.51% for TSV body and 81.95% to 55.59% for landing pad, respectively, compared with the idle case. These variations suggest that TSV fatigue in smart phones is indeed a serious problem and should not be neglected by designers.

The above analysis assumes that only one app is repeatedly run. However, in real life scenarios, smartphone apps

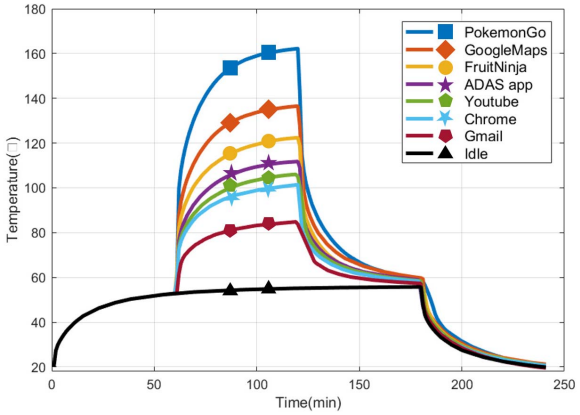


Fig. 15. Stacked TSV-based CPU temperature profiles with various apps running.

TABLE IV
ENTROPY PRODUCTION AND NORMALIZED LIFETIME OF LANDING PAD AND TSV BODY WITH DIFFERENT ANDROID APPS

Running app	Max Entropy Production($\times 10^8$J/m^{3}K)		Normalized Lifetime	
	Landing Pad	TSV Body	Landing Pad	TSV Body
Idle	5.94	4.93	1	1
ADAS app	19.56	16.19	0.3039	0.3044
Google Maps	32.92	27.23	0.1805	0.181
Youtube	19.43	16.07	0.3058	0.3065
Chrome	24.74	20.41	0.2402	0.2415
Gmail	13.38	11.08	0.4441	0.4449
Pokemon Go	57.61	47.08	0.1032	0.1047
Fruit Ninja	26.15	21.86	0.225	0.2255

usage varies depending on the behavior of the users. To further investigate the impact of user behavior on the fatigue life of TSVs in smartphone, we collect eight real user profiles and compute the corresponding lifetime, and the results are shown in Table V. The baseline case again assume a constant idle scenario. Both users 1 and 4 run ADAS app in 30% of a thermal cycle. The fatigue lifetime is significantly shortened by Google Maps by 23.2% compared 20% use of Google Maps with Youtube. Users 3 and 4 has the same usage of ADAS app while user 4 spends 10% more time on Chrome. The lifetime is reduced by 16.6% accordingly. Users 2 and 7 has the same idle time, but the former spends 60% more time in ADAS app, same time with Gmail and 50% less time with Fruit Ninja. As a result, the lifetime is shortened by 16.7%. Additionally, more usage on ADAS app leads to a shorter fatigue lifetime, which can be observed by comparing users 3 and 6.

Therefore, it could be concluded that running various apps in real scenarios on the smartphone with 3D IC TSVs implemented indeed vary the fatigue lifetime of TSVs significantly.

Remark: It is important to note that the power consumption and lifetime reduction caused by two or more running apps running simultaneously is not simply the linear superposition of those from individual app running. How to estimate the lifetime accurately with multiple apps running simultaneously will be our future work.

TABLE V
ENTROPY PRODUCTION AND NORMALIZED LIFETIME OF LANDING PAD AND TSV BODY WITH DIFFERENT ANDROID USERS PROFILES

Users	Runtime of App/Total cycle time								Max Entropy Production($\times 10^8 J/m^3K$)		Normalized Fatigue life	
	Idle (Baseline)	ADAS app	Google Maps	Youtube	Chrome	Gmail	Pokemon Go	Fruit Ninja	Landing Pad	TSV Body	Landing Pad	TSV Body
Idle	100%	0%	0%	0%	0%	0%	0%	0%	5.94	4.93	1	1
1	50%	30%	0%	20%	0%	0%	0%	0%	16.54	13.71	0.3593	0.3594
2	20%	60%	0%	0%	0%	20%	0%	0%	48.96	40.59	0.1214	0.1215
3	40%	30%	20%	0%	10%	0%	0%	0%	25.87	21.45	0.23	0.2298
4	50%	30%	20%	0%	0%	0%	0%	0%	21.54	17.86	0.276	0.2759
5	80%	0%	0%	0%	0%	20%	0%	0%	6.15	5.1	0.967	0.9668
6	60%	10%	30%	0%	0%	0%	0%	0%	11.42	9.47	0.5206	0.5204
7	20%	0%	0%	0%	0%	20%	10%	50%	40.81	33.78	0.1457	0.1459

VII. CONCLUSION

In this paper, a new TSV fatigue model based on entropy production has been proposed. By combining thermodynamics and mechanics laws, the fatigue process can be quantitatively evaluated with the proposed model. The method is compared and validated against measurement data. Experimental results show many interesting and important observations on the impact of TSV structure and location, providing guidance for reliability enhancement. Additionally, full-chip fatigue analysis is performed based on stress superposition. Finally, we conducted experiments on Android smart phones to demonstrate the effect of different apps on the lifetime. To the best of the authors' knowledge, this is the first TSV fatigue model that is free of measurement data fitting, the first that is capable of considering detailed thermal profiles, and the first framework for efficient full-chip TSV fatigue analysis.

REFERENCES

[1] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration," *Proc. IEEE*, vol. 89, no. 5, pp. 602–633, May 2001.

[2] Y. Guillou and A.-M. Dutron, "3D IC products using TSV for mobile phone applications: An industrial perpective," in *Proc. Eur. Microelectron. Packaging Conf. (EMPC)*, 2009, pp. 1–6.

[3] U. R. Tida, R. Yang, C. Zhuo, and Y. Shi, "On the efficacy of through-silicon-via inductors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 7, pp. 1322–1334, Jul. 2015.

[4] U. R. Tida, C. Zhuo, and Y. Shi, "Novel through-silicon-via inductor-based on-chip DC–DC converter designs in 3D ICs," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 11, no. 2, 2014, Art. no. 16.

[5] U. R. Tida, C. Zhuo, and Y. Shi, "Through-silicon-via inductor: Is it real or just a fantasy?" in *Proc. 19th Asia South Pac. Design Autom. Conf. (ASP-DAC)*, Singapore, 2014, pp. 837–842.

[6] M. Jung, D. Z. Pan, and S. K. Lim, "Chip/package co-analysis of thermo-mechanical stress and reliability in TSV-based 3D ICs," in *Proc. 49th Annu. Design Autom. Conf.*, 2012, pp. 317–326.

[7] I. H. Jeong *et al.*, "Analysis of the electrical characteristics and structure of cu-filled TSV with thermal shock test," *Electron. Mater. Lett.*, vol. 10, no. 3, pp. 649–653, 2014.

[8] C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng, "A detailed failure analysis examination of the effect of thermal cycling on cu TSV reliability," *IEEE Trans. Electron Devices*, vol. 61, no. 1, pp. 15–22, Jan. 2014.

[9] N. Khan *et al.*, "Development of 3D silicon module with TSV for system in packaging," in *Proc. 58th Electron. Compon. Technol. Conf. (ECTC)*, 2008, pp. 550–555.

[10] X. Liu, Q. Chen, V. Sundaram, R. R. Tummala, and S. K. Sitaraman, "Failure analysis of through-silicon vias in free-standing wafer under thermal-shock test," *Microelectron. Rel.*, vol. 53, no. 1, pp. 70–78, 2013.

[11] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, "Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA," in *Proc. IEEE 61st Electron. Compon. Technol. Conf. (ECTC)*, 2011, pp. 285–290.

[12] C. S. Selvanayagam *et al.*, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," *IEEE Trans. Adv. Packag.*, vol. 32, no. 4, pp. 720–728, Nov. 2009.

[13] J. Auersperg, D. Vogel, E. Auerswald, S. Rzepka, and B. Michel, "Nonlinear copper behavior of TSV and the cracking risks during beol-built-up for 3D-IC-integration," in *Proc. 13th Int. Conf. Thermal Mech. Multi Phys. Simulat. Exper. Microelectron. Microsyst. (EuroSimE)*, Cascais, Portugal, 2012, pp. 1–6.

[14] T. Frank *et al.*, "Reliability of TSV interconnects: Electromigration, thermal cycling, and impact on above metal level dielectric," *Microelectron. Rel.*, vol. 53, no. 1, pp. 17–29, 2013.

[15] Q. Zeng, W. Meng, Y. Guan, J. Chen, and Y. Jin, "Evaluation and optimization of thermo-mechanical reliability of a TSV-based 3D mems," in *Proc. IEEE 66th Electron. Compon. Technol. Conf. (ECTC)*, 2016, pp. 1797–1802.

[16] S.-H. Choa, C. G. Song, and H. S. Lee, "Investigation of durability of TSV interconnect by numerical thermal fatigue analysis," *Int. J. Precision Eng. Manuf.*, vol. 12, no. 4, pp. 589–596, 2011.

[17] L. J. Ladani, "Numerical analysis of thermo-mechanical reliability of through silicon vias (TSVs) and solder interconnects in 3-dimensional integrated circuits," *Microelectron. Eng.*, vol. 87, no. 2, pp. 208–215, 2010.

[18] M. Jung, J. Mitra, D. Z. Pan, and S. K. Lim, "TSV stress-aware full-chip mechanical reliability analysis and optimization for 3D IC," *Commun. ACM*, vol. 57, no. 1, pp. 107–115, 2014.

[19] M. A. Miner *et al.*, "Cumulative damage in fatigue," *J. Appl. Mechanics*, vol. 12, no. 3, pp. 159–164, 1945.

[20] X. Fan, G. Rasier, and V. S. Vasudevan, "Effects of dwell time and ramp rate on lead-free solder joints in FCBGA packages," in *Proc. 55th Electron. Compon. Technol. Conf.*, Lake Buena Vista, FL, USA, 2005, pp. 901–906.

[21] C. Basaran and C.-Y. Yan, "A thermodynamic framework for damage mechanics of solder joints," *J. Electron. Packag.*, vol. 120, no. 4, pp. 379–384, 1998.

[22] M. D. Bryant, M. M. Khonsari, and F. F. Ling, "On the thermodynamics of degradation," in *Proc. Roy. Soc. A Math. Phys. Eng. Sci.*, vol. 464, no. 2096, pp. 2001–2014, 2008.

[23] M. Naderi, M. Amiri, and M. M. Khonsari, "On the thermodynamic entropy of fatigue fracture," *Proc. Roy. Soc. London A Math. Phys. Eng. Sci.*, vol. 466, no. 2114, pp. 423–438, 2009.

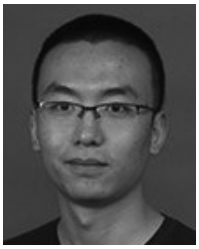
[24] M. Amiri, M. Naderi, and M. M. Khonsari, "An experimental approach to evaluate the critical damage," *Int. J. Damage Mechanics*, vol. 20, no. 1, pp. 89–112, 2011.

[25] J. Morrow, "Cyclic plastic strain energy and fatigue of metals," in *Internal Friction, Damping, and Cyclic Plasticity*. Philadelphia, PA, USA: ASTM Int., 1965, pp. 45–84.

[26] R. Filippi *et al.*, "Thermal cycle reliability of stacked via structures with copper metallization and an organic low-k dielectric," in *Proc. IEEE Int. 42nd Annu. Rel. Phys. Symp.*, 2004, pp. 61–67.

[27] J. Zhang, M. O. Bloomfield, J.-Q. Lu, R. J. Gutmann, and T. S. Cale, "Modeling thermal stresses in 3-d ic interwafer interconnects," *IEEE Trans. Semicond. Manuf.*, vol. 19, no. 4, pp. 437–448, Nov. 2006.

[28] Q. Chen, X. Liu, V. Sundaram, S. K. Sitaraman, and R. R. Tummala, "Double-side process and reliability of through-silicon vias for passive interposer applications," *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 4, pp. 1041–1048, Dec. 2014.
[29] T. H. Low and J. H. L. Pang, "Modeling plated copper interconnections in a bumpless flip chip package," in *Proc. 5th Conf. Electron. Packag. Technol. (EPTC)*, 2003, pp. 791–796.
[30] K. H. Lu *et al.*, "Thermo-mechanical reliability of 3-D ICs containing through silicon vias," in *Proc. 59th Electron. Compon. Technol. Conf. (ECTC)*, 2009, pp. 630–634.
[31] T. Wang, K. Hao, C.-C. Liu, and Y. Shi, "Resource constrained real-time lane-vehicle detection for advanced driver assistance on mobile devices," in *Proc. Symp. Appl. Comput. (SAC)*, Marrakech, Morocco, 2017, pp. 1430–1435. [Online]. Available: http://doi.acm.org/10.1145/3019612.3019650, doi: 10.1145/3019612.3019650.
[32] *What Is the Most Downloaded App in Google Play?* [Online]. Available: https://www.quora.com/What-is-the-most-downloaded-app-in-Google-Play
[33] Z. Luo, H. Cho, X. Luo, and K.-I. Cho, "System thermal analysis for mobile phone," *Appl. Thermal Eng.*, vol. 28, nos. 14–15, pp. 1889–1895, 2008.
[34] N. Khan *et al.*, "Development of 3-D silicon module with TSV for system in packaging," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 1, pp. 3–9, Mar. 2010.



Tianchen Wang (S'17) received the B.S. and M.S. degrees from the North China Electric Power University, Beijing, China, in 2010 and 2013, respectively, and the second M.S. degree in computer engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2015. He is currently pursuing the Ph.D. degree in computer science and engineering with the University of Notre Dame, Notre Dame, IN, USA.

His current research interest includes applications and performance enhancement of deep learning.

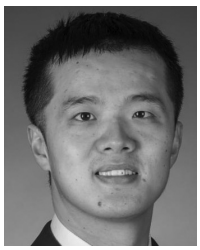
Sandeep Kumar Samal (S'12–M'18) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology Kharagpur, Kharagpur, India, in 2012, and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2013 and 2017, respectively.

He joined Intel Corporation, Hillsboro, OR, USA, in 2017, where he is currently a Senior Engineer, focusing on technology-design integration and process optimization. He has authored over 20 publications in refereed journals and conferences. His current research interests include low power and reliable digital design, technology-design co-optimization, and CAD and modeling for through-silicon-via-based and monolithic 3-D IC technology.

Sung Kyu Lim (S'94–M'00–SM'05) received the B.S., M.S., and Ph.D. degrees from the University of California at Los Angeles, Los Angeles, CA, USA, in 1994, 1997, and 2000, respectively.

In 2001, he joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, where he is currently the Dan Fielder Endowed Chair Professor. His current research interests include modeling, architecture, and electronic design automation for 3-D ICs. His research on 3-D IC reliability is featured as Research Highlight in the Communication of the ACM in 2014. In 2012, his 3-D IC test chip published in the IEEE International Solid-State Circuits Conference is generally considered the first multicore 3-D processor ever developed in academia. He has authored the book entitled *Practical Problems in VLSI Physical Design Automation* (Springer, 2008).

Dr. Lim was a recipient of the National Science Foundation Faculty Early Career Development Award in 2006, the Best Paper Awards from the IEEE Asian Test Symposium in 2012 and the IEEE International Interconnect Technology Conference in 2014, and the Class of 1940 Course Survey Teaching Effectiveness Award from Georgia Institute of Technology in 2016. He was on the Advisory Board of the ACM Special Interest Group on Design Automation from 2003 to 2008 and awarded a Distinguished Service Award in 2008. He was an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS from 2007 to 2009. He has been an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS since 2013. He has served on the Technical Program Committee of several premier conferences in EDA.



Yiyu Shi (S'05–M'10–SM'14) received the B.S. degree (Hons.) in electronic engineering from Tsinghua University, Beijing, China, in 2005, the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 2007 and 2009, respectively.

He is currently an Associate Professor with the Departments of Computer Science and Engineering and Electrical Engineering, University of Notre Dame, Notre Dame, IN, USA. His current research interests include 3-D integrated circuits and machine learning on chips.

Dr. Shi was a recipient of the IBM Invention Achievement Award in 2009, the Japan Society for the Promotion of Science Faculty Invitation Fellowship, the Humboldt Research Fellowship for Experienced Researchers, the IEEE St. Louis Section Outstanding Educator Award, the Academy of Science (St. Louis) Innovation Award, the Missouri S&T Faculty Excellence Award, the National Science Foundation CAREER Award, the IEEE Region 5 Outstanding Individual Achievement Award, and the Air Force Summer Faculty Fellowship. In recognition of his research, he has received many best paper nominations in top conferences.