Frequency and Time Domain Analysis of Power Delivery Network for Monolithic 3D ICs

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***Abstract*—As 2D scaling reaches its limit, monolithic 3D IC (M3D) is a leading contender to continue equivalent scaling. Although M3D shows power and performance benefits over 2D designs, designing a power delivery network (PDN) for M3D is challenging. In this paper, for the first time, we present a system-level PDN model of M3D designs focusing on both resistive (IR) and inductive (Ldi/dt) components of power-supply integrity. In addition, we present frequency- and time-domain analysis of the M3D PDN. We show that the additional resistance in the M3D PDN, while being worse for resistive drops, improves resiliency against current noise showing 35.9% peak impedance reduction during worst-case resonant oscillations.**

I. Introduction

Compared with through-silicon-via (TSV)-based 3D ICs, monolithic 3D ICs (M3D) offer manyfold benefits in vertical dimension for system integration. The key enabler is monolithic inter-tier vias (MIVs) which are 100x smaller than TSVs. This dramatic dimensional reduction opens up numerous opportunities in ultra-fine-grained design optimizations across multiple tiers without a significant overhead.

Challenges in designing a reliable power delivery network (PDN) increase mainly due to lower supply voltage, faster operating clock frequency, and higher power density. Along with restricted budget of resources and cost, these challenges may cause functional failures and performance degradation due to parasitics-induced voltage drop in a non-ideal PDN. The total voltage drop is decomposed into a resistive (IR)-drop component and an inductive (Ldi/dt)-drop component. Increasing the metallization in a PDN can mitigate the resistive component of the voltage drop using wider interconnects while taking into account routing resources and cost budget.

Meanwhile, the inductance of package including controlled collapsed chip connection (C4) bumps leads to significant Ldi/dt-drop due to time-varying current drawn by cells in a die. In order to mitigate this drop, decoupling capacitors (decaps) are utilized for local charge storage. Decaps can be placed on a die with decoupling cells (decap cells), or explicitly added in package. However, this decap along with resistance and inductance of a PDN forms a RLC circuit resulting in its own resonance frequency [1]. If the resonance frequency lies on the system's operating frequency range, significant Ldi/dt-drop can be induced, and hence, it is crucial to have low input impedance across wide range of frequencies.

While PDNs of 2D designs have been explored actively [2][3], PDNs of M3D have not been studied widely. A study for a system-level PDN for TSV-based 3D ICs is presented in [4], but PDNs in M3D and TSV-based 3D ICs show quite different characteristics due to their tier connection method and achievable vertical integration density. In [5], the authors have investigated the impact of PDNs on power and performance of M3D by proposing PDN designs, but the authors did not perform voltage drop analysis on them.

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TABLE I
Comparison of static and dynamic voltage drop in 2D vs. M3D DCT designs

	2D	M3D	Δ%
static voltage drop (mV)	27.6	68.1	146.7 %
dynamic voltage drop (mV)	323.4	346.9	7.3 %
Δ%	1,073.9 %	507.1 %	

In this paper, we present the benefits and challenges of PDNs in M3D designs. Using three benchmarks, we model a system-level PDN circuit of M3D designs as well as 2D designs, and perform in-depth analysis of both static and dynamic behavior of the PDN. We also present resonance frequency analysis and in-rush current study for M3D designs, which shows the frequency and time domain response of the PDN. This, to the best of our knowledge, is the first work studying the dynamic voltage drop as well as the frequency and time domain analysis in M3D.

II. Motivational Example

We compare PDNs of 2D and M3D designs taking into account two analysis modes. The static mode is a vector-less analysis mode wherein the switching activity of cells is averaged into a single instance. In the dynamic mode, we perform a real workload-based (vector-based) power analysis for a given period of time. The dynamic mode thus incorporates the impact of inductive (Ldi/dt) transients by taking into account workload-dependent time-varying current flow.

Although both M3D and TSV-based 3D ICs utilize vertical integrations to connect PDNs in multiple tiers, there are major differences which impact on their behaviors in both static and dynamic mode.

In TSV-based 3D ICs, power is delivered directly to power pads of each tiers through dedicated power TSVs, forming a parallel resistive path between multiple tiers, However, in M3D, instead of having external power pads on the bottom tier, power MIVs are utilized to connect the bottom metal layer of the top tier PDN and the top metal layer of the bottom tier PDN, consisting of a series resistive path across multiple tiers, so that bottom tier cells experience much longer resistive path compared to TSV-based 3D ICs. Furthermore, irregular power MIV placement due to cell blocking on the top tier makes power delivery issue more complicated in M3D. For these reasons, M3D suffers from much higher voltage drop in the static mode, especially on cells on the bottom tier as shown in Table I than TSV-based 3D ICs [4].

Although the series resistive path of a M3D PDN worsens the voltage drop in the static mode, it benefits the voltage drop in the dynamic mode by improving resiliency against AC noise, which will be discussed in later of this paper. Thus, the difference in the voltage

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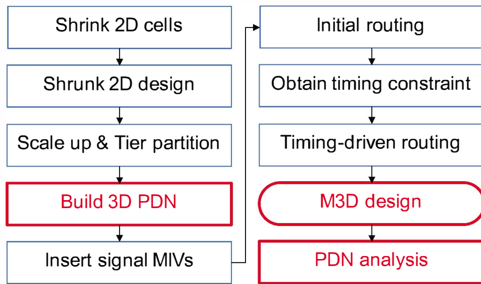

Fig. 1. Our M3D design flow based on [6], extended to insert PDN

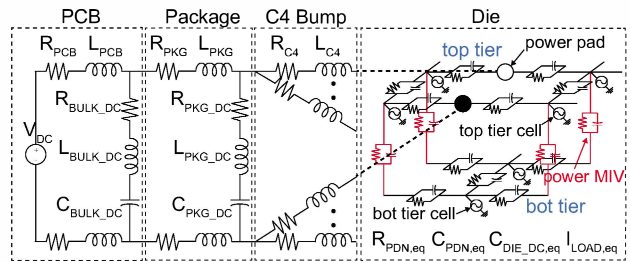

Fig. 2. Our simplified model of the system-level PDN structure

drop between the 2D and the M3D design in the dynamic mode is 7.3%, which is similar to TSV-based 3D ICs [4].

In the following sections, we perform an in-depth study of M3D PDNs to explain the significantly different trend in the voltage drop in two analysis methods, and investigate the benefits and challenges of M3D PDNs over 2D designs.

III. Design Flow

Fig. 1 shows the overview of the M3D design flow including a PDN used in this paper. The authors of [6] presented a M3D design flow, but it does not include a PDN design step. In this work we have extended the flow to incorporate a PDN design in M3D.

The flow starts with scaling x-y dimension of all existing 2D standard cells and metal wires by $1/\sqrt{2}$ since cells in a M3D design are placed on half footprint of the corresponding 2D design, but onto two tiers. Then, a shrunk 2D design is implemented with the shrunk cells and metal wires, performing all steps required in 2D implementation. From the shrunk 2D design, only cell placement is retained, and all other information is discarded. After that, the size of all cells are scaled up to their original size, which results in overlaps between the cells. In order to remove these overlaps and place the cells onto two tiers, we perform min-cut area-balanced partitioning, so that half of the cells are placed on the top tier and the other half on the bottom tier.

To build a full M3D PDN and determine the location of signal MIVs, we duplicate all metal layers, so that the original metal layers account for those in the bottom tier, and the duplicated ones in the top tier. In addition, the metal layer of pins in every cell is annotated with their respective tiers, so that pins of bottom tier cells utilize M1 of the bottom tier, and top tier cells, M1 of the top tier.

Before determining the location of signal MIVs, it is crucial to build a M3D PDN with the full metal stack (the original and the duplicated metal layers) because the signal MIVs should not be placed at the location that power MIVs are to be placed, thereby preventing the signal MIVs from deteriorating the quality of the M3D PDN. After having the PDN structure of the M3D design including the power MIVs, the signal MIV location is determined by routing the design and using the location of vias connecting the top metal layer of the bottom tier and the bottom metal layer of the top tier.

Then, with the netlist of each tier and the location of MIVs along with the PDN design, initial-routing is performed, and timing constraints for each tier are derived. The timing-constraints are used to perform timing-driven routing for each tier, resulting in fully placed and routed designs for each tier. The designs are then merged into a single final M3D design, and timing/power analysis as well as PDN analysis is performed.

IV. System-Level PDN Modeling

In order to perform an in-depth PDN analysis, it is crucial to build a system-level PDN model. Fig. 2 shows a simplified representation of the PDN design. It consists of a system model and a die model, and the system model is further categorized into C4 bump, package, and printed circuit board (PCB) models [7].

In the die model, the parasitics of the PDN of a design is extracted from Cadence® Voltus™. In Fig. 2, the resistance of the metal wire, $R_{PDN,eq}$, represents the equivalent resistive parasitics of the metal wires consisting the PDN of the implemented design, and the implicit decaps of the die, $C_{PDN,eq}$, consists of the equivalent capacitance of the PDN metal wires, non-switching device capacitance, and coupling capacitance between N-well and substrate. The current drawn by switched cells is lumped by the tool and modeled as an AC load current source, $I_{LOAD,eq}$.

We design our representative lumped system model based on the parameters obtained from [2] and [7]. The C4 bumps and power-line traces in the package and PCB are modeled as a series connection of the a resistor and a inductor (C4 bumps: R_{C4} = 1mΩ and L_{C4} = 10pH; package: R_{PKG} = 10mΩ and L_{PKG} = 100pH; PCB: R_{PCB} = 5mΩ and L_{PCB} = 1uH), and a DC voltage source supplies power on the PCB. The inductor and the capacitor used in the Voltage Regulator Module (VRM) LC-tank filter are incorporated within the PCB parasitics.

Since the implicit decaps alone is not sufficient to keep the design in safe voltage drop region from Ldi/dt-drop, explicit decaps are deployed both on the die using decap cells, $C_{DIE_DC,eq}$, and on the package and PCB using discrete decaps, C_{PKG_DC} (= 400nF) and C_{BULK_DC} (= 400uF), respectively. The discrete decaps are modeled by a capacitor connected to an effective resistor and inductor in series (R_{PKG_DC} = 20mΩ and L_{PKG_DC} = 200pH; R_{BULK_DC} = 10mΩ and L_{BULK_DC} = 2nH). These explicit decaps and the implicit decap of the die act as charge storage elements and prevent system failure or performance degradation due to severe Ldi/dt-drop.

V. Experimental Setup

Three benchmarks, DCT, AES-128, and JPEG Encoder from OpenCores are used as benchmarks in this study. Nangate 45nm Open PDK is used to synthesize, place and route the designs. 2D designs and each top and bottom tier of M3D designs are implemented using 7 metal layers. The footprint of the 2D designs are determined such that the cell utilization is 60%, and the M3D designs have half the footprint of the corresponding 2D designs. Target frequency of each benchmarks is fixed to their maximum operating frequency available in the technology node.

Table II summarizes the resources used on each metal layer to build the 2D and M3D PDN designs. The dimensions of power rails are determined by targeting the maximum instance IR-drop to be 5% of nominal voltage (1.1V) for the 2D designs of all benchmarks in static

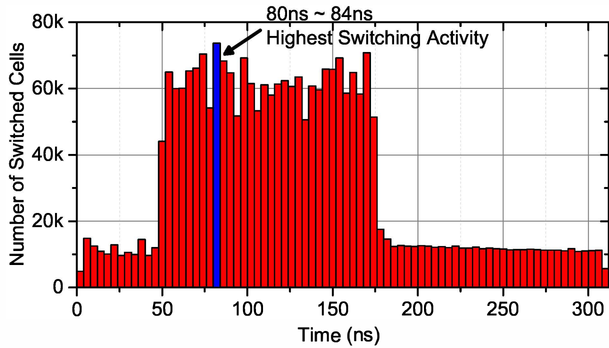

Fig. 3. Number of switched cells during a workload-based simulation. Only the time period which shows the highest switching activity (blue bar) is used for analysis.

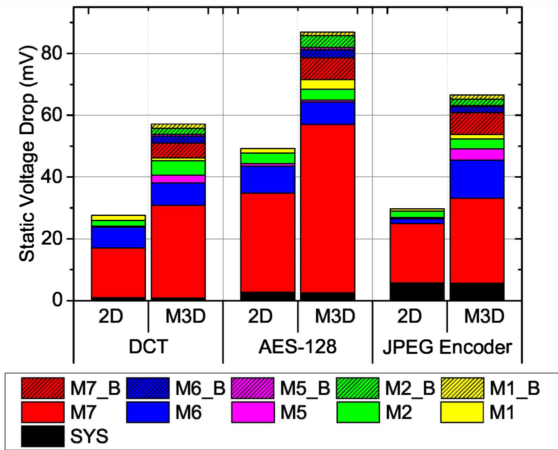

Fig. 4. Breakdown of the maximum instance static IR-drop across metal layers. M7_B denotes M7 of the bottom tier in M3D design. SYS represents IR-drop experienced at the system model which includes C4 bump, package, and PCB model.

rail analysis. For fair comparison, same metrics are used for both the top and the bottom tier of the M3D designs. Power rails on M1 and M2 layers are tightly coupled and run in parallel in the horizontal direction of the design, and M2 and M5 power rails are connected with only via arrays, which cross M3 and M4 metal layers. Power rails on M5 to M7 metal layers form a mesh-structure to distribute power across the chip.

Since Nangate 45nm Open PDK does not provide decap cells, we made our own decap cells with various sizes for our experiment. Table III shows the size and decoupling capacitance of the decap cells. The decoupling capacitance of each cell is derived using the method presented in [8]. With the fully placed and routed 2D and M3D designs, decap cells are first placed next to clock buffers and inverters which drive clock pins of flip-flops, which usually suffer from high Ldi/dt-drop. Then, rest of decap cells are placed in empty area of the design to meet a target decoupling capacitance of the chip.

The power and ground pads of the designs are located on the top metal layer of designs (M7 for the 2D designs, M7 of the top tier for the M3D designs) with 120um spacing, which model the C4 bumps of the designs.

TABLE II
WIDTH, PITCH, AND UTILIZATION OF PDN. WE USE THE SAME SPECS FOR BOTH 2D AND M3D (BOTH TOP AND BOTTOM TIER) DESIGNS. WIDTH AND PITCH ARE IN um.

metal layer	direction	width	pitch	utilization
M2	H	0.07	1.4	10.0 %
M5	V	0.28	14	20.6 %
M6	H	0.28	14	20.6 %
M7	V	0.8	42	11.1 %

TABLE III
DESIGN METRICS AND DECOUPLING CAPACITANCE VALUES OF OUR DECAP CELLS. CELL WIDTH AND HEIGHT ARE IN um, AND CAPACITANCE IN fF.

cell name	cell width	cell height	cap
DECAP_X1	0.19	1.4	3.4
DECAP_X2	0.38	1.4	6.8
DECAP_X4	0.76	1.4	13.7
DECAP_X8	1.52	1.4	27.3
DECAP_X16	3.04	1.4	54.7
DECAP_X32	6.08	1.4	109.4

VI. RESULTS AND ANALYSIS

Fig. 3 shows the number of switched cells in the DCT design during workload-based simulation. The vector-based power consumption in Table IV is measured during the time step which shows the highest switching activity throughout the simulation (blue bar in Fig. 3), while the statistical power consumption of the designs is calculated assuming the switching ratio of the primary input and sequential logic as 20% and 10%, respectively. Therefore, we observe that the dynamic power (internal + switching power) shows significant difference between two analysis methods whereas the static power (leakage power) remains similar.

The M3D designs offer power benefit over their 2D counterparts. Since M3D designs utilize short vertical integration with MIVs instead of using long metal wires on x-y plane, wire-length of the designs are reduced, as shown in Table V, offering switching power saving. In addition, since cells drive reduced wire-load, the number of buffers as well as the drive-strength of cells decreases, which, in turn, reduces the standard cell area, hence, showing benefits on the internal and leakage power consumption.

A. Static Rail Analysis

Since static rail analysis is based on statistical power consumption, which summarizes the behavior of designs, only IR-drop can be analyzed. Fig. 4 shows the breakdown of the maximum IR-drop into each metal layers consisting the PDN of the 2D and M3D designs. The M3D designs show approximately 2x higher IR-drop on average compared to the 2D counterparts. Since M3D designs utilize more metal layers for their PDN structure to deliver power to the cells on the bottom tier, those cells experience worse IR-drop compared to the top tier cells (The dashed box from M1_B to M7_B in Fig. 4).

Another reason for the higher IR-drop in M3D design is irregular placement of power MIVs which connect PDNs of two tiers. Fig. 5 illustrates the impact of irregular power MIV placement. In M3D PDNs, current flowing in metal layers of the top tier is greater than those of the bottom tier (e.g. $I_{M7_T} > I_{M7_B}$ in Fig. 5) since top tier metal layers deliver current to both top and bottom tier cells whereas only current drawn by bottom tier cells flows on bottom tier metal layers. Therefore, the minimum IR-drop path in Fig. 5 to

TABLE IV
POWER COMPARISON OF 2D AND M3D. WE CONDUCT BOTH STATISTICAL AND VECTOR-BASED POWER SIMULATIONS.

benchmark		DCT 2D	DCT M3D	DCT Δ%	AES-128 2D	AES-128 M3D	AES-128 Δ%	JPEG Encoder 2D	JPEG Encoder M3D	JPEG Encoder Δ%
statistical power analysis	internal power (mW)	16.4	16.2	-1.6 %	49.3	48.5	-1.6 %	109.4	109.8	0.4 %
	switching power (mW)	15.9	13.4	-15.8 %	46.8	41.1	-12.3 %	93.4	89.3	-4.4 %
	leakage power (mW)	0.8	0.7	-2.8 %	1.9	1.7	-7.6 %	4.5	4.4	-1.9 %
	total power (mW)	33.1	30.3	-8.4 %	98.0	91.3	-6.8 %	207.3	203.6	-1.8 %
vector-based power analysis	internal power (mW)	48.0	51.2	6.7 %	197.3	186.0	-5.7 %	218.1	222.1	1.8 %
	switching power (mW)	36.7	31.3	-14.7 %	134.8	87.9	-34.8 %	88.8	91.8	3.4 %
	leakage power (mW)	0.7	0.7	-3 %	2.0	1.8	-7.2 %	4.7	4.6	-2.1 %
	total power (mW)	85.4	83.2	-2.6 %	334.0	275.7	-17.5 %	311.6	318.5	2.2 %

TABLE V
DESIGN METRIC COMPARISON OF 2D AND M3D. Δ% FOR M3D DESIGNS IS CALCULATED WITH RESPECT TO THE 2D COUNTERPARTS.

benchmark	DCT 2D	DCT M3D	DCT Δ%	AES-128 2D	AES-128 M3D	AES-128 Δ%	JPEG Encoder 2D	JPEG Encoder M3D	JPEG Encoder Δ%
frequency (MHz)	500	500	-	1,000	1,000	-	500	500	-
footprint (um^2)	369x368	260x260	-50.2 %	509x507	360x360	-49.8 %	897x895	634x636	-49.8 %
C4 bump count	9	4	-55.6 %	16	9	-43.8 %	64	25	-60.9 %
std cell area (um^2)	85,432	85,312	-0.1 %	166,560	163,938	-1.6 %	503,070	503,068	0 %
wire-length (um)	784,072	723,139	-7.8 %	1,921,276	1,708,362	-11.1 %	3,770,356	3,730,150	-1.1 %
total capacitance (pF)	236.1	220.0	-6.8 %	568.6	500.3	-12 %	1,186.4	1,153.7	-2.8 %
signal MIV count	-	11,753	-	-	50,589	-	-	58,807	-

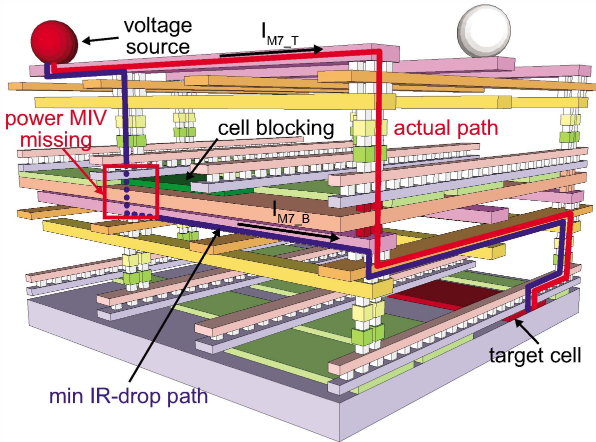

Fig. 5. Current path to deliver power to a target cell. A top tier cell is blocking a power MIV along the minimum IR-drop path, so the current is delivered through an alternative path.

deliver power to a bottom tier cell utilizes the minimum length of top tier power rails. However, the path can be blocked by missing power MIV. The absence of power MIV stems from top tier cells since MIVs cannot penetrate those cells in order to preserve their active areas. In this case, the current needs to flow through an alternative path shown as actual path in Fig. 5, which utilizes longer top tier metal wires and hence, exhibits worse IR-drop due to higher current in those wires. It is important to note that top tier metal layers are more susceptible to electromigration because of higher currents, however that discussion is out of the scope of this work.

The reduced number of C4 bumps in a M3D design also degrades voltage integrity. As the footprint of a M3D design is half of its 2D counterpart, the number of the C4 bumps that can be placed in the M3D design is approximately half of those in the 2D design as shown in Table V. This affects the amount of current flowing through each

TABLE VI
AVERAGE AMOUNT OF CURRENT FLOWING THROUGH C4 BUMPS IN 2D AND M3D DESIGNS. THE UNIT OF CURRENT IS mA.

benchmark	2D	M3D	Δ%
DCT	3.34	6.89	106.07 %
AES-128	5.48	9.23	68.20 %
JPEG Encoder	2.87	7.34	155.73 %

C4 bump. Table VI compares the average current flowing through C4 bumps in the 2D and M3D designs. Up to 155.7% higher current flows through the C4 bumps in the M3D designs incurring significant difference in IR-drop on the top metal layer (M7) in Fig. 4.

However, in typical systems, Ldi/dt-drop dominates over IR-drop [2]. The longer resistive path and the higher effective resistance of C4 bumps of a M3D PDN increases the damping factor during worst-case resonant oscillations, effectively attenuating the amplitude of oscillations. We demonstrate this counter-intuitive behavior of M3D PDNs in the following sub-sections.

B. Dynamic Rail Analysis

Unlike static rail analysis, the dynamic voltage drop consists of two categories, resistive (IR)-drop and inductive (Ldi/dt)-drop. Ldi/dt-drop has significantly higher impact on the voltage drop since we perform dynamic rail analysis for two clock cycles with the maximum switching activity in a real workload. The voltage drop of the M3D designs is 11.3% higher on average than the 2D designs as shown in Fig. 6, which is much less than that in the static rail analysis.

The first thing to note in Fig. 6 is that, in the dynamic rail analysis, the difference between the voltage drop of the metal layers in the 2D design and the metal layers of the top tier in the M3D PDN is significantly less than that in the static rail analysis. The reduced voltage drop on those metal layers first results from 3D placement of decaps in M3D designs. As discussed in Section IV, decaps from non-switching devices (implicit) and decap cells (explicit) in a design act as charge reservoir, preventing nearby cells from experiencing

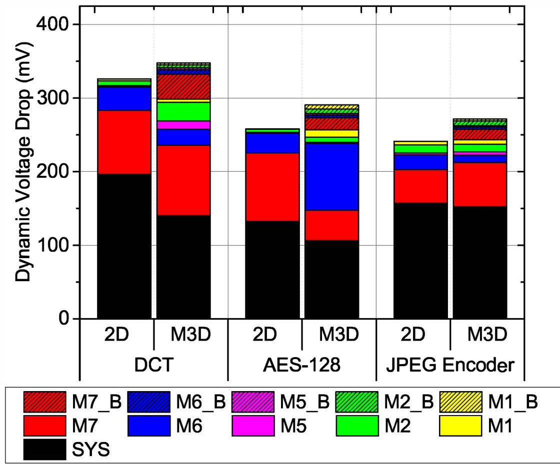

Fig. 6. Breakdown of the maximum instance dynamic voltage drop (= IR-drop + Ldi/dt-drop) across metal layers

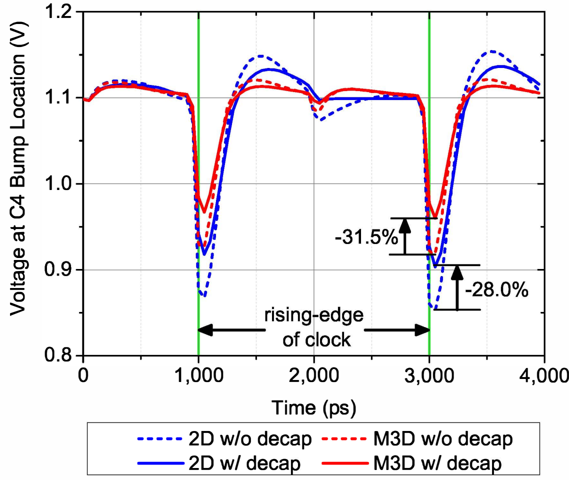

Fig. 7. Comparison of the worst voltage drop experienced at C4 bump. The decoupling capacitance is set to 30% of the total capacitance of the design.

sudden high Ldi/dt-drop. In M3D designs, Ldi/dt-drop is reduced because of decap cells in both, the x-y plane, as in the case of 2D designs, as well as decap cells in the adjacent tier (z-dimension), as in TSV-based 3D ICs [4].

Fig. 7 shows the maximum voltage drop experienced at the C4 bump comparing the 2D and M3D DCT designs with and without decap cells. The decoupling capacitance of the 2D and M3D designs with decap cells is targeted to 30% of their total capacitance. Even though the decoupling capacitance added to the M3D design (72.6pF) is smaller than the 2D design (77.9pF) due to the lower total capacitance of the M3D DCT design, it benefits more from the added decap cells than the 2D design as it utilizes decaps in the z-dimension as well.

Another reason for the smaller gap between the 2D and M3D voltage drop in the dynamic rail analysis is the reduced voltage drop on the system model as shown in Fig. 6. This can be explained by the varying impedance seen from the die depending on operating frequency, which will be discussed in detail in the next sub-section.

TABLE VII
EFFECTIVE RESISTANCE AND CAPACITANCE OF 2D AND M3D PDN. RESISTANCE IS IN Ω, AND CAPACITANCE IN nF.

		2D	M3D	Δ%
DCT	$R_{PDN,eq}$	0.221	0.812	267.5 %
	$C_{PDN,eq}$ + $C_{DIE_DC,eq}$	0.232	0.211	-8.7 %
	product of R and C	0.051	0.172	235.5 %
AES-128	$R_{PDN,eq}$	0.164	0.341	108.1 %
	$C_{PDN,eq}$ + $C_{DIE_DC,eq}$	0.528	0.439	-16.8 %
	product of R and C	0.086	0.150	73.1 %
JPEG Encoder	$R_{PDN,eq}$	0.076	0.202	164.4 %
	$C_{PDN,eq}$ + $C_{DIE_DC,eq}$	1.290	1.220	-5.4 %
	product of R and C	0.098	0.246	150.1 %
average product of R and C		0.079	0.189	140.4 %

C. Frequency and Time Domain Analysis

As shown in Fig. 2, implicit and explicit decaps on a die model are coupled with inductors in a system model, forming an RLC circuit. The RLC circuit has its own resonance frequency, causing significant voltage drop on the PDN even with small changes in load current. Explicit decaps on the package and PCB also forms RLC circuits with the corresponding inductors, showing their unique resonance frequencies.

In order to perform in-depth frequency and time domain analysis on a PDN, a reasonable die model which represents 2D and M3D full-chip SoC is needed. Since the benchmarks used in this work are small compared to full-chip SoC designs, we use their parameters to create a full-chip die model for our analysis. Table VII shows the effective resistance and capacitance of the PDN of each benchmark ($R_{PDN,eq}$ and $C_{PDN,eq}$ + $C_{DIE_DC,eq}$ in Fig. 2, respectively). We observe that as a design becomes larger, the capacitance of its PDN increases due to the increased ground and coupling capacitance of the PDN, while the resistance becomes smaller because more number of parallel resistive paths to the cells are available. For ease in modeling, we take the average of the RC product from the three benchmarks, and then model a full-chip die by assuming $C_{PDN,eq}$ + $C_{DIE_DC,eq}$ = 10nF, resulting in the associated resistances as 7.87mΩ and 18.9mΩ for the 2D and M3D designs, respectively.

Fig. 8 shows the frequency response of the 2D and M3D full-chip SoC sweeping the frequency of the AC load current source, $I_{LOAD,eq}$. We observe three resonance frequency points, first-order resonance caused by $C_{PDN,eq}$ + $C_{DIE_DC,eq}$ coupled with L_{C4}, second-order resonance by C_{PKG_DC} with L_{PKG}, and third-order resonance by C_{BULK_DC} with L_{PCB}. While third-order and second-order resonance occurs at a few kHz and MHz range, the largest resonance, first-order resonance is in the range between 50MHz-200MHz. Although the M3D design shows 16.7% increase at second-order resonance frequency, as the operating frequencies of full-chip designs at advanced technology nodes are in the range of first-order resonance frequencies, it is crucial to minimize the first-order resonance impact for a robust PDN.

As shown in the figure, the M3D design exhibits 35.9% lower peak impedance at first-order resonance frequency because of high effective resistance of the M3D PDN due to the series resistive path across tiers. A very interesting point to note is that the high resistance of the M3D PDN, which worsens IR-drop, in fact, improves the resiliency against noise by damping noise at worst-case resonance oscillation. This work is the first comprehensive study to demonstrate this effect of M3D designs.

Fig. 9 (a) and (b) shows the improved resiliency of the M3D PDN, showing the time-domain response for a unit step, which models

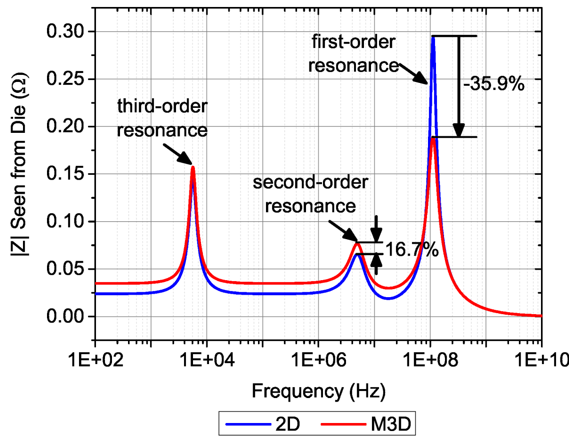

Fig. 8. Impedance seen from ΔV_{DIE} in Fig. 2 by sweeping the frequency of AC load current source, $I_{LOAD,eq}$

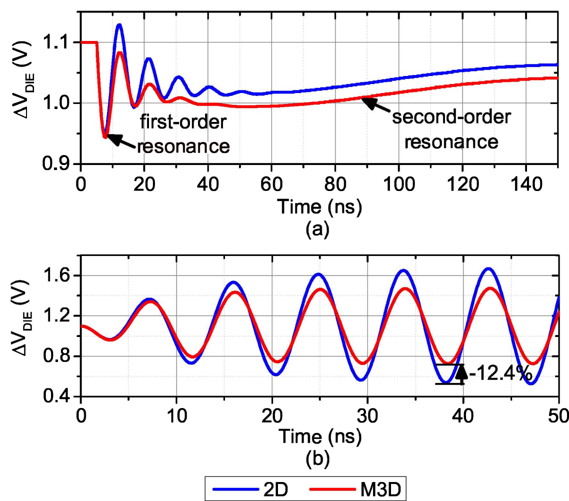

Fig. 9. Transient voltage response for (a) a unit step, and (b) a unit 112MHz (first-order resonance frequency) sine-wave load current source, $I_{LOAD,eq}$. Third-order resonance frequency is not shown in (a) for brevity.

in-rush current simulation, and for a 112MHz (first-order resonance frequency) unit sine-wave load current source. Eq. 1 explains the die voltage response affected by first-order resonance for a unit step load current source [7].

$$\Delta V_{DIE} \cong 2R + \sqrt{\frac{2L_{C4}}{C_{DIE,eq}}} \cdot e^{-\frac{R}{2L_{C4}}t} sin(\omega_r - \theta) \qquad (1)$$

where R = R_{PCB} + R_{PKG} + R_{C4} + $R_{PDN,eq}$, ω_r and θ are first-order resonance frequency and phase, respectively. While the increased R in a M3D worsens the IR-drop at cell (the first term in Eq. 1), it helps to reduce the second term, Ldi/dt-drop. The improved resiliency for first-order resonance helps to neutralize the voltage drop gap induced by second-order resonance in the worst voltage drop as shown in Fig. 9, and shows 12.4% less voltage drop with current source oscillating at first-order resonance frequency as shown in Fig. 9 (b).

VII. Observations

We summarize our findings on in-depth analysis of the M3D PDN.

- We observed approximately 2x higher IR-drop in the M3D designs in the static rail analysis based on the statistical power simulation.
- The higher IR-drop in M3D results from first, increased resistive path due to additional metal layers to pass through to supply power to bottom tier cells, second, irregular placement of power MIVs due to top tier cells, which prevents current from flowing the optimal resistive path, third, high current flowing C4 bumps due to the reduced number of C4 bumps placed in M3D design.
- We observed that the voltage drop gap between the 2D and M3D design is significantly reduced if Ldi/dt-drop is also considered. We performed workload-based power analysis to analyze the dynamic behavior of the PDNs. The voltage drop difference, which includes both IR-drop and Ldi/dt-drop, of the 2D and M3D designs is only 11.3%, which is much lower than that in the static rail analysis.
- The reduced difference in dynamic rail analysis results from lower Ldi/dt-drop of M3D design. In M3D designs, a cell utilizes decaps placed on the same tier (x-y plain) as well as on the different tier (z-direction) showing more Ldi/dt decrease with less decap cells.
- Although the increased resistance of M3D PDN due to series connection across tiers worsens IR-drop, it makes M3D PDN more resilient to the overall current noise during the worst-case resonance oscillations showing 35.9% peak impedance reduction.
- Since M3D PDN shows its strength on Ldi/dt-drop, M3D PDN optimization should be focused on reducing IR-drop by first, using wider width for top tier metal layers in M3D PDN since higher current flows in the metal layers than those of the bottom tier, second, avoiding top cell placement on the location that power MIVs are to be placed, so that current flows the minimum resistive path without being blocked.

VIII. Conclusions

In this paper, we, for the first time, presented an in-depth study of PDNs in M3D designs. We built a system-level PDN of M3D designs, and performed comprehensive studies including static, dynamic rail analysis as well as frequency and time domain analysis. Although M3D PDNs suffer from high IR-drop due to additional metal layers, irregular placement of power MIVs, and less C4 bumps, they reduce Ldi/dt-drop from 3D placement of decap cells. Additionally, higher resistance of M3D PDN due to its series resistive path across tiers improves the resiliency against AC noise showing up to 35.9% peak impedance reduction at first-order resonance frequency. This work paves the way for future research in designing optimized M3D PDNs, trading off worse IR-drop for better noise immunity.

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