Full Chip Power Benefits with Negative Capacitance FETs

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***Abstract*—We study, for the first time, full chip power benefits of negative capacitance FET (NCFET) device technology for commercial-grade GDSII-level designs. Owing to sub-60mV/decade characteristics, NCFETs provide significantly higher drive-current than standard FETs at a given voltage, enabling significant iso-performance power savings by lowering VDD. We use SPICE models of NCFETs corresponding to 14nm node, which incorporate experimentally calibrated models of ferroelectric. We then characterize NCFET-based standard-cell libraries followed by full-chip NCFET-based GDSII-level design implementations of different benchmarks. Our results show that even with increased device capacitance, we can achieve about 4X (up to 74.7%) full-chip power reduction with low-VDD NCFETs over nominal VDD baseline FETs at iso-performance. The power savings are consistent across multiple benchmarks and are higher for low power designs.**

I. Introduction

With increasing challenges in technology scaling, the next generation energy efficient circuits and systems need novel semiconductor devices which can overcome the so-called Boltzman tyranny and have a sub-threshold slope (SS) better than 60mV/decade at room temperature. Indeed, the research for sub-60mV/decade switches has gained significant momentum with several options being aggressively explored [1]. Negative capacitance FETs (NCFET) are rapidly emerging as a very strong candidate for achieving this important break-through in SS. Fig. 1 shows the structure of a typical NCFET device. In terms of device fabrication, the structure is very close to the fabrication of regular FETs, and thus the existing industry infrastructure does not need significant changes for mass production. In terms of device performance, NCFETs not only promise a sub-60 mV/decade but also improved on-current [2], making them a very attractive prospect.

After the recent experimental demonstration of NCFETs [3], device modeling and small-scale circuit-level analysis studies have been performed [4], [5]. However, there is a clear need to analyze and demonstrate the impact of NCFETs on large commercial-grade circuits. None of the prior works have carried out such a study using practical GDSII designs, where device, interconnect and design features play a combined role in determining realistic benefits. In our work, we perform such a study in detail and show the large-scale advantages of NCFETs over baseline FETs. According to the best of our knowledge, for the first time, we study and explain power benefits of NCFET based digital designs from gate to full-chip level using real GDSII level layouts and sign-off analysis. The major contributions of this paper are: (1) We incorporate accurate SPICE device models of NCFETs corresponding to 14nm node in the design flow and generate standard cell libraries for circuits based on NCFETs. (2) We study the power-performance trade-off for NCFETs at a full-chip level at various VDDs and demonstrate significant iso-performance power reduction. (3) We study the advantage of NCFETs for low power, low-speed, low voltage designs and highlight the impact of leakage savings at lower VDD.

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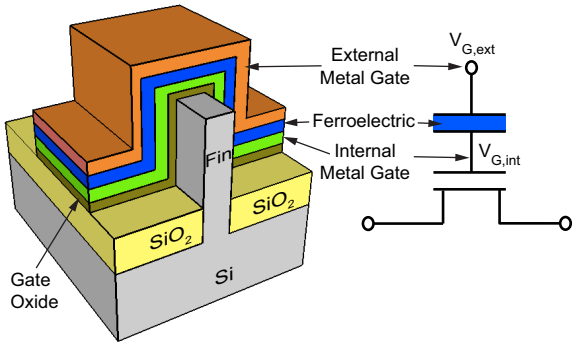

Fig. 1. Negative capacitance FET device structure. Internal gate voltage controls the drain current.

II. NCFET Device

The idea of NCFETs was proposed by Salahuddin *et al.* [6]. Since then, several experimental demonstrations have been made showing sub-60 mV/decade sub-threshold slope at room temperature overcoming the Boltzman tyranny [3], [7], [8] . A recent demonstration of negative capacitance FinFETs [3] brings these devices even closer to the main-stream technologies, demonstrating the applicability of the original idea for advanced nodes. NCFET device in [3] consist of regular FinFET device (baseline FET) and a ferroelectric layer is deposited on it to take the advantage of its negative capacitance behavior (Figure 1). Negative capacitance is shown to not only improve the sub-threshold slope but also increase the on-current. The actual voltage which the baseline FET "sees" gets amplified due to the negative capacitance phenomenon [2].

A schematic of NC-FinFET device being used in this work is shown in Figure 1. Lee *et al* have fabricated such NCFET devices in [3]. They have presented the fabrication flow along with measured device characteristics. This device has internal- and external-gate contacts. When the device is measured from internal-gate (while external gate is floating) the baseline FinFET I-V characteristics can be obtained. On the other hand, NC-FinFET I-V can be obtained via the measurements taken from the external gate connection. The characteristics of the NCFETs depends on both the baseline device and the ferroelectric layer. Measurements from both internal- and external-gate contacts were performed and used to develop the SPICE model as explained in the next section.

III. NCFET SPICE Model

To perform circuit level studies with NCFETs, a SPICE device model is required. Accurate SPICE model development for these new devices have been discussed in prior works [4], [9]. We develop an accurate physics-based SPICE model for these devices, based on these works. In our model, three-dimensional electrostatics for

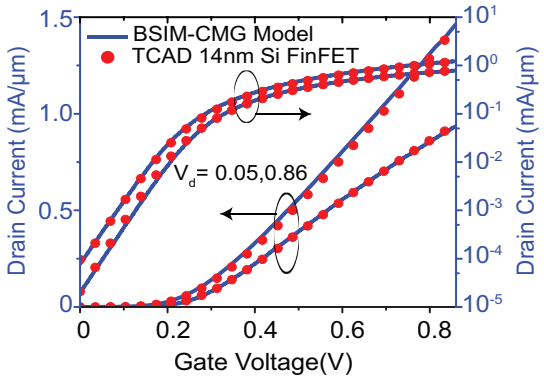

Fig. 2. Our baseline FET model validation: agreement between high performance CMOS 14 nm ITRS TCAD and our BSIM-CMG model.

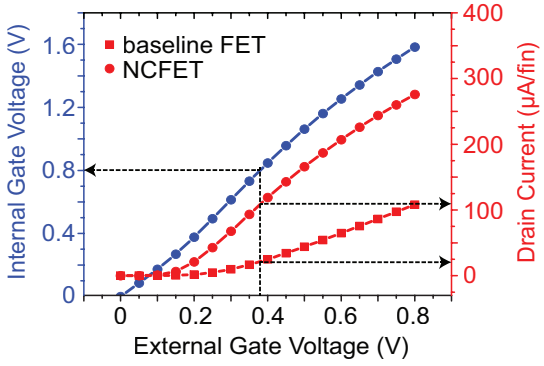

Fig. 3. ON-current and internal gate voltage amplification in NCFETs.

the baseline FinFET device is solved self-consistently with single-domain Landau-Khalatnikov (L-K) model for ferroelectric layer. The ferroelectric response time is assumed to be much smaller than the baseline FET delay in our model.

First, we model the experimental baseline FinFET using the industry standard BSIM-CMG compact model. BSIM-CMG accurately models the second-order effects for aggressively scaled devices and also accounts for different fin-shapes and short-channel effects [10]. An accurate baseline FinFET model is very important to develop a model for NC-FinFETs as L-K equations depend on the charge of the baseline FinFET device. NCFET behavior depends on the charge that the ferroelectric layer "sees". Since the negative capacitance of the ferroelectric layer and the baseline FET capacitance are in series, ferroelectric layer sees the same charge as the baseline FET device. This underlines the importance of an accurate baseline FET model.

Next we model the experimental NCFET device. As we have already modeled the baseline FinFET in previous step, only ferroelectric layer parameters are adjusted for modeling NCFET, the baseline FinFET parameters remains fixed to the values obtained in the previous step. This enables us to get an accurate and experimentally calibrated values for the ferroelectric parameters of L-K equations. The thickness of the ferroelectric layer in our device is T_{fe} = 5 nm. The values obtained for the other ferroelectric layer parameters obtained after modeling are: Critical electric field E_c = 0.7 MV/cm and remnant polarization P_0 = 6 μ C/cm^2. In addition to the parameters E_c and P_0, we found that trapped charges in the ferroelectric layer also needs to be considered in the model. These are accounted for by modeling it as equivalent voltage due to charges

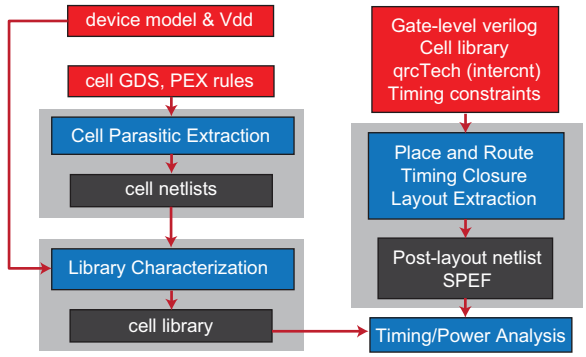

Fig. 4. Design flow used in our work. All steps are carried out using commercial state-of-the-art CAD tools.

TABLE I
SUMMARY OF BENCHMARKS USED IN OUR STUDY (BASED ON GDSII LAYOUTS WITH 14NM BASELINE FET PDK).

Benchmark	Footprint ($\mu m \times \mu m$)	Cell count	Frequency (GHz)
itc99_b19	200×200	64K	1.4
aes	250×250	128K	2.0
jpeg	450×450	280K	1.6
fft	480×480	338K	1.6
256-bit multiplier	750×750	700K	1.0

(V_c) which appear across the ferroelectric layer. We obtained V_c to be 15 mV in our experimental data.

The experimentally calibrated ferroelectric parameters obtained by modeling NCFET represent a fabricated ferroelectric layer. Now, for a new baseline device the same ferroelectric layer model can be used. To obtain meaningful results at circuit level we use the new baseline device as the ITRS 14 nm high performance technology device (nominal VDD = 0.8V). The device dimensions for the new baseline device are: Fin-height H_{fin} = 42 nm, Channel length L = 20 nm, and Fin-thickness T_{fin} = 7 nm. We model the new baseline device with BSIM-CMG model and obtained an excellent model agreement as shown in Figure 2. Both I_{DSAT} and I_{LIN} are plotted with the corresponding drain voltage values labeled. The current is also plotted in linear scale to show the high accuracy of our model at on-current values. This new baseline FET model is used in conjunction with the experimentally obtained ferroelectric parameters to obtain the SPICE model for NCFETs corresponding to 14nm technology node. The voltage amplification due to negative capacitance in this device is shown in Figure 3. We see that the internal gate voltage (0.8V) is almost double that of the applied external gate voltage (0.4V) due to the presence of negative capacitance.

The internal gate voltage controls the drain current and hence, the drain current for the same VDD (0.4V) is significantly higher (25 vs. 120 $\mu A/fin$) as shown in Figure 3. This amplification enables promising device level characteristics. The drain current is plotted in linear scale to focus on on-current comparison between baseline FET and NCFET. The same drive current as 0.8V baseline FET can be obtained in NCFET at reduced VDD (0.4V), offering dramatic power reduction advantages at the circuit and full-chip level. These are studied and discussed in detail in next sections.

IV. Full-Chip Design Flow

Figure 4 shows the design flow used in this study to implement full-chip GDSII designs from basic transistor models and design

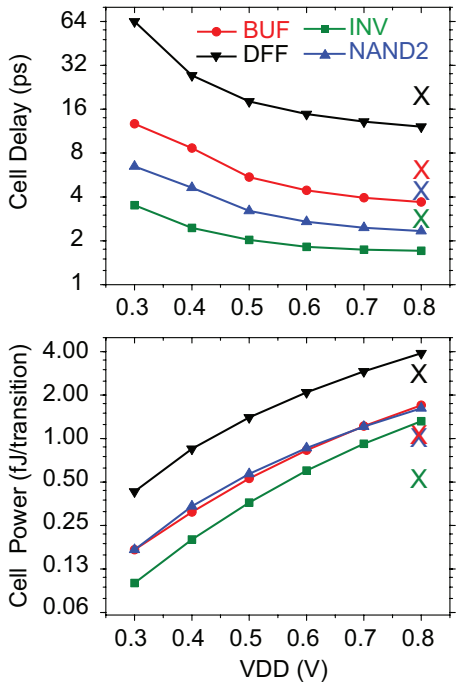

Fig. 5. Cell delay and cell power for NCFET-based cells. The colored X denotes the values for the respective baseline FET-based cells measured at VDD = 0.8V.

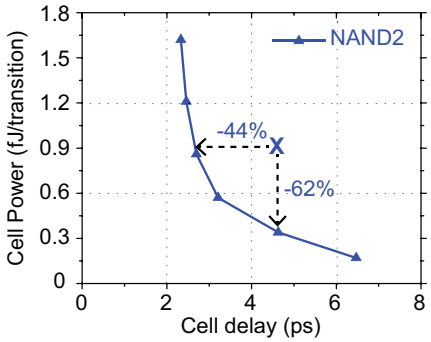

Fig. 6. Power vs. delay trade-off for NAND2 cell. NCFET offers 62% lower power at iso-performance and 44% faster performance at iso-power against the baseline FET (denoted X).

TABLE II
COMPARISON OF CELL INPUT CAPACITANCE (IN FF).

Cell	baseline FET (0.8V)	NCFET	
		0.8V	0.4V
Buffer	1.74	2.63 (+51%)	2.29 (+32%)
DFF (ck)	1.20	2.23 (+86%)	1.66 (+38%)
INV	1.72	2.64 (+53%)	2.29 (+33%)
NAND2	1.72	2.81 (+63%)	2.45 (+42%)

benchmark RTLs. We use state-of-the-art commercial design tools to implement our flow.

For full-chip layout with timing optimization and practical timing/power analysis including the parasitic information, we use Nangate15nm cell layouts for our study [11]. We use Synopsys Siliconsmart and Hspice to generate the power-delay look up tables (.lib files) for the standard cell layouts based on the device models, cell-netlists and the supply voltage. We obtain the cell timing/power libraries for NCFET at various voltages (at VDD = 0.3V - 0.8V in steps of 0.1V) and also for baseline FET (at VDD = 0.6V and 0.8V) for baseline comparison. We synthesize the gate-level verilog netlists for various benchmarks using their behavioral RTL and the timing/power libraries using Design Compiler. Then, we use the gate-level verilog netlist, cell timing/power library, cell physical information (LEF), timing constraints and qrcTech information to generate timing optimized GDSII design layouts using Cadence Innovus. We use Synopsys Primetime for timing and power analysis of the post-layout designs with the cell libraries and the extracted parasitic information to provide accurate practical analysis.

For our study, we use five different benchmarks from OpenCores. The summary of design benchmarks used is given in Table I. The smallest benchmark (itc99_b19) has approximately 64K cells while the largest benchmark (256-bit multiplier) has approximately 700K cells. The actual number of cells in the final layout implementation vary with the strength of the cell library used. The footprint of the designs are determined using an average placement utilization value of 70%. The use of a wide range of benchmarks helps us generalize the impact of NCFETs on power-performance of designs across all types and sizes.

V. LIBRARY CHARACTERIZATION

The impact of a new device technology on full chip power and performance is heavily dependent on the properties of the standard cell library characterized using the cell layouts and the device models. With multiple libraries characterized at different voltages for both NCFET and baseline FET, we compare and contrast the important metrics of delay, cell-internal power and input capacitance load offered by the cells.

Figure 5 shows the cell delay and cell power vs.voltage characteristics for four different standard cells with NCFET transistors. The corresponding values for baseline FET transistor based cells are also shown with 'X' at nominal VDD of 0.8V. From the delay plot, we observe that even at very low VDD of 0.4-0.5V, NCFET cell delays are comparable to baseline FET cells operating at nominal VDD. This is because of the higher on-current offered by NCFET devices. This is the single most important factor which enables us to reduce VDD and still maintain the same performance at the full-chip level. Flipflop has the largest delay (clk-q) among all cells and has the highest sensitivity to VDD change.

In terms of cell-internal power, Figure 5 shows that NCFET cells have higher internal power dissipation for the same 0.8V VDD due to higher drive current and increased internal capacitance. However, with reduced VDD, the energy reduces quadratically. For the same performance as baseline FET at 0.8V VDD, the NCFET cells show up to 4X power savings. This is the major factor which enables us to achieve dramatic power savings at iso-performance operation using NCFET based cells.

Another important characteristic of NCFET-based cells is the increase in input (load) capacitance which the cells offer to its driver cells. Table II compares the input capacitance of few standard cells. The capacitance reduces with lower VDD but NCFET cell capacitance is still higher than that of baseline FET cells. The input capacitance of NCFETs is higher than the baseline FETs because the negative capacitance of the ferroelectric layer in this device is in series with the positive baseline FET input capacitance. For two positive capacitance elements in series, equivalent capacitance reduces. However, with negative capacitance in series with the positive baseline FET capacitance, the equivalent capacitance increases. This

TABLE III
COMPARISON OF NCFET CELL LEAKAGE POWER (IN NW) AROUND VDD VALUES THAT SHOW A SIMILAR DELAY AS BASELINE FET.

Cell	baseline FET (0.8V)	NCFET		
		0.5V	0.4V	0.3V
Buffer	48.4	17.5 (-64%)	11.9 (-75%)	7.5 (-85%)
DFF	176.0	31.8 (-82%)	21.6 (-88%)	13.8 (-92%)
INV	45.2	17.4 (-62%)	11.8 (-74%)	7.9 (-83%)
NAND2	51.6	18.6 (-64%)	12.6 (-76%)	7.4 (-86%)

affects the overall power savings relative to the ideal power savings expected with VDD scaling.

Figure 6 shows the power-performance trade-off for one of the cells (NAND2). The amplification in on-current in NCFET enables 44% faster cell performance at the same power. Conversely, 62% power can be reduced for iso-performance cells. These are just based on cell characterization results for the NAND2 cell at moderate output load and slew values. Interconnect parasitics come into picture at the full-chip level and better drive current for NCFETs, even at reduced VDD, helps in achieving same performance as baseline FET based full chip designs. We exploit these characteristics of NCFET in full-chip level to lower supply VDD and obtain high power savings.

In addition to dynamic power, leakage power is also reduced with reduction in VDD. Table III shows the leakage power comparison of NCFET at voltage supplies which are good enough to match baseline FET cell delays at 0.8V. Leakage current reduces at low voltage due to reduced supply and reduction in drain induced barrier lowering. Flipflops with many transistors, including the clock-related transistors, show significant leakage savings of 88% at 0.4V and 92% at 0.3V supply. Leakage is a major component of total power in low power designs. These savings with NCFET cells at low voltage play a big role in reducing full-chip leakage power significantly without compromising performance.

VI. FULL-CHIP DESIGN STUDY

To understand the impact of new device technology at a full-chip level, we implement GDSII-based layouts and analyze them with the process discussed in Figure 4. First, we study the supply voltage dependence of a single benchmark using the NCFET libraries characterized for different voltages. The target is to reduce the supply voltage to the lowest allowable value while achieving the same high performance as the baseline FET based design. After identifying the lowest VDD value in NCFETs for iso-performance operation as baseline FET design, we study the power benefits on multiple benchmarks of varying sizes at this fixed low supply voltage and compare it with the reference baseline FET designs. We study the power benefits for both high frequency operation and low power, low frequency operation.

A. Impact of VDD on NCFET Designs

We used the advanced encryption standard (AES) core for our preliminary full-chip design study using NCFETs at different voltages. The design is targeted for 2 GHz operating frequency and uses up to six metal layers as per interconnect definition in the Nangate15nm. The first metal layer (M1) is reserved for intra-cell routing and is not used for inter-cell routing. Figure 7 shows the full chip GDSII layouts of AES designed with baseline FET and NCFET libraries.

Table IV shows the detailed results and comparison of design and power metrics for NCFET-based AES at different VDDs. Baseline FET numbers are also given for comparison. The supply VDD for NCFET are varied from 0.3V to 0.5V based on the on-current and

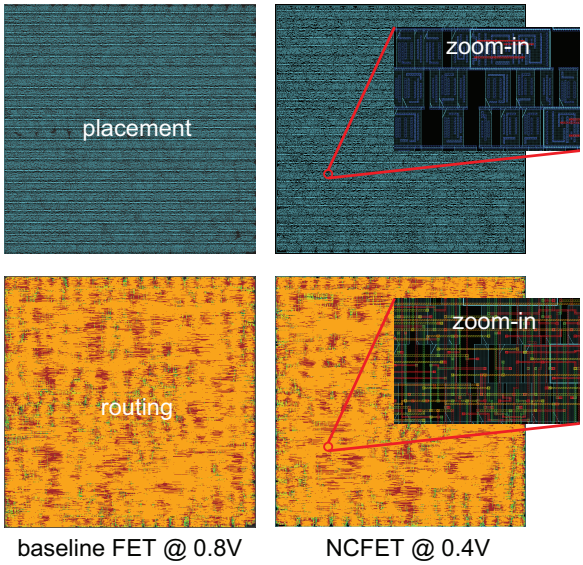

Fig. 7. GDSII layouts for AES benchmark. All our data is based on sign-off quality GDSII designs.

cell delay comparisons discussed earlier. It is important to note that full chip timing closure uses different number of cells and different cell sizes to achieve the targeted performance. Therefore, based on the strength of the cell library, final implementation numbers vary in the different designs. The worst negative slack (WNS) after timing analysis is also reported. The switching, internal and leakage power components are reported along with the total power. Here switching power includes the power dissipation due to switching of wires and cell input-caps i.e. the effective load cap seen by the drivers. Internal power includes the power dissipated inside the cell boundaries, due to switching of internal nodes and short-circuit (crowbar) current. It is directly taken from the power-timing library information based on the load and slew values. For all power analysis in this work, we set an average switching activity of 10%.

We observe that NCFET-based AES design operating at a low 0.4V meets the same performance as baseline FET AES at nominal 0.8V. Further reduction to 0.3V leads to timing failure and sharp increase in usage of cells and cell-area. This is because the tool tries to optimize the design to meet timing by upsizing cells and adding more buffers but fails to achieve a high-performance target. VDD value of 0.4V is good enough to just meet the target frequency set by the baseline design. The placement utilization (=cell area) increases due to additional optimization effort but timing is successfully met, while dramatically reducing power w.r.t. the nominal baseline FET designs.

The 0.4V NCFET-based design uses 9% more cell area than baseline design but the return on power savings (71% = 4X) is very significant. These savings directly follow VDD scaling, where ideal savings should be 75% for half supply voltage. The total savings are less than the ideal savings due to the increase in switching capacitance relative to baseline baseline FET design. This total capacitance increase is the other key observation which directly follows the discussion on cell characterization (Table II). Total capacitance is the summation of all wire cap and input cap of all cells. The total capacitance is almost 36% higher for the best case at VDD = 0.4V. This leads to higher switching power relative to the expected ideal savings with VDD scaling. Though the total capacitance reduces

TABLE IV
ISO-PERFORMANCE (2GHZ) AES DESIGNS USING NCFET AT VARIOUS VDD LEVELS. NOMINAL (0.8V) BASELINE FET IS GIVEN FOR REFERENCE.

Device	**VDD**	# Cells	Cell Area (mm^2)	Wirelength (m)	Total Cap (pF)	WNS (ps)	Power (mW)			
							Switching	Internal	Leakage	Total
baseline FET	**0.8V**	127,757	0.043	1.02	686.8	6.3	57.3	91.4	6.2	154.9
NCFET	**0.5V**	128,438	0.043	1.03	992.3 (+44%)	19.2	33.6	40.4	0.9	74.9 (-52%)
	0.4V	135,235	0.047	1.01	933.6 (+36%)	0.9	20.1	23.9	0.9	44.9 **(-71%)**
	0.3V	152,328	0.053	1.02	927.4 (+35%)	**-77.5**	10.5	12.9	0.8	24.2 (-84%)

with reduction in voltage, it is still very high compared to the total capacitance of the baseline FET design. However, with proper additional design effort, there is enough room to reduce the supply voltage to 0.4V and achieve almost 4X power savings at the same performance, even with increased load capacitance.

B. High Performance Applications

Based on the voltage-sweep analysis using AES design, we fix 0.4V as the supply voltage for high performance (GHz) designs using NCFETs for iso-performance comparison with baseline FET designs at 0.8V. We carry out full chip design comparison with the other four benchmarks. The results are tabulated in Table V. AES metrics are also included in this table. The design footprint and approximate gate count is given in Table I. The footprint is kept the same for the same benchmark implementation, but the gate-count varies based on the cell library used.

Our design sizes vary from 60K gates to 800K gates, and hence provide a general idea of NCFET benefits without any design bias. The target frequencies are set to be in GHz range in all cases, with the exact value determined by the baseline design and the cell to interconnect proportion in the benchmark implementations. All the benchmarks satisfy their respective target frequencies. High performance NCFET based standard cells are capable of achieving such high frequencies even at the lower voltage of 0.4V. On average, the cell delay of NCFET cells at 0.4V is slightly higher than that of baseline FET cells at 0.8V (Figure 5). This results in some extra design effort at the full-chip level which results in minor increase in cell area usage.The cell area is reported along with cell count to show the impact of upsizing cells. For example, in the largest multiplier design, many buffers are added in both the implementations. There are more cells in baseline FET design but the cell area is higher in the 0.4V NCFET design due to use of larger cells.

The major characteristic of any voltage scaling approach is that the relative power reduction is a strong function of the voltage scaling factor and mostly independent of the design being used. That is what we observe and validate across all the benchmarks. The total power reduction with 0.4V NCFET designs consistently lies within 70% to 73%. On average, the switching power savings are 62%, internal power savings are 75%, and leakage power savings are 85%. The relative switching power savings are lower due to increased full-chip total capacitance. As explained earlier, this is primarily because of the NCFET devices in the standard cells. The total capacitance of NCFET designs are 36%-46% higher than the baseline FET counterparts, but the reduced VDD enables such high power reduction. The switching power dissipation ($P = 0.5CV^2f$) should ideally reduce quadratically with VDD (=4X here), but the capacitance increases by 36-46% leading to the observed switching power savings of 62% (=2.7X).

Leakage power reduction is most significant with 85% average leakage savings across all benchmarks. This directly follows the cell leakage savings discussed in Section V. However all our designs are analyzed at room temperature and for high-performance operation, leakage component is very low (3-4%). The impact of leakage power savings is more prominent at low-voltage and low frequency operation where dynamic power component and leakage power component become comparable.

C. Low Power Applications

To study the impact of NCFET for low power designs and to demonstrate the impact of high leakage savings, we use the same five benchmarks and implement them at low 200MHz frequency. FinFETS are fast devices and for low frequency operation, a supply voltage of 0.8V is not necessary. Therefore, for a fair and realistic low power, low performance analysis, we reduce the baseline VDD for baseline FET to 0.6V and use the library characterized at this lower VDD. Likewise for NCFETs, we use the 0.3V library. The 0.3V library is not strong enough for GHz performance, but it is more than sufficient for low frequency designs. The results of the design implementations and the power comparison is shown in Table VI. The cell library strength is lowered for these designs. However, for a modest 200MHz frequency, the design effort is also lowered. This can be observed from the reduced cell usage in low-frequency designs as compared to high-frequency designs discussed earlier.

Dynamic power is directly proportional to operating frequency while leakage power is independent of frequency. Therefore, in low frequency designs, the leakage component is quite significant even at room temperature. The leakage power contribution in total power increases from 3-4% in high frequency designs to around 25-30% in low frequency designs. With the relative leakage power savings being the highest (85%) among all components, the overall power savings increases further for low frequency designs. For the different benchmarks, the power savings with 0.3V NCFET ranges from 73-75% relative to the 0.6V baseline FET designs. The total capacitance increase is also lesser due to the reduced VDD, leading to better switching power savings. All of these factor combine to increase the total power savings for low power operations.

VII. FUTURE DIRECTIONS

Low voltage near-threshold computing has been an active area of research with attractive energy efficiency, but the associated performance degradation is the major showstopper. With high performance low voltage NCFETs, low voltage designs need not compromise on performance. In addition, NCFET based designs offer opportunities for extensive dynamic voltage frequency scaling (DVFS) with wider range of power-performance options. This will make the system highly efficient. However, the physical design in such cases will need to address all extreme levels. While the existing CAD tools used can be directly used for NCFET-based designs, the standard cell layouts need to be optimized for best performance across all voltages. Also, the variation analysis and simulations need to be extensive. The presence of new materials in the transistor will introduce newer variation parameters which need to be included during characterization and design closure.

TABLE V
ISO-PERFORMANCE DESIGN AND POWER COMPARISON WITH NOMINAL (0.8V) BASELINE FET AND LOW-VDD (0.4V) NCFET.

Device	**VDD**	# Cells	Cell Area (mm^2)	Wirelength (m)	Total Cap (pF)	Power (mW)			
						Switching	Internal	Leakage	Total
itc99_b19 (1.4 GHz)									
baseline FET	**0.8V**	64,093	0.024	0.45	326.5	20.8	33.7	2.8	**57.3**
NCFET	**0.4V**	68,981	0.025	0.47	477.3 (+46%)	7.9 (-62%)	8.7 (-74%)	0.5 (-82%)	**17.1 (-70.2%)**
aes (2.0 GHz)									
baseline FET	**0.8V**	127,757	0.043	1.02	686.8	57.3	91.4	6.2	**154.9**
NCFET	**0.4V**	135,235	0.047	1.01	933.6 (+36%)	20.1 (-65%)	23.9 (-74%)	0.9 (-85%)	**44.9 (-71.0%)**
jpeg (1.6 GHz)									
baseline FET	**0.8V**	279,353	0.140	1.85	1412.3	160.0	331.8	14.7	**506.5**
NCFET	**0.4V**	293,578	0.144	1.82	2052.8 (+45%)	63.9 (-60%)	83.7 (-75%)	2.4 (-84%)	**150.0 (-70.4%)**
fft (1.6 GHz)									
baseline FET	**0.8V**	337,804	0.166	2.13	1676.0	163.4	494.2	19.8	**677.4**
NCFET	**0.4V**	338,358	0.166	2.18	2284.3 (+36%)	61.6 (-62%)	124.8 (-75%)	2.8 (-86%)	**189.2 (-72.1%)**
multiplier (1.0 GHz)									
baseline FET	**0.8V**	793,860	0.420	4.35	3537.2	323.0	896.5	48.8	**1268.3**
NCFET	**0.4V**	783,935	0.423	5.15	4918.6 (+39%)	118.6 (-63%)	223.2 (-75%)	6.5 (-87%)	**348.3 (-72.5%)**

TABLE VI
ISO-PERFORMANCE (200MHZ) COMPARISON OF LOW POWER, LOW FREQUENCY DESIGNS WITH VDD = 0.6V FOR BASELINE FET AND 0.3V FOR NCFET.

Device	**VDD**	# Cells	Cell Area (mm^2)	Wirelength (m)	Total Cap (pF)	Power (mW)			
						Switching	Internal	Leakage	Total
itc99_b19 (200 MHz)									
baseline FET	**0.6V**	63,928	0.024	0.45	303.3	1.55	2.04	1.51	**5.10**
NCFET	**0.3V**	63,047	0.024	0.45	368.0 (+21%)	0.48 (-69%)	0.58 (-72%)	0.27 (-82%)	**1.33 (-73.9%)**
aes (200 MHz)									
baseline FET	**0.6V**	128,089	0.043	0.98	642.9	3.00	3.96	3.44	**10.40**
NCFET	**0.3V**	134,745	0.047	0.99	793.9 (+23%)	0.93 (-69%)	1.15 (-71%)	0.55 (-84%)	**2.63 (-74.7%)**
jpeg (200 MHz)									
baseline FET	**0.6V**	272,445	0.139	1.76	1285.4	10.1	17.6	7.83	**35.53**
NCFET	**0.3V**	278,174	0.140	1.77	1622.5 (+26%)	3.45 (-66%)	4.97 (-72%)	1.39 (-82%)	**9.81 (-72.4%)**
fft (200 MHz)									
baseline FET	**0.6V**	166,932	0.166	2.07	1571.9	10.6	26.6	11.0	**48.20**
NCFET	**0.3V**	164,972	0.165	2.09	1901.0 (+21%)	3.43 (-68%)	7.52 (-72%)	1.79 (-84%)	**12.74 (-73.6%)**
multiplier (200 MHz)									
baseline FET	**0.6V**	679,188	0.396	3.53	2755.9	31.1	76.9	24.2	**132.2**
NCFET	**0.3V**	683,650	0.397	3.68	3499.8 (+27%)	10.0 (-68%)	22.1 (-71%)	3.65 (-85%)	**35.75 (-73.0%)**

Memory using NCFET devices is also very promising, enabling huge reduction in stand-by power at low VDD without compromising performance. Memory design and its impact on processors and SoCs are important next steps in NCFET-based circuit design research.

VIII. CONCLUSION

In our work, we demonstrated the huge full chip power savings offered by NCFET-based designs. Our results are based on commercial quality full-chip GDSII layouts using state-of-the-art RTL-GDSII design flow and containing hundreds of thousand of logic gates. We use accurate SPICE device models verified with measurement data for ferroelectric layer. NCFETs indeed offer much higher drive current compared to baseline FET at same voltages, enabling us to reduce supply voltage for iso-performance designs. We studied the impact of voltage scaling and observed greater than 70% power savings at iso-performance across all benchmarks, even with increased device capacitance. Leakage reduction is most significant and its impact is observed better for low-voltage-low-frequency designs. We also discussed design challenges and opportunities with NCFET devices. Negative capacitance FETs open up a feasible and highly attractive device technology to carry forward the semiconductor era beyond the scaling wall. They provide greater than one-node design benefits at the same technology node and with minimal fabrication overhead.

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