Monolithic 3D IC vs. TSV-based 3D IC in 14nm FinFET Technology

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***Abstract*—In this paper, we conduct a comprehensive design comparison of 2D ICs, monolithic 3D ICs and TSV-based 3D ICs using a silicon-validated 14nm FinFET foundry technology and commercial quality designs. Through full-chip layouts and sign-off analysis using commercial-grade tools, the potential of monolithic 3D IC is explored and validated in terms of power, performance and area against that of TSV-based 3D ICs and 2D ICs.**

I. Introduction

Monolithic 3D ICs (M3D) is enabled by sequential integration of device layers in the vertical direction [1]. With increased challenges in scaling device technology to below 10nm nodes, M3D is being carefully studied and evaluated as a feasible alternative to scaling or an extension to an existing technology node. Therefore, a feasible and attractive alternative to scaling of devices needs to provide overall benefits in terms of power and cost reduction.

TSVs are few micrometers in diameter and they have large pitch (30-50μm) and keep-out-zone (KOZ) requirements. In addition to that, they have large parasitic capacitance. With logic gate size scaling to less than 0.5μm^2 in 14nm technology nodes and below, such large TSVs will be beneficial only for coarse-partitioning for block-level or die-level memory-on-logic 3D IC designs. Monolithic Inter-Tier Vias (MIVs) are similar to metal-to-metal vias in dimensions and parasitics, enabling very fine-grained 3D partitioning.

II. Monolithic 3D IC vs. TSV 3D IC

Figure 1 shows the form factor comparison of 3D vias with logic gates of 14nm and 28nm NAND gates. The TSVs are actually aggressively sized to 2μm for mini-TSV and 5μm for TSV. A practical TSV diameter would be 5-10μm. Also the figure does not show the KOZ.

A. Design Methodology and Setup

We use OpenSPARC T2 single core design and implement it in 2D IC, TSV-based 3D IC and monolithic 3D IC using a foundry 14nm FinFET technology. For simple power and area comparison, all three design implementations are targeted for 1.5ns clock period (667MHz frequency) at typical operating conditions. TSV-based logic-on-logic 3D ICs cannot operate at very high frequencies due to large TSV parasitic impact. Figure 2 shows the layouts of the different implementations with a section of TSV and MIV placement enlarged. We designed the GDSII layouts for 2D IC using Cadence Innovus. All timing and power analysis is carried out using Synopsys PrimeTime. For 3D IC designs, we used specific design methodologies discussed below.

1) TSV 3D IC Design: TSVs are much larger compared to the 14nm logic gates. Therefore for practical and optimistic analysis, we aggressively sized the TSVs to 5μm and 2μm diameters and pitch of 15μm and 6μm, respectively. The extent of KOZ around a TSV is kept equal to its diameter. We used the methodology in [2] for TSV-based designs. To accommodate the large size of TSVs, we carry out area-unbalanced partitioning with global mincut, so that the TSVs are minimized and also planned in the die which has lesser number of cells (top-tier). The pitch and KOZ requirements for TSVs are honored by placement blockages around TSV pads (Figure 2). For 3D IC timing and power analysis, we use TSV RC as $[0.01\Omega, 20fF]$ and $[0.05\Omega, 3fF]$ for 5μm and 2μm TSVs respectively.

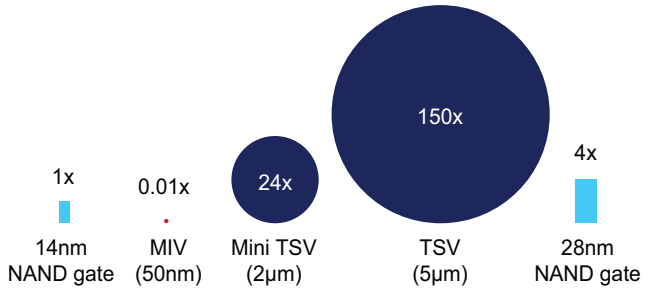

Fig. 1. Relative size comparison of 3D vias and NAND gates (14nm and 28nm). The diameter of monolithic inter-tier via (MIV) is $50nm$, mini TSV is $2\mu m$, and TSV is $5\mu m$.

2) Monolithic 3D IC Design: We use 'Shrunk2D' design flow [3] for monolithic 3D IC designs. In this technique, physical dimensions of all standard cells, interconnects and layout sizes are scaled by $1/\sqrt{2}$ to represent 50% footprint scaling but all electrical properties are kept the same. This is followed by regular placement, timing optimization and routing using commercial 2D IC tool. The next step is division of the 2D placement into different rectangular bins and then partitioning of cells into two tiers. Partitioning is followed by MIV planning by using a 3D metal stackup with cell pins defined in appropriate metal layers [3]. After tier-by-tier routing and interconnect parasitic extraction, the individual tier netlists, wire parasitics, MIV parasitics ($[10\Omega, 0.2fF]$) and top level 3D netlist is used in Primetime for timing and power analysis.

B. Full-Chip Design Comparisons

Table I shows the comparison of TSV 3D ICs and monolithic 3D IC in terms of area, wirelength, 3D interconnect overhead and power savings w.r.t. 2D IC implementation. Note that placement density for designs are similar with TSV designs having slightly higher utilization. Hence, the comparison of 3D via overhead is fair in terms of silicon area required for full design. Here placement density represents the portion of total silicon area used for logic gates, memory modules and 3D vias with their KOZ. It is clear that even optimistic TSV sizes result in area overhead for 14nm T2 core. Even with 996 and 1,839 TSVs, there is a 76% and 18% area overhead for 5μm and 2μm TSV 3D IC designs, respectively. Table I also shows the area overhead of the 3D vias and their KOZ. The 3D via and cell size comparison is magnified in Figure 2.

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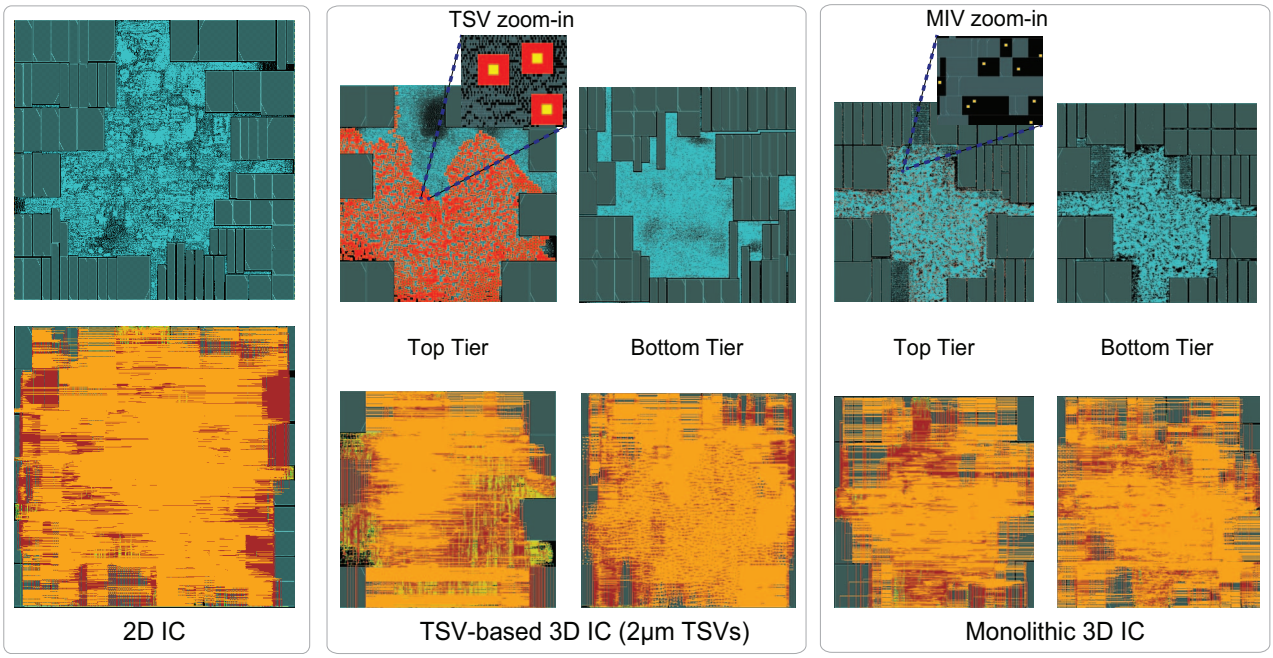

Fig. 2. Commercial quality GDSII layouts of OpenSPARC T2 single core using a foundry 14nm FinFET PDK. The footprints of 2D, mini TSV 3D, and monolithic 3D IC (M3D) are $585 \times 585\mu m$, $450 \times 450\mu m$, and $415 \times 415\mu m$, respectively. The red region around yellow TSV is the Keep-Out-Zone (KOZ). Note that we use a much deeper zoom-in in M3D to reveal MIVs, so cells shown in cyan colored rectangles appear larger than in TSV zoom-in.

TABLE I

AREA, 3D INTERCONNECT OVERHEAD, AND POWER COMPARISON OF THE DESIGNS SHOWN IN FIGURE 2. THE FREQUENCY OF OPERATION IS $667MHz$. THE NUMBERS IS PARENTHESIS ARE RELATIVE TO 2D IC VALUES. PLACEMENT DENSITY IN 3D ICS IS AVERAGE BETWEEN TWO TIERS AND INCLUDES AREA USED BY 3D VIAS.

		2D IC	TSV 3D IC ($5\mu m$)	TSV 3D IC ($2\mu m$)	Monolithic 3D IC
Footprint	(μm)	586×586	550×550 (-12%)	450×450 (-41%)	415 x 415 (-50%)
Silicon Area	(mm^2)	0.344	0.605 **(+76%)**	0.405 **(+18%)**	0.344 **(0%)**
Cell-utilized Area	(mm^2)	0.260	0.257 (-1%)	0.260 (0%)	0.258 (0%)
Total Wirelength	(m)	4.20	4.86 (+16%)	4.30 (+2%)	3.30 **(-21%)**
# 3D Vias		-	996	1,839	48,790
3D Via Pitch	(μm)	-	15	6	0.1
KOZ (around 3D Via)	(μm)	-	5	2	0
Area Overhead	(mm^2)	-	**0.241**	**0.069**	**0.001**
3D Via overhead %		-	**39.8%**	**17.0%**	**0.3%**
Placement Density		75.6%	82.1%	81.2%	75.8%
Wire Power	(mW)	**54.3**	62.5 (+15%)	53.1 (-2%)	43.4 **(-20%)**
Cell Pin Power	(mW)	**30.7**	30.4 (-1%)	31.3 (+2%)	29.1 **(-5%)**
Cell Internal Power	(mW)	**77.9**	77.0 (-1%)	80.8 (+4%)	75.4 **(-3%)**
Leakage Power	(mW)	**1.22**	1.15 (-6%)	1.22 (0%)	1.15 **(-6%)**
Total Power	(mW)	**164.1**	171.0 **(+4%)**	166.4 **(+1%)**	149.1 **(-9%)**

Due to less number of TSVs allowed (high area overhead), the wirelength reduction is not significant in TSV-designs compared to that in M3D and hence power savings are very low. Monolithic 3D IC implementation has 21% wire savings and 9% power savings over 2D ICs, most of which come from wire-power savings. Note that wire power savings are dependent on both wire capacitance and switching activity of the respective nets. The leakage is very low in all designs because power is analyzed at room temperature.

III. CONCLUSION

We studied the comparison of monolithic 3D ICs and TSV-based 3D ICs using a foundry 14nm FinFET PDK and demonstrated that fine-grained partitioning is not practical with TSVs due to huge size of 3D vias compared to logic gates. Though designs will continue to benefit in performance and I/O savings by using TSVs for die-level memory-on-logic or block-level folding, with few TSVs required. However, fine-grained partitioning in advanced nodes using current TSV technology is not practical. Monolithic 3D IC technology, on the other hand, provides true 3D IC benefits in the vertical direction.

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