Full Chip Impact Study of Power Delivery Network Designs in Gate-Level Monolithic 3-D ICs

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***Abstract*—In this paper, we present a comprehensive study on the impact of power delivery network (PDN) on full-chip wirelength, routability, power, and thermal effects in gate-level monolithic 3-D (M3-D) ICs across different technology nodes. Our studies show that PDN worsens routing congestion more severely in M3-D ICs than in 2-D designs due to the significant reduction in resources for 3-D connections. The relative impact worsens at advanced technology nodes due to higher congestion of interconnects. The increase in signal wirelength translates into additional net switching power dissipation, which significantly contributes to total power. This in turn aggravates thermal issues further in 3-D ICs. In addition, we observe that PDN tradeoffs among wirelength, power, and thermal are more pronounced in M3-D ICs than through silicon via-based 3-D and 2-D designs because of the higher integration density and the severe competition between signal and power connections. We also compare the impact of PDN on full chip routing in M3-D ICs versus face-to-face 3-D ICs. Lastly, we use various PDN design optimization techniques for M3-D ICs at different nodes and obtain up to 13.9% signal wirelength and 17.6% total power reduction under the given IR drop budget.**

***Index Terms*—3-D IC, monolithic, monolithic intertier via (MIV), power delivery network (PDN), routing congestion.**

I. Introduction

MONOLITHIC (M3-D) 3-D IC is an emerging technology which is enabled by sequential vertical integration of extremely thin device layers with very high alignment precision [1]. Unlike through silicon vias (TSVs), monolithic intertier vias (MIVs) are miniscule (<100 nm diameter) and can be used in large numbers within the design. This helps in high integration density allowing numerous 3-D connections which results in reduced wirelength, improved power and better performance [2], [3]. TSV-based 3-D ICs allow only limited number 3-D connections due to large TSV area and parasitics. MIVs on the other hand are similar to inter metal layer vias and have negligible capacitance ($\ll$1 fF) compared to TSVs and therefore improve the potential benefits in 3-D ICs.

In this paper, we study the impact of power delivery network (PDN) on M3-D IC design quality of results and discuss various PDN design techniques to reduce the adverse effects. The major contributions of this paper are as follows.

1) We study the impact of PDN in gate-level M3-D ICs designs. In particular we show that PDN affects M3-D ICs more severely than 2-D ICs in terms of wirelength increase and hence interconnect power increase (Section IV).
2) We analyze and compare the full chip impact of PDN on signal routing and power across three different technology nodes and study the increase in impact with advanced technology nodes (Section IV-B).
3) We compare the PDN impact on face-to-face (F2F) 3-D ICs versus sequential M3-D ICs (Section IV-C).
4) We study the thermal impact due to the presence of PDN in M3-D ICs and show that though PDN helps in improving lateral conductivity, the increase in power due to increased signal interconnect dampens this effect (Section V).
5) We study simple yet effective PDN design techniques to reduce its impact on wirelength and power increase without exceeding the IR drop budget (Section VI).
6) We propose efficient PDN design guidelines specific to M3-D ICs to help reduce its negative impact without exceeding the IR drop budget of a given circuit (Section VII).

We discuss the motivation and background in Section II and explain our design setup and analysis techniques in Section III.

II. Motivation and Background

The side-view of a typical two-tier monolithic sequential structure with seven metal layers in each tier is shown in Fig. 1. The device layer thickness is around 30 nm and the intertier dielectric (ILD) which separates different tiers is about 100 nm thick. The MIV diameter of <100 nm allows high integration density with significant wirelength reduction in M3-D. Note that the MIV connects the top metal of bottom tier to the bottom metal of the top tier.

A new emerging technology comes with new design challenges and issues which need to be first identified and then resolved to get maximum benefits. Gate-level M3-D ICs

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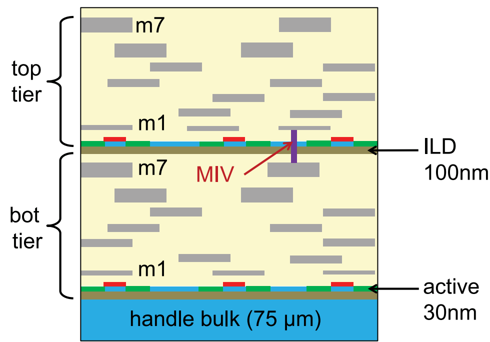


Fig. 1. Side-view of two-tier M3-D IC structure (with seven metal layers in each tier).

provide ultra high integration density but the stacking of dies increases the power density of the chip and also the current demand per unit area. This in turn complicates the cooling issues and the PDN design. Interconnects do not scale at the same rate as devices and the parasitic resistance of wires is higher at advance nodes [4], [5]. Therefore, interconnect impact worsens as devices become smaller. M3-D ICs helps in reducing the interconnect length significantly by allowing tens of thousands of 3-D MIVs. However, the presence of PDN reduces the routing resources and adversely affects the total signal wirelength. This impact is more severe in M3-D due to heavy usage of top metals for 3-D routing along with PDN routing. PDN is always important in any design, but due to sequential 3-D layers with very high integration density in M3-D, optimal PDN planning becomes much more critical.

Recent works focusing on power reduction benefits in gate-level M3-D ICs and related CAD methodologies [6], [7] do not address any thermal issues and totally ignore power delivery design and challenges. Wei *et al.* [8] have shown that PDN helps in reducing the temperature in M3-D ICs with an example of OpenSPARC T2 processor core. Though the presence of PDN helps in improving the thermal conductivity and reduces maximum temperature, they assume the same power dissipation of the blocks with or without PDN, ignoring its impact on increased congestion during signal routing. This congestion results in increased signal wirelength and hence increased net power, especially in advanced technology nodes. Also, their power simulation has been carried out at the architectural level and does not include parasitic impacts from full layout-extraction. In [9], we quantified the full chip impact of PDN in M3-D for the first time, with comparison to conventional 2-D ICs. Billoint *et al.* [10] further studied the impact of tungsten in bottom tier along with the presence of PDN in designs but their primary focus was development of CAD flow. Panth *et al.* [11] developed a tier-partitioning technique to handle power-delivery and thermal tradeoff in M3-D for mobile applications.

Some other 3-D PDN works focus only on TSV-based 3-D ICs or 3-D PDN simulation and analysis techniques. A 3-D IC floorplan and power-ground co-synthesis tool is developed in [12]. However, only block level floorplanning and power/ground design is considered for TSV-based 3-D designs. There is no discussion on the PDN inside the blocks. The total intrablock wirelength heavily dominates the total wirelength in any design. In other works, Luo *et al.* [13] have developed 3-D IC PDNs benchmark for research purposes. They have covered various sizes of 3-D designs but all of them are TSV-based and at the block level.

Full chip impact study of PDN design on M3-D ICs has not been studied much. With advancement of technology and scaling limits, gate-level M3-D ICs enable further extension with significant power and scaling benefits. Therefore, it is very important to study and understand all factors influencing M3-D technology, and develop methods to maximize the overall benefits, especially in advanced nodes.

III. Design and Analysis Setup

For this paper, we implement two benchmark circuits at three different technology nodes and analyze the PDN impact on physical design for 2-D and M3-D. The benchmarks used are: 1) OpenSPARC T2 single core [14] and 2) advanced encryption standard (AES) circuit [15]. We use 28 nm, 14 nm, and predictive 7 nm technology library for the design implementations and studies.

The 2-D physical design is carried out using standard RTL-GDSII flow in Cadence Encounter. The 3-D designs are first placed using the same tool in a 2-D fashion but with doubled capacity and then partitioned by placement driven partitioning [16]. Since, the focus of this paper is the impact of PDN on the full design, any good partitioning methodology [6], [10], [16] will suffice and the relative impact of similar PDN on signal wirelength will be same. MIV planning and insertion is carried out by stacking the individual tiers together into a single 3-D metal stack with appropriate cell-pin locations and then using Encounter nanoroute tool to get the via locations [6], [10], [16]. After 3-D placement and MIV planning, we perform tier by tier routing to get the final designs. We design two types of 2-D and 3-D designs with similar placement of cells, respectively. One is routed without any power or ground wires in the metal layers, while the other one has power/ground wires in the relevant metal layers. The circuits are designed to meet similar timing constraints in both 2-D and 3-D at the respective nodes and are therefore iso-performance designs. Power analysis is carried out on these iso-performance designs using Synopsys PrimeTime. Fig. 2 shows example layouts of the placement and routing of both tiers of T2 benchmark with 28 nm technology. Power/ground wires are not shown for clear view of signal routing.

A. Technology Scaling

Technology node is a major aspect that will affect the power benefits of M3-D and the impact of PDN. As per recent ITRS roadmap [17], interconnect scaling lags behind device scaling. Resistivity of copper wires increase rapidly at advanced nodes due to increased electron scattering at the grain boundaries and surfaces. At 7 nm, copper has 3.7× larger resistivity than 45 nm node. Therefore, it is imperative to study and analyze the impact of PDN on M3-D at future nodes as well.

Full process design kits (PDKs) for 45 and 28 nm are openly available for use in research. However, the new open-source

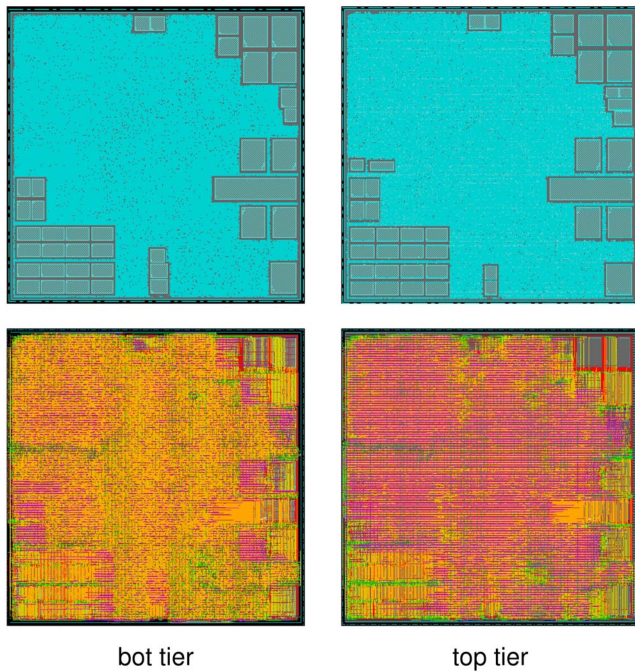


Fig. 2. OpenSPARC T2 layouts in M3-D. The top row is the placement/floorplan in each tier and the bottom row shows the overall signal net routing. PDN is not shown in routing for clarity.

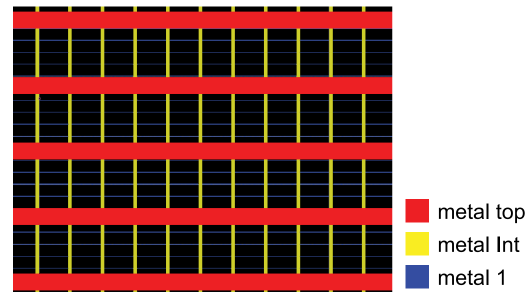
15 nm PDK [18] is not fully developed yet and lacks important information for full RTL-GDSII designs. In addition, there is no real 7 nm PDK available in any form. Therefore, for this paper, we build predictive libraries at 14 and 7 nm nodes for relative comparison based on Synopsys 28/32 nm PDK [19] and ITRS data (advancement of two and four nodes, respectively, relative to 28 nm node). Prior works [5], [20] have used ITRS-based scaled PDKs for their research studies.

The cell layouts are scaled as per ideal area-scaling ratio of 50% per technology node. Though this is optimistic scaling, it allows us to have direct relative comparison of PDN impact on signal routing and hence wire power across different technologies. Therefore, the same cell in 28 nm technology is 4× the size of 14 nm cell and 16× the size of 7 nm cell in terms of area. All cells are 11-track layouts, i.e., the height of the cell is 11× that of minimum metal1 pitch (as provided in 28 nm PDK). Transistor models are used from ASU-PTM [21] to obtain the new timing libraries for the 14 and 7 nm standard cells. The nominal voltages for 28, 14, and 7 nm PDKs are 1.05, 0.8, and 0.7 V, respectively. While 1.05 V is as provided in the 28 nm PDK, the other values are based on the transistor model data. The high input gate-capacitance and internal power of cells (relative to the expected reduction with scaling) of FinFETs used in post-16 nm nodes are accounted for in the 14 and 7 nm cell libraries.

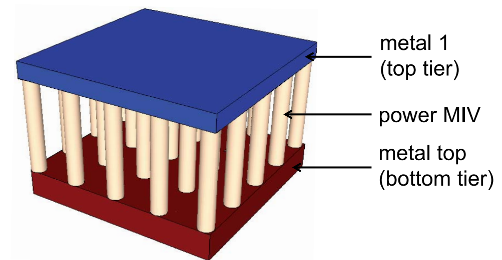
Table I shows the power-delay comparison of some basic cells in the three technology nodes. The libraries built for 14 and 7 nm closely follow the predictive technology trend in [4] and [5], where the authors have used 45 nm library as their reference. In this paper, we used 28 nm library [19] as the reference. For the new libraries, we generated new

TABLE I
POWER/DELAY COMPARISON OF BASIC CELLS (X1 SIZE) AT DIFFERENT NODES. (INPUT TRANSITION TIME = 32 ps, LOAD CAP = 1 fF)

		Cell Power (fJ)		Rise Delay (ps)		Fall Delay (ps)	
INV	28nm	0.350	(1.00)	5.79	(1.00)	6.01	(1.00)
	14nm	0.147	(0.42)	5.05	(0.87)	5.29	(0.88)
	7nm	0.054	(0.15)	4.63	(0.80)	4.71	(0.78)
NAND2	28nm	0.559	(1.00)	20.59	(1.00)	18.06	(1.00)
	14nm	0.252	(0.45)	17.12	(0.83)	15.89	(0.88)
	7nm	0.099	(0.18)	15.47	(0.75)	14.44	(0.80)
NOR2	28nm	0.606	(1.00)	21.69	(1.00)	23.35	(1.00)
	14nm	0.270	(0.45)	18.28	(0.84)	20.05	(0.86)
	7nm	0.117	(0.19)	15.35	(0.71)	17.68	(0.76)



(a)



(b)

Fig. 3. (a) Section of power/ground mesh structure. (b) Power MIV array at periphery.

interconnect technology files with extensive EM simulation using Cadence Techgen for use in accurate full chip layout parasitic extraction. RC parasitic values and material properties are based on ITRS projections [17]. While capacitance per unit length remains almost the same across nodes (~0.2 fF/μm) due to use of low-K dielectrics, the metal layers become severely resistive at advanced nodes due to the larger copper resistivity and the smaller metal width/thickness. But the length of nets also reduce, so the overall impact cannot be directly predicted without full chip design and analysis.

B. Power Delivery Network Designs

We use standard PDN design methodology which uses topmost metal layer for global wires and then intermediate metal layers to connect to the metal1 VDD and VSS rails [11]. Fig. 3(a) shows the PDN mesh layout structure. The density of power/ground wires is determined such that the maximum IR drop in 2-D designs is limited to 5% of the supply voltage (VDD). Similar PDN layout is maintained across all technologies with respective pitches/widths of metals and supply bumps. We use the same pitch of PDN wires in 2-D and 3-D

designs for the same technology and then perform full chip impact comparisons. It is to be noted that our benchmarks are parts of larger SoC designs and hence submodules or cores of a bigger design (e.g., T2 single core is one unit of 8-core T2). The power supply to such designs is delivered mostly through rings and stripes that are connected to the full SoC's PDN. These supplies are then distributed using the intramodule PDN. The C4 bumps in flip-chip designs supply power to the full SoC which in turn distributes it to these different modules through their rings. Therefore, in our analysis, we only provide input power/ground supply at periphery of the chips. Since we maintain the same relative density of PDN usage in both 2-D and M3-D designs, it gives a direct comparison on PDN impact. Addition of more power/ground inputs with same mesh will only improve the IR drop numbers in both 2-D and 3-D designs.

OpenSPARC T2 single core contains register-file modules which block up to metal4. Therefore, we use seven metal layers for full signal routing in T2. AES is a gate only design and relatively smaller and five metal layers are sufficient for full routing. These numbers are determined after performing experiments to verify the total routing requirement.

For T2 single core benchmark, metal7 is used for horizontal wires and metal4 for the intermediate vertical wires in the power/ground mesh. The preferred orientations are used as specified in the technology. 40% of the top metal and 20% of the intermediate metal is used for PDN. The top metal power/ground wires are made wider while the intermediate metal4 wires are relatively less wide. The frequency of occurrence of the wires are determined by the percentage usage as mentioned earlier and all the wires are placed equidistant from each other. The VDD and VSS cell rails run on metal1 cell rows as usual. For the AES design where five metal layers are used, metal5 is used for the horizontal power/ground wires. All the designs are circumscribed with VSS and VDD rings.

For 3-D designs, 3-D power ground connections are in the form of MIV arrays distributed along the periphery [Fig. 3(b)]. Since a single MIV is extremely thin, it offers very high resistance to the supply paths (~10 Ω). Therefore, an array of such MIVs is used for a single supply connection. We use 15×15 arrays (3×3 μm at 28 nm node). Such arrays are not placed inside the main area of the design because it consumes and blocks extra silicon area. Also reduced footprint in 3-D designs helps reduce path resistance from periphery to center.

We carry out full IR drop analysis using Cadence VoltageStorm. 3-D technology files are generated to allow the tool to carry out 3-D IR drop analysis. The 3-D technology file has the basic stack-up information of the two tiers of M3-D IC along with the vertical dimensions of the ILD and MIVs connecting the tiers. Current sources (cell locations) are placed at the respective metal1 rails of each tier and the full two-tier IR drop analysis is carried out. The values of the current sources are determined using the detailed cell-level power analysis with PrimeTime. For 3-D designs, it is always the tier farther from the external supplies that is affected most. In our case, the bottom tier of Fig. 1 shows maximum IR drop since it is away from the external power supply input which is on the top metal of top tier.

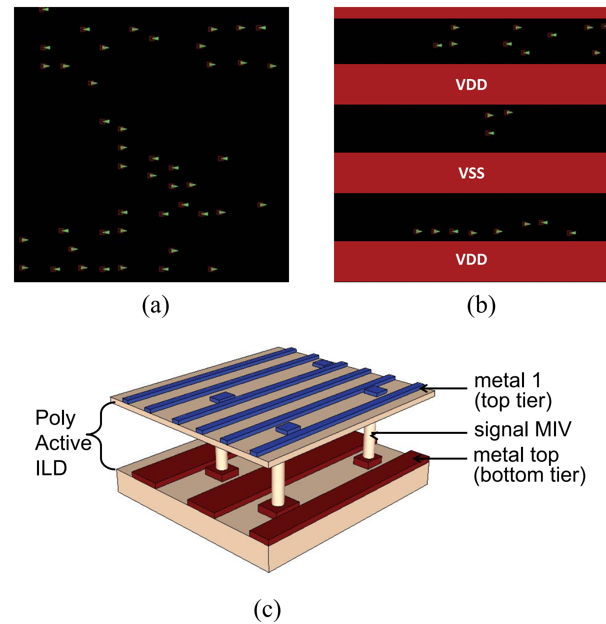


Fig. 4. Impact of PDN on MIV landing pads. (a) MIVs freely distributed without any PDN blockages in top metal. (b) PDN blockages affect MIVs in top metal. (c) Isometric view showing the constraints on signal MIV landing pad locations in top metal and metal1 of the next tier.

IV. New PDN Issues in Monolithic 3-D ICs

PDN with low max IR drop is an integral part of any digital circuit. In general, the top metal layer(s) is completely dedicated for power delivery depending on the number of supply voltages required for the design. Instead of having a long via-stack to metal1 VDD and VSS rails which connect directly to the standard cells, one or more intermediate metal layers are also used in between to redistribute the supply and reduce the resistive drop [11]. Because of the usage of these metals for PDN, there are less routing resources available for signal nets. This results in many detours for signal nets and hence increased wirelength. This increased wirelength and coupling results in more wire power dissipation.

A. *Impact of PDN*

Top metals are usually thick and wide and are not used for signal routing in traditional 2-D designs. Therefore, using a significant portion of these metal layers for power delivery does not affect the overall signal interconnect length. The other intermediate metal layers are not heavily used up by PDN (~20%) and therefore the overall impact, though present, is not extremely high. However, for 3-D designs, an important feature is that the top metal of the bottom tier is used for all 3-D signal connections (TSVs or MIVs) which connect to the metal1 landing pads of the next tier above. For very few 3-D connections, like in TSV-based 3-D designs, the presence of blockages in top metal is not very critical. On the other hand, M3-D ICs allow tens of thousands of 3-D MIVs and therefore face serious routing blockages when top metal is heavily used up for power delivery. Unavailability of continuous free routing area in these top metal layers results in heavy reduction in MIV count which reduce the 3-D benefits.

TABLE II

DETAILED COMPARISON OF IMPACT OF PDN ON 2-D IC AND M3-D IC DESIGNS FOR DIFFERENT TECHNOLOGY NODES. ALL $\Delta\%$ NUMBERS ARE EVALUATED RELATIVE TO THE RESPECTIVE WITHOUT PDN DESIGN

Benchmark	Design Style		Footprint (μm x μm)	# MIVs	Wirelength WL (m)	**Δ%**	Wire Power (mW)	**Δ%**	Cell-Pin Power (mW)	Cell-Internal Power (mW)	Total Power (mW)	**Δ%**
OpenSPARC T2 - Single Core	28nm node (0.667GHz)											
	2D	w/o PDN	1600 x 1600	-	17.89		273.2		185.2	169.2	754.3	
		w/ PDN			19.12	**+6.9%**	293.4	**+7.4%**	185.5	173.9	779.4	**+3.3%**
	3D	w/o PDN	1140 x 1140	140,546	15.33		212.6		157.9	159.0	642.9	
		w/ PDN		116,727	17.09	**+11.5%**	242.0	**+13.8%**	158.1	162.7	676.1	**+5.2%**
	14nm node (0.770GHz)											
	2D	w/o PDN	800 x 800	-	9.16		137.7		101.0	90.3	405.0	
		w/ PDN			10.13	**+10.6%**	162.5	**+18.0%**	100.6	95.9	435.0	**+7.4%**
	3D	w/o PDN	570 x 570	120,099	8.32		121.5		86.2	84.5	360.2	
		w/ PDN		107,371	9.91	**+19.1%**	161.5	**+32.9%**	85.8	90.8	406.1	**+12.7%**
	7nm node (1.000GHz)											
	2D	w/o PDN	400 x 400	-	4.59		108.3		57.5	55.2	268.7	
		w/ PDN			5.26	**+14.6%**	137.7	**+27.1%**	57.5	55.2	301.1	**+12.0%**
	3D	w/o PDN	285 x 285	121,022	4.16		96.2		49.2	49.3	240.0	
		w/ PDN		108,068	5.17	**+24.3%**	137.4	**+42.8%**	49.9	52.8	285.4	**+18.9%**
Advanced Encryption Standard (AES)	28nm node (1.250GHz)											
	2D	w/o PDN	750 x 750	-	3.64		92.3		77.4	63.6	247.0	
		w/ PDN			3.90	**+7.1%**	97.8	**+6.0%**	77.6	63.9	253.0	**+2.4%**
	3D	w/o PDN	540 x 540	57,442	3.02		64.4		78.7	65.7	222.5	
		w/ PDN		47,850	3.64	**+20.5%**	85.0	**+32.0%**	80.1	66.8	245.6	**+10.4%**
	14nm node (1.667GHz)											
	2D	w/o PDN	375 x 375	-	1.94		71.6		62.2	50.3	192.4	
		w/ PDN			2.09	**+7.7%**	79.6	**+11.2%**	62.5	50.8	201.1	**+4.5%**
	3D	w/o PDN	270 x 270	54,000	1.66		57.1		63.4	50.1	178.9	
		w/ PDN		42,543	2.02	**+21.7%**	74.6	**+30.6%**	64.9	51.8	199.7	**+11.6%**
	7nm node (2.778GHz)											
	2D	w/o PDN	188 x 188	-	0.97		63.2		37.9	29.1	135.7	
		w/ PDN			1.05	**+8.2%**	75.8	**+19.9%**	38.8	29.8	149.9	**+10.5%**
	3D	w/o PDN	135 x 135	67,169	0.81		51.9		37.9	29.0	124.3	
		w/ PDN		48,643	1.01	**+24.7%**	70.4	**+35.6%**	38.1	29.3	143.4	**+15.4%**

Fig. 4 shows the magnified view of top metal layer of a circuit designed with and without PDN. The same regions of the layout are shown in both Fig. 4(a) and (b). The presence of wide power and ground rails prohibits the MIVs from getting freely distributed as explained in Fig. 4(c).

B. PDN Impact Analysis Results

Table II shows the detailed results and comparison of the impact of PDNs on 2-D and M3-D designs. The total power in any digital IC includes cell-internal power, switching power and leakage power, as categorized during power analysis in PrimeTime. Switching power can be further divided into cell-pin and wire switching. Cell-pin switching is due to the input gate capacitance of the standard cells while wire switching is from signal interconnects. The individual components are shown in the table to highlight the PDN impact on signal routing power and also the overall power. Note that wirelength increase is not a direct measure of wire power increase because wire power also depends on the switching activity of the net. Fig. 5 highlights the relative increase in wire-power and total-power of both benchmarks at different technology nodes.

The OpenSPARC T2 single core has memory (register-file) modules and uses up to seven metal layers. Wire power along with leakage power is a significant portion of the total power. Due to the presence of PDN, the overall increase in power is higher at advanced technology nodes in both 2-D and 3-D designs. Since interconnect scaling lags behind device scaling, the interconnect impact is more severe at advanced nodes. This impact is much higher in 3-D ICs because the MIV locations are affected by presence of PDN in top metal of bottom tier. While the overall power increase due to PDN in 3-D T2 is 5% at 28 nm, it is as high as 19% at advanced 7 nm node. Fig. 6 shows the metal usage for signal routing of all the metal layers except metal1 in the bottom tier of M3-D T2 design at 28 nm. The bottom tier is critical because its top metal is used heavily for signal MIV insertion (Fig. 1). It can be clearly observed from Fig. 6 that due to the presence of PDN, the density of overall routing reduces significantly in metal4–metal7. While metal4 and metal7 have the actual power/ground mesh, the presence of PDN via arrays in metal5 and metal6 to connect these PDN wires prohibit continuous signal routing in these layers as well. This can be better visualized by observing the spaced routing in the bottom row of Fig. 6 compared to the continuous dense routing in the top row which has routing

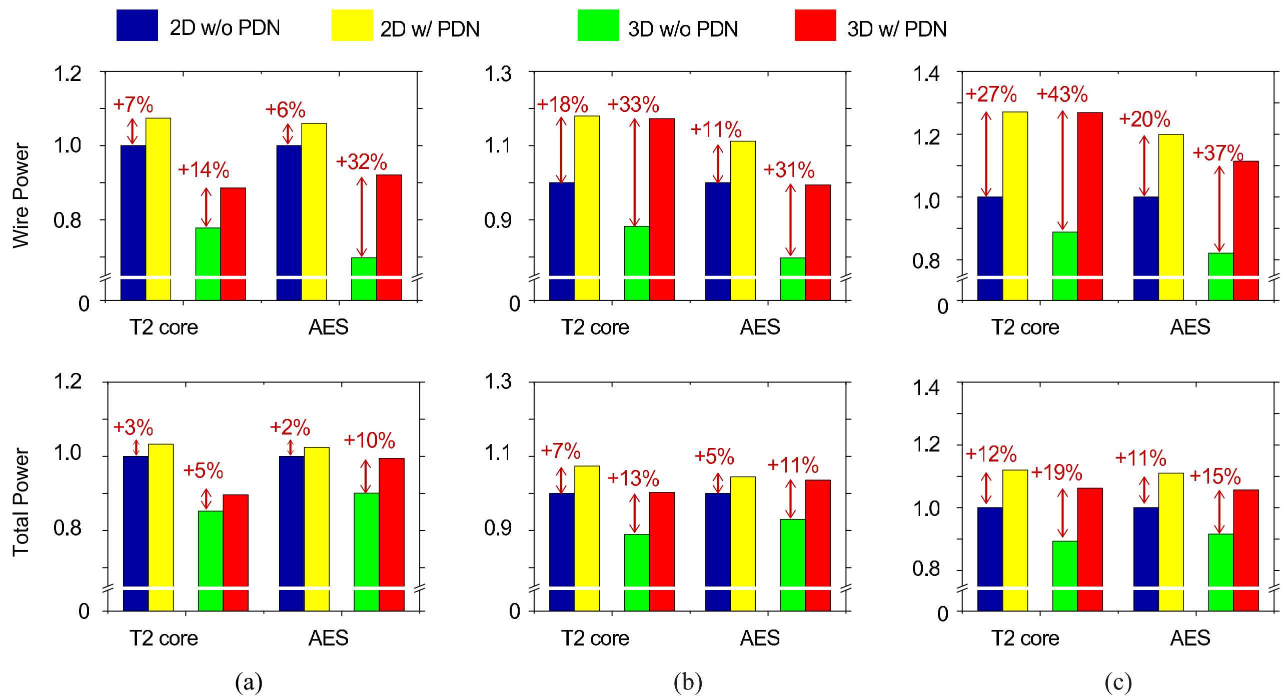


Fig. 5. Relative impact of PDN on wire power and total power of 2-D and M3-D designs at (a) 28 nm node, (b) 14 nm node, and (c) 7 nm node. All values are normalized with respect to 2-D without PDN. Note that the *y*-axis range is different at different nodes to accommodate the additional impact at advanced nodes.

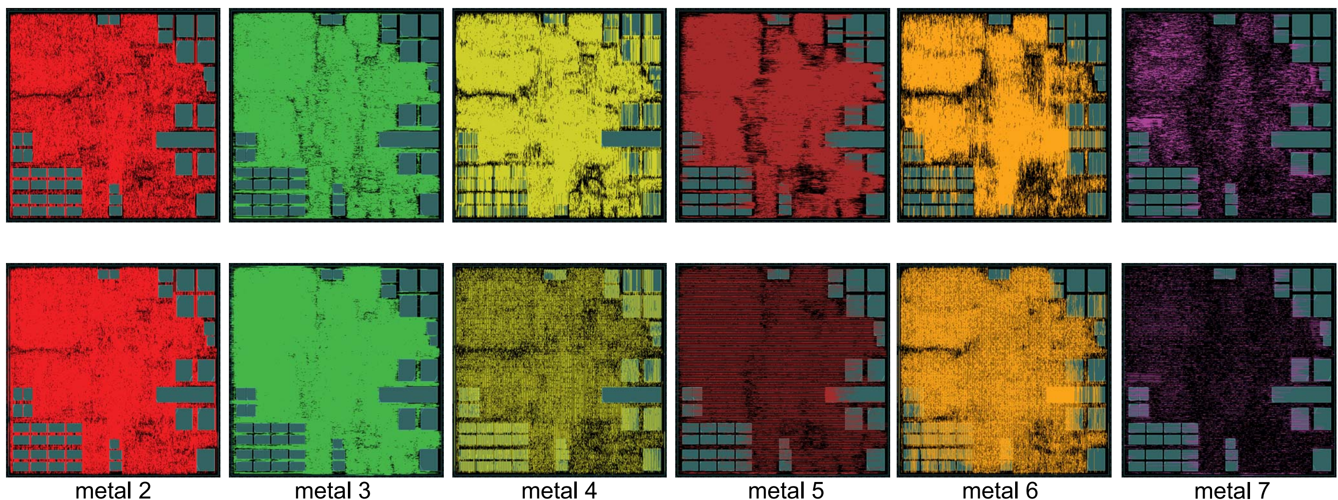


Fig. 6. Complete signal routing from metal2–metal7 in the bottom tier (tier with MIVs on top metal) of the two-tier monolithic T2 design. The top row shows the routing done without PDN blockages and the bottom row shows routing after PDN blockages.

completed without any PDN blockages. Though, the usage of metal2 and metal3 becomes much more in the designs with PDN blockages, it is not able to compensate for the loss in routing resources in the top metals and also result in increased coupling parasitics. Fig. 7 gives a closer look at the metal7 and metal4 layers with and without PDN blockages. The density of routing and the placement of MIVs can be clearly differentiated in the two cases.

AES is a pure logic circuit with no memory modules and uses five metal layers for signal routing. PDN impact on 3-D IC power compared to 2-D ICs is relatively higher than in T2 because fewer metal layers are used for routing and 3-D routing is more affected. The overall power increase due to presence of PDN in 3-D IC is 10% at 28 nm, 12% at 14 nm, and 15% at 7 nm. Interestingly, the relative degradation with advancement of technology is lesser in AES compared to T2. This is because T2 has memory modules and they block a lot of routing area. This additional factor has more severe impact at advanced nodes. AES does not have memory modules and therefore, only interconnect versus device scaling affects the degradation.

C. PDN Impact in F2F 3-D ICs

Since M3-D IC technology is still in the development stage, F2F stacking is being explored as an early qualified 3-D IC

TABLE III
PDN IMPACT ON F2F 3-D ICS

		Wirelength (m)	# F2F bumps	Wire Power (mW)	Cell-pin Power (mW)	Cell Internal Power (mW)	Total Power (mW)
T2 core	28nm node						
	w/o PDN	15.05	168,915	210.0	158.0	159.4	640.8
	w/ PDN	18.35 (+21.9%)	119,827	270.8 (+28.9%)	158.1	165.2	707.5 (+10.4%)
	14nm node						
	w/o PDN	7.54	181,506	118.6	85.9	82.8	355.3
	w/ PDN	11.88 (+57.5%)	113,702	175.9 (+48.3%)	85.7	93.8	423.5 (+26.3%)
	7nm node						
	w/o PDN	4.02	181,377	99.9	49.9	47.4	242.5
	w/ PDN	7.18 (+78.6%)	114,026	180.3 (+90.5%)	49.7	53.0	328.4 (+35.4%)
AES	28nm node						
	w/o PDN	2.94	82,983	63.1	78.6	63.6	219.1
	w/ PDN	3.63 (+23.5%)	57,604	97.1 (+53.9%)	78.9	70.3	260.1 (+18.7%)
	14nm node						
	w/o PDN	1.46	90,434	50.3	63.1	49.7	171.3
	w/ PDN	1.87 (+28.1%)	53,215	79.5 (+58.1%)	65.6	54.8	207.8 (+21.3%)
	7nm node						
	w/o PDN	0.71	93,207	41.8	37.8	28.2	110.3
	w/ PDN	0.93 (+31.0%)	62,921	67.5 (+61.5%)	37.9	29.8	140.7 (+27.6%)

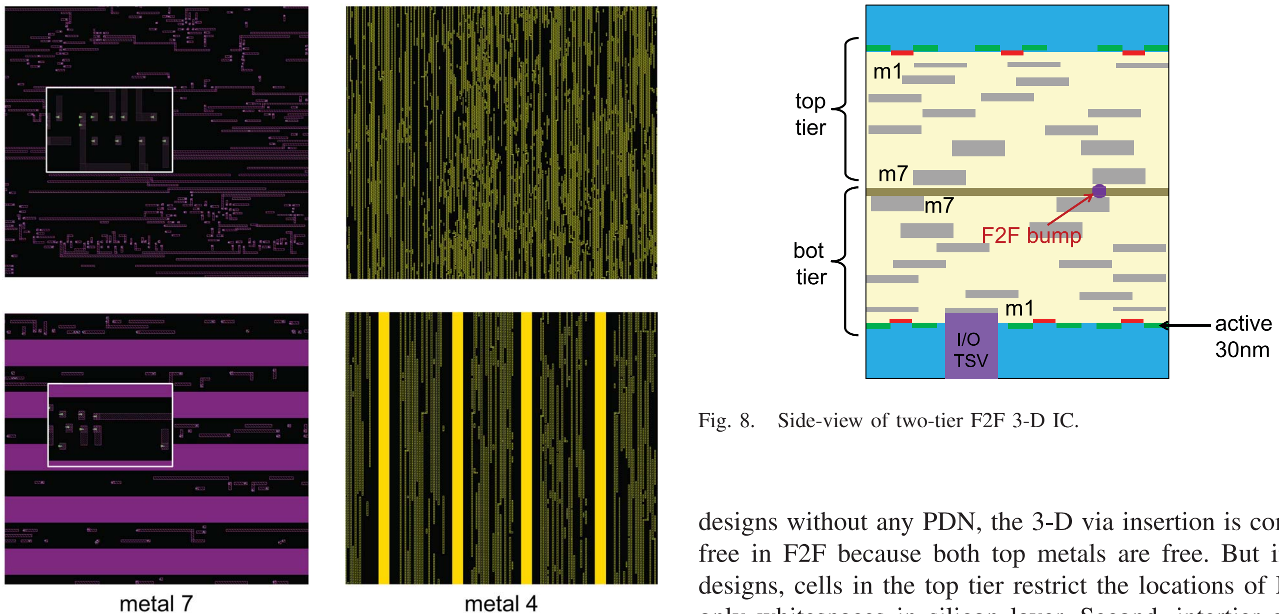


Fig. 7. Closer look at the signal routing in the metal layers with the PDN mesh. The top row shows the routing done without PDN blockages and the bottom row is routing with PDN (solid line) blockages.

Fig. 8. Side-view of two-tier F2F 3-D IC.

technology with high density 3-D interconnects. Fig. 8 shows the vertical structure of F2F 3-D ICs. In this technology, the top metal layers of both tiers are connected using μ-bumps. TSVs are used only for the external I/O connections. Both F2F and M3-D technologies enable high density 3-D connections unlike TSV-based 3-D ICs which has huge area overhead. Therefore, we also carry out comparison of PDN impact on F2F 3-D ICs for the design benchmarks at all three nodes. In our analysis, we assume the F2F pitch same as the top metal layer pitch [22].

Table III shows the comparison of 3-D F2F designs with and without PDN. There are two major important differences in terms of 3-D via usage in F2F and M3-D designs. First, for designs without any PDN, the 3-D via insertion is completely free in F2F because both top metals are free. But in M3-D designs, cells in the top tier restrict the locations of MIVs to only whitespaces in silicon layer. Second, intertier cell connections have to travel through 14 metal layers in F2F in contrast to seven metal layers in M3-D (ten and five metal layers, respectively, for AES). With the presence of PDN, F2F is affected more than M3-D because the PDN of both tiers impact the 3-D signal routing. PDN also includes the intermetal via connections and hence F2F designs have more such blockages for 3-D signal routing. In M3-D designs, only bottom tier PDN affects 3-D signal routing. Like M3-D designs, the wire power overhead and total power overhead due to PDN in F2F designs increase significantly at advanced technology with up to 35% extra power dissipation at 7 nm node.

Therefore, we clearly observe that power savings in M3-D ICs take a major hit with presence of PDN. The major difference in impact of PDN compared to 2-D comes from the top metal layer blockages, which reduces the 3-D connections and hence diminish the 3-D benefits. PDN is an integral part of design and we cannot ignore the severity of impact in M3-D compared to classical 2-D ICs. In the next sections, we focus

on the thermal impact of PDN and optimization techniques. We only focus on M3-D IC designs at 28 nm node. The same can be extended to advanced nodes as well.

V. Thermal Impact of Power Delivery Network

A. New Issues

Thermal issues have remained one of the major challenges of 3-D IC design. All the potential benefits which 3-D IC offers over 2-D designs in terms of power savings, wirelength reduction, footprint area reduction and increase in bandwidth are of no use if the chip temperatures are above tolerable limits.

The device layers are extremely thin in M3-D ICs and there is negligible lateral conductivity at the source of power dissipation. As discussed earlier, Wei *et al.* [8] demonstrated that the presence of thick PDN metal helps in improving the lateral conductivity and reducing the maximum temperature. However, the power simulations were done at architectural level and do not take into account the fact that PDN present in the individual modules increases the net switching power as demonstrated in the earlier section. This power rise offsets the conductivity enhancement brought about by the thick and wide power/ground wires. In this section, we re-establish the fact that PDN indeed helps in improving the temperature profile and reducing the maximum temperature, but the overall improvement compared to a no PDN design case is affected by the wire power increase due to increased signal wirelength and coupling.

B. Temperature Results and Discussion

We carry out detailed full chip thermal analysis with the help of ANSYS Fluent and supporting scripts to generate the required input files for Fluent [23]. Our thermal analysis tool considers all the layers in the technology and assigns conductivity to each individual tile of the 3-D mesh. A full GDS analysis is carried out to know the exact position of the active, poly and signal and PDN metal layers in each tier. For each tile, weighted conductivity is assigned depending on the materials which fall in that tile. For example, a tile may have some portion as SiO_2 and some portion as metal and the average conductivity is assigned based on the volume occupied by each material. Conventional heat sink and heat spreader are used on the side of the handle bulk (Fig. 1 in flip-chip). The power dissipation occurs only at the device layers of each tier. These power numbers are obtained for each individual cell using PrimeTime analysis.

We evaluate three different cases for our benchmarks at each technology node. The first case is the 3-D design which has no PDN. In the second case, we use the 3-D design with PDN and the corresponding power dissipation numbers, but we ignore the conductivity of the metal wires used for PDN. For the third case, we use the same design and power as the second case but now the PDN wires are included while assigning the conductivity values to each tile. We handle this by modifications to the post-routing GDS files. We use the second case to isolate the impact of PDN in conductivity.

TABLE IV
Thermal Analysis Results of the 3-D Designs. Maximum Temperature Values Are Reported (in °C). Room Temperature Is 27 °C. % Numbers Are Calculated With Respect to Rise Above Room in Without PDN Case

		w/o PDN	w/ PDN	
			w/o PDN conductivity	w/ PDN conductivity
T2 core	28nm	52.81	55.72 (**+11.3%**)	53.99 (**+4.6%**)
	14nm	65.7	71.52 (**+15.0%**)	67.59 (**+4.9%**)
	7nm	80.05	90.21 (**+18.9%**)	83.88 (**+7.2%**)
AES	28nm	58.7	63.89 (**+16.4%**)	62.04 (**+10.5%**)
	14nm	67.61	74.57 (**+17.1%**)	72.29 (**+11.5%**)
	7nm	83.85	95.60 (**+20.7%**)	91.47 (**+13.4%**)

Table IV shows the maximum temperature values for each of the evaluated cases at the different technology nodes. The maximum temperature occurs at the device layer away from the heat sink. The full tier temperature maps for these layers at 28 nm node are shown in Fig. 9. The cooler rectangular regions for the T2 temperature maps are the memory modules in the design which have lower power density compared to the rest of the design. On comparing the second and third columns in the figure, we observe that PDN indeed helps in improving the temperature profile by enhancing the lateral conductivity close to the device layers. This is in agreement with [8]. However, the situation is still worse than designs with no PDN in it. This can be explained easily by the fact that there is a power increase from 3-D without PDN to 3-D with PDN (Table II). The total power dissipation per unit footprint increases at advanced technology and therefore, the maximum temperature is higher. The relative power increase due to PDN impact is higher for 7 nm designs leading to higher increase in temperature even with PDN conductivity. Therefore, while PDN metal does play an important role in enhancement of conductivity, it is very important to include the additional impact of power increase because of PDN.

VI. Power Delivery Network Optimization

In this section, we explore different PDN designs in M3-D ICs to reduce its impact on 3-D signal routing. The maximum IR drop of the design has to remain within the specified budget while using any other power/ground layout. We use very simple yet effective changes to the existing PDN, which helps in providing more free areas for MIVs in the top metal, while keeping the IR drop under control. We utilize the fact that 3-D designs have 50% footprint compared to 2-D designs and hence distance from peripheral connections is lesser in 3-D. We specify the maximum allowed IR drop to be around 5% of the supply voltage, i.e., 50 mV for 28 nm PDK, 40 mV for 14 nm PDK, and 35 mV for 7 nm PDK.

A. Design Styles

Table V summarizes the various PDN design styles used for full chip impact analysis along with the percentage of metal layers used. The first modification we make is bringing the power and ground rails together instead of having

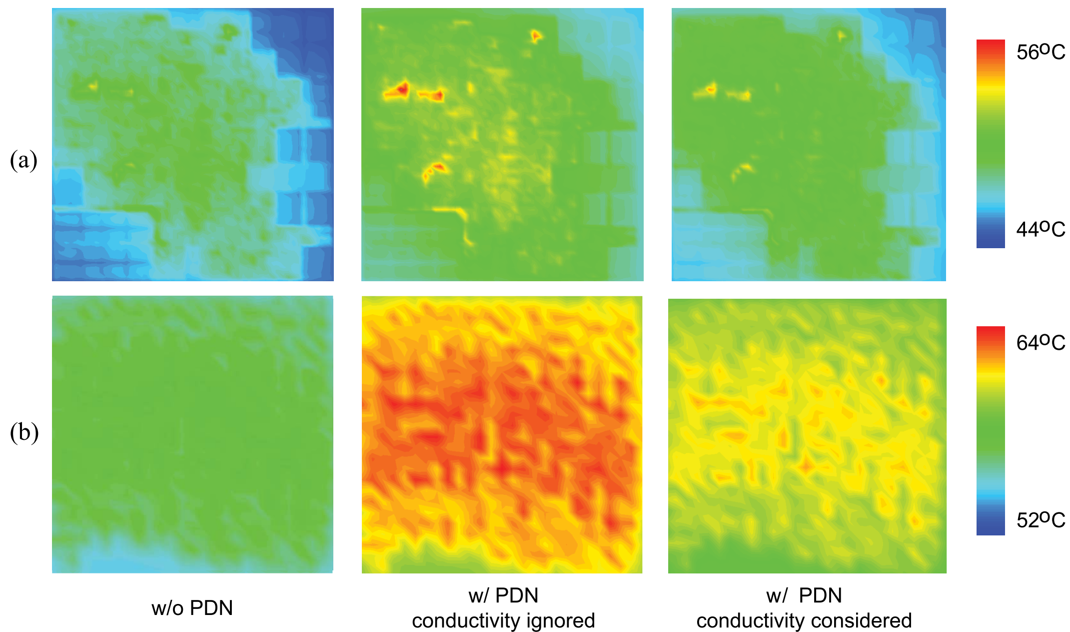


Fig. 9. Top tier (away from heat sink) temperature maps for (a) T2 design and (b) AES design. The actual dimensions are normalized. Note that the middle column is having the same power dissipation as the right column but does not consider the enhancement of conductivity because of PDN.

TABLE V
SUMMARY OF METAL USAGE IN THE VARIOUS ALTERNATIVE PDN DESIGNS (T2 BENCHMARK). ALL THESE CHANGES ARE DONE TO THE BOTTOM TIER ONLY, I.E., THE TIER WITH MIV LANDING PADS ON TOP METAL

PDN Design	Metal 7	Metal 6	Metal 5	Metal 4
baseline	40%	-	-	20%
modified	40%	-	-	20%
less topmetal	20%	-	-	20%
multiple metals	10%	10%	10%	20%
intermediate metals	Rings Only	-	40%	20%
no topmetal	Rings Only	-	-	20%

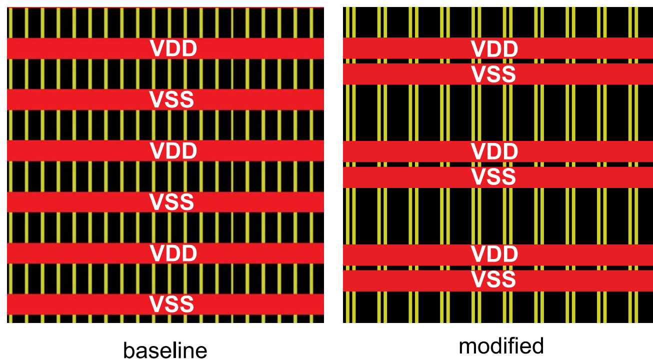


Fig. 10. Baseline PDN versus modified PDN. Note the extra continuous space between the red top metal wires which enhances MIV insertion and routing. The yellow wires are on intermediate metal.

all of them equally spaced. Fig. 10 explains this modification. The purpose is to provide more unblocked space for MIV routing and to avoid long detours. This technique is being used in advanced chip designs but is highly relevant for M3-D. By using this type of technique alone, we achieve wire power savings of 4.9%, 9.4%, and 19.9% in 28, 14, and 7 nm designs, respectively (Table VI). All other design styles discussed later use this modification. This technique can also be used in 2-D ICs, but it will not be as effective in bridging the wire power gap because very less top metal is used for signal routing anyways. The other design styles include reduction of top metal layer usage for PDN and compensation with PDN wires in other metals below. The design *less topmetal* reduces top metal usage to half that of the baseline. *Multiple metals* uses the metal layers between the top and intermediate metals used for the PDN in baseline. Only the intermediate metal layers are used in *intermediate metals*. They are connected to the input on top metal through rings only. The final case *no topmetal* uses only one intermediate metal layer for PDN and is connected to supply through rings in the top metal. Even though this is impractical PDN design from an IR drop perspective, nevertheless we implement it and study the full chip impact for comparison. Similar to earlier sections, we use PDN in metal4 as the common intermediate metal used across all design styles. T2 designs use metal7 as top metal while AES uses metal5 as top metal. Therefore, the design styles *multiple metals* and *intermediate metals* do not apply to the AES benchmark as metal4 and metal5 are continuous layers.

B. Full PDN Analysis Results

The full chip impact of the different power delivery design styles are summarized in Table VI. The baseline PDN of the design at the respective technology is treated as reference and all percentage numbers are reported with respect to this baseline. The impact of PDN on signal routing and power is worse at advanced nodes. Therefore, similar optimization techniques show greater benefits in 7 nm designs followed by 14 nm and then 28 nm designs. The wirelength and total power improvements are more pronounced in the AES benchmark than the T2 benchmark because it is gate-only design. A significant area of T2 is memory modules and related nets are not impacted much by changing PDN layout. Therefore,

TABLE VI
WIRELENGTH AND POWER COMPARISON OF VARIOUS OPTIMIZED 3-D PDN DESIGNS FOR DIFFERENT TECHNOLOGY NODES. THE FOOTPRINT AREA IS SAME FOR THE SAME BENCHMARK. THE % NUMBERS ARE EVALUATED WITH RESPECT TO THE BASELINE PDN

Benchmark	PDN Design Style	Wirelength (m)	No. of MIVs	Wire Power (mW)	Cell-Pin Power (mW)	Cell-Internal Power (mW)	Total Power (mW)	IR Drop (mV)	
								Maximum	Average
OpenSPARC T2 - Single Core	28nm node								
	baseline	17.09	116,727	242.0	158.1	162.7	676.1	29	15
	modified	16.86 (**-1.3%**)	118,121 (**+1.2%**)	239.9.0 (**-0.9%**)	158.1	162.7	673.3 (**-0.4%**)	29	15
	less topmetal	16.89 (**-1.1%**)	128,715 (**+10.3%**)	237.1 (**-2.0%**)	158.1	162.0	670.3 (**-0.8%**)	55	23
	multiplemetals	16.75 (**-2.0%**)	132,205 (**+13.3%**)	236.6 (**-2.2%**)	158.1	161.8	669.9 (**-0.9%**)	39	18
	intermediate metals	16.46 (**-3.7%**)	136,156 (**+16.7%**)	237.5 (**-1.9%**)	158.1	161.8	671.0 (**-0.8%**)	32	14
	no topmetal	16.08 (**-5.9%**)	137,173 (**+17.5%**)	225.7 (**-6.7%**)	158.1	160.7	657.8 (**-2.7%**)	214	46
	14nm node								
	baseline	9.91	107,371	161.5	85.8	90.8	406.1	25	14
	modified	9.75 (**-1.6%**)	108,048 (**+0.6%**)	149.8 (**-7.2%**)	85.8	88.0	391.6 (**-3.6%**)	25	14
	less topmetal	9.77 (**-1.4%**)	111,608 (**+3.9%**)	142.6 (**-11.7%**)	85.8	87.0	383.4 (**-5.6%**)	41	19
	multiplemetals	9.69 (**-2.2%**)	114,070 (**+6.2%**)	141.5 (**-12.4%**)	85.8	87.0	382.3 (**-5.9%**)	32	17
	intermediate metals	9.65 (**-2.6%**)	114,255 (**+6.4%**)	138.3 (**-14.4%**)	85.8	87.2	379.3 (**-6.6%**)	28	16
	no topmetal	9.28 (**-6.4%**)	121,245 (**+12.9%**)	127.3 (**-21.2%**)	85.8	85.4	366.5 (**-9.8%**)	146	44
	7nm node								
	baseline	5.17	108,068	137.4	49.9	52.8	285.4	22	12
	modified	5.02 (**-3.1%**)	108,292 (**+0.2%**)	119.1 (**-13.3%**)	49.9	48.6	262.9 (**-7.9%**)	22	12
	less topmetal	5.00 (**-3.3%**)	112,828 (**+4.4%**)	113.3 (**-17.5%**)	49.9	48.0	256.5 (**-10.1%**)	34	20
	multiplemetals	4.98 (**-3.7%**)	115,267 (**+13.3%**)	112.2 (**-18.3%**)	49.9	47.9	255.4 (**-10.5%**)	27	16
	intermediate metals	4.92 (**-4.8%**)	115,813 (**+7.2%**)	109.8 (**-20.1%**)	49.9	48.0	253.1 (**-11.3%**)	24	14
	no topmetal	4.64 (**-10.3%**)	123,081 (**+13.9%**)	100.5 (**-26.8%**)	49.9	47.1	242.9 (**-14.9%**)	118	28
Adv. Encryption Standard (AES)	28nm node								
	baseline	3.64	47,850	85.0	80.1	66.8	245.6	28	16
	modified	3.56 (**-2.2%**)	47,970 (**+0.3%**)	80.8 (**-4.9%**)	80.1	66.6	241.2 (**-1.8%**)	28	16
	less topmetal	3.35 (**-8.1%**)	55,311 (**+15.6%**)	73.0 (**-14.1%**)	80.1	66.3	233.1 (**-5.1%**)	45	17
	no topmetal	3.35 (**-8.1%**)	56,954 (**+19.0%**)	72.6 (**-14.6%**)	80.1	66.3	232.7 (**-5.3%**)	69	22
	14nm node								
	baseline	2.02	42,543	74.6	64.9	51.8	199.7	29	17
	modified	3.56 (**-2.2%**)	43,813 (**+0.6%**)	67.6 (**-9.4%**)	64.9	49.4	190.3 (**-4.7%**)	29	17
	less topmetal	1.81 (**-10.4%**)	51,213 (**+20.3%**)	59.5 (**-20.2%**)	64.9	48.9	181.5 (**-9.1%**)	42	18
	no topmetal	1.80 (**-10.9%**)	52,713 (**+23.9%**)	58.8 (**-21.1%**)	64.9	48.9	180.9 (**-9.4%**)	66	23
	7nm node								
	baseline	1.01	48,643	70.4	38.1	29.3	143.4	25	14
	modified	0.95 (**-5.9%**)	49,173 (**+1.1%**)	56.4 (**-19.9%**)	38.1	27.7	127.7 (**-10.9%**)	25	14
	less topmetal	0.87 (**-13.9%**)	61,210 (**+25.8%**)	46.8 (**-33.5%**)	38.1	27.8	118.2 (**-17.6%**)	36	16
	no topmetal	0.85 (**-15.8%**)	62,691 (**+28.9%**)	46.3 (**-34.2%**)	38.1	27.8	117.7 (**-17.9%**)	53	20

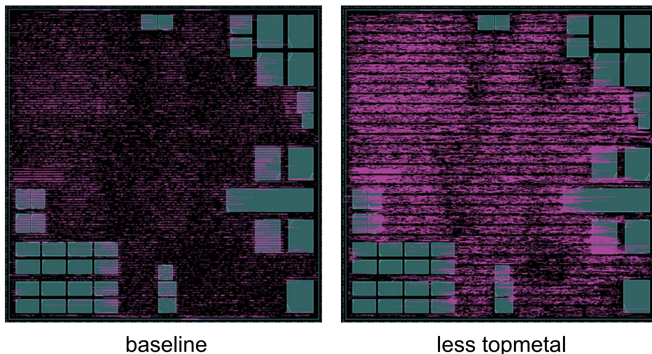


Fig. 11. Signal routing for top metal of bottom tier (T2 design) after reducing PDN wires along with clustering of VDD and VSS wires (*less topmetal* design).

the observed improvement in total power is not as high as in AES.

Fig. 11 shows the massive improvement in signal routing density in top metal of bottom tier when we allow more continuous space. Not only does it help in adding more vias, it also provides sufficient space for routing without unnecessary detours. The *less topmetal* design shows very good improvement especially in the AES benchmark. In 7 nm AES design, we save 17.6% power by reducing the density of PDN usage in top metal. For 7 nm T2 design case, *intermediate metals* case has maximum power savings of 11.3%. The *no topmetal* design shows best improvement. Though, it is attractive from power perspective, it is not practically feasible due to huge IR drop. The other design styles satisfy the IR drop requirement. The baseline and modified designs have similar IR drop values because the density of the PDN remains the same. Only the VDD and VSS wires come closer to each other. Since there is reduction in power, the maximum temperature reduces as well. Fig. 12 shows the AES design temperature maps for the tier away from the heat sink. The left map is the baseline and is same as the one shown earlier (in Fig. 9). The thermal map on right in Fig. 12 is the temperature map for the *less topmetal* design case.

VII. PDN DESIGN GUIDELINES FOR MONOLITHIC 3-D ICs

While designing PDN for M3-D ICs, the key is that the top metal of the lower tiers are heavily used for signal MIV landing pads and therefore cannot be fully utilized for PDN as done in regular 2-D designs. Therefore, the target is to reduce the usage of top metal for PDN in the lower tiers, i.e., tiers

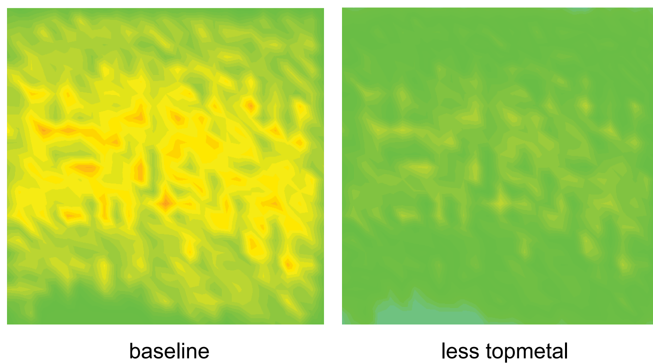


Fig. 12. AES top tier (away from heat sink) thermal maps for baseline PDN versus PDN design with less top metal used (at 28 nm node). The temperature scale is kept same as Fig. 9.

grown first in the fabrication process (Fig. 1). The proposed design guidelines are as follows.

1) The top metal needs to be given more free area for optimal MIV placement and therefore power/ground wires' density in top metal layers should be reduced. The PDN wires removed from top metal can be compensated by using resources in the metal layers below.
2) Different power/ground supply wires should clustered together and then these clusters equally spaced on the respective metal layers. This practice is already getting common but needs to be strictly followed in M3-D designs. It allows more continuous room for signal routing and MIV planning without affecting IR drop.
3) Depending on the footprint and the overall current demand, the pitch of PDN wires can be optimized to reduce the impact of PDN blockages on 3-D signal routing while satisfying the IR drop budget.
4) PDN needs to be designed much more carefully for interconnected dominated designs compared to cell/memory dominated designs because bad PDN affects signal routing and increases wire power.
5) PDN impact on signal power in M3-D is worse at advanced nodes and with technology scaling, PDN optimization becomes more critical for M3-D designs.

VIII. Conclusion

We studied the full chip impact of PDN in M3-D ICs in detail and demonstrated that the impact is more severe compared to simple 2-D designs. The issue becomes much more serious at advanced technology nodes. We also analyze the role of PDN in the full chip thermal behavior. As pointed out in earlier works, this paper re-establishes the fact that PDN does help in enhancing lateral thermal conductivity in M3-D IC and hence results in temperature reduction. But we also show that the increase in power dissipation due to increased signal wirelength must be taken into account for accurate temperature analysis, especially in M3-D designs where PDN has more impact. We demonstrate simple yet efficient PDN design styles for wirelength and power reduction. In this paper, we only focus on designs with single supply voltage. Many practical designs have multiple supply voltages and the top metals are heavily used for PDN layout. With the advent of M3-D IC, it is imperative to find better solutions for such multiple supply designs if we want to get the best benefits of 3-D over 2-D. This paper will serve as a starting reference for further optimization of PDN in such cases which will help in reducing the impact on signal routing and hence reduce power and maximum temperature.

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