Electrical Coupling of Monolithic 3-D Inverters

Yun Seop Yu, *Senior Member, IEEE*, Shreepad Panth, *Student Member, IEEE*, and Sung Kyu Lim, *Senior Member, IEEE*

***Abstract*— In this brief, we investigate the electrical coupling between stacked field-effect transistors (FETs) in monolithic 3-D inverters (M3INVs). We study the range of interlayer dielectric (ILD) thickness (T_{ILD}) and channel length L_g values that lead to a strong coupling between stacked FETs. Our device simulations show that M3INVs with $T_{ILD} \geq 50$ nm lead to negligible interaction between the stacked FETs. In addition, our 3-D mixed-mode circuit simulations show that the switching threshold voltages, propagation delays, and fall times of M3INVs with $T_{ILD} < 50$ nm are significantly affected by other tiers. This means that new circuit simulation techniques that consider the electrical coupling between the stacked devices are required in monolithic 3-D integrated circuits.**

***Index Terms*— 3-D integrated circuit (3-D IC), coupling, monolithic 3-D IC (M3IC), parasitic extraction.**

I. INTRODUCTION

3-D INTEGRATED circuits (ICs) have recently attracted considerable attention as a potential solution to the scaling trajectory predicted by Moore's law, as they reduce interconnect length [1]. Compared with the currently available through-silicon-via (TSV)-based 3-D ICs [2], monolithic 3-D IC (M3IC) [3]–[6] is a promising technology that enables ultrafine-grained vertical integration of devices and interconnections. Two or more layers can be stacked at the transistor scale and are connected vertically with nanoscale monolithic intertier vias (MIVs).

There have been extensive studies of process and device technologies for M3IC, but only a few design studies for memory and logic have been carried out [3]–[6]. There have been a few M3IC design flows developed which are different from those used to design 2-D ICs or TSV-based 3-D ICs [7]–[9]. However, existing work has ignored electrical coupling between stacked devices in M3IC circuit simulation and analysis. Conventional circuit simulators such as SPICE assume that the current–voltage (I–V) characteristics of a device are only affected by its neighbors through changes in their terminal voltages. This usually means that the interactions between adjacent devices can be neglected [10], and existing tools can be used to design M3IC.

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When the interlayer dielectric (ILD) is very thin (tens of nanometers), static random access memory and inverter circuits have been demonstrated to exhibit dynamic threshold voltage (V_{th}) modifications because of the electrical coupling between the stacked top and bottom metal–oxide–semiconductor field-effect transistors (MOSFETs) [11]. Accordingly, in order to investigate the possible influence of the bottom MOSFET bias condition on the top MOSFET performance, the threshold voltages of top MOSFET with a 32-nm gate length and only two types of ILD thicknesses (10 and 300 nm) were calculated using 2-D Technology Computer-Aided Design (TCAD) simulator when the gate bias of the bottom MOSFET changed [11]. However, the electrical coupling for various types of dimensions and parameters in M3IC has not been investigated. Therefore, in order to accurately design and analyze M3ICs with ultrathin ILDs, the regime where electrical coupling between the stacked FETs needs to be considered must be systematically investigated. In addition, it is also required to investigate how the dc/transient characteristics of M3ICs change according to the electrical coupling between their stacked FETs. The circuit simulation including the coupling can help design new types of M3ICs more exactly than that excluding it.

In this brief, the electrical coupling between the stacked FETs in a monolithic 3-D inverter (M3INV) will be investigated. The impact of the sizes of ILD and length of channel will be studied in terms of device characteristics (Section II). Next, in order to investigate how the dc/transient characteristics of M3ICs change with the amount of electrical coupling between their stacked MOSFETs, these characteristics of a M3INV will be studied with varying ILD thicknesses (Section III). Finally, Section IV will conclude this brief.

II. DEVICE COUPLING ANALYSIS IN M3INV

Fig. 1 shows the schematics of an M3INV structure. Fig. 1(a) shows the 3-D schematic of the M3INV, and Fig. 1(b) shows the cross section of A-A′ shown in Fig. 1(a). To compensate for the hole/electron mobility skew, the width of pMOSFET is larger than that of the corresponding nMOSFET. In order to accommodate this area skew, along with the extra space required for MIVs (or contacts), the pMOSFET and nMOSFET are placed at the bottom and top tiers, respectively [7]. Each MOSFET consists of the source (S)/drain (D) highly doped with 10^{21} cm^{-3} and lightly doped with 10^{18} cm^{-3}, the channel doped with 10^{15} cm^{-3}, the gate oxide (SiO_2), and the polysilicon gate (G). To study the electrical coupling in the M3INV, device parameters are used as shown in Table I, and especially, in line with the fully depleted silicon on insulator (FDSOI)

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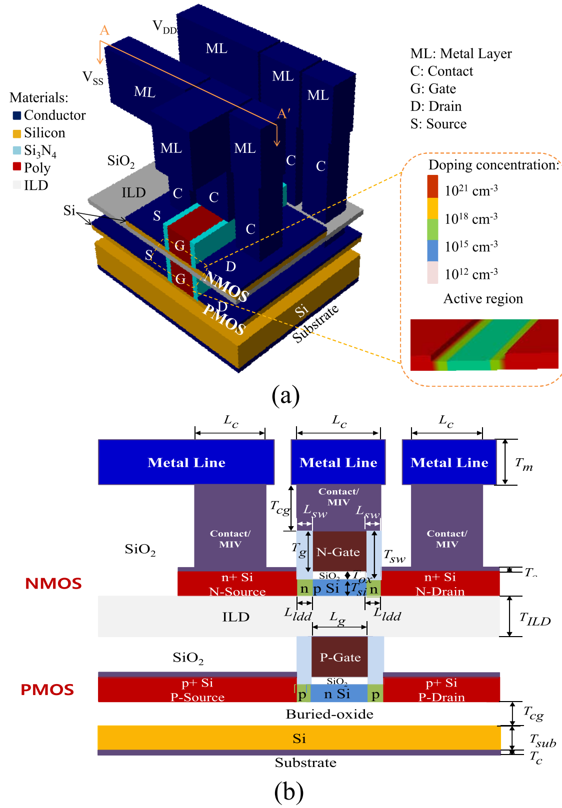

Fig. 1. Schematics of a monolithic 3-D inverter cell. (a) 3-D schematic. (b) Cross section of A-A′ in (a). ML, C, G, D, and S denote the metal layer, contact, gate, drain, and source, respectively. Materials in the structure and doping concentration in silicon body are classified with colors.

TABLE I
DEVICE PARAMETERS DIMENSIONS

Symbols	Description	Value
L_g	Gate length	variable
L_{sw}	Sidewall length	10 nm
L_{ldd}	Lightly-doped drain length	10 nm
L_c	Contact length	50 nm
T_g	Gate thickness	Same to L_g
T_{ox}	Gate-oxide thickness	variable
T_{si}	Silicon-channel thickness	variable
T_{sw}	Sidewall thickness	variable
T_{BOX}	Buried-oxide thickness	30 nm
T_{sub}	Silicon substrate thickness	50 nm
T_c	Contact thickness	6 nm
T_{ILD}	ILD thickness	variable
T_{cg}	Bottom gate contact thickness	100 nm
T_m	ML thickness	100 nm
ε_{ox}	Oxide dielectric constant	3.9
ε_{si}	Silicon dielectric constant	11.8
ε_{ILD}	ILD dielectric constant	variable

technology roadmap guidelines [1], [12], [13], $L_g(\approx T_g)$, T_{ox}, T_{si}, and $T_{\text{sw}}(=T_g+T_{\text{ox}})$ are varied, and T_{ILD} is also varied to investigate the coupling effect between tiers. Table II shows the electrical and performance parameters. The sources in the bottom and top MOSFETs are grounded. The drains in both the bottom and top MOSFETs are common ($V_{nds} = V_{pds}$) and can be operated as the output. The gates in the bottom and top MOSFETs are separately biased.

By using the 3-D TCAD simulator, ATLAS [14], the drain–source current (I_{nds}), transconductance ($g_m = dI_{nds}/dV_{ngs}$), gate capacitance (C_{ngng}) versus the gate voltage V_{ngs} of the top nMOSFET are simulated when the gate voltage V_{pgs} of the bottom pMOSFET is 0 and -1 V. The drain–source voltage V_{nds} of the top nMOSFET is biased as 0.1 V. A frequency $f = 1$ MHz is applied for transconductance and capacitance calculation. Three types of device configurations are considered as follows: the first one has $L_g = 50$ nm, $T_{\text{Si}} = 10$ nm, and $T_{\text{ox}} = 1.1$ nm, the next has $L_g = 30$ nm, $T_{\text{Si}} = 6$ nm, and $T_{\text{ox}} = 1$ nm, and the last has $L_g = 20$ nm, $T_{\text{Si}} = 6$ nm, and $T_{\text{ox}} = 0.9$ nm. In this structure, the electrical coupling of the bottom pMOSFET due to the gate of top nMOSFET can be ignored [11]. The electrical coupling of the top nMOSFET will be quantified when the gate of the bottom pMOSFET is biased at two different voltages (0 and -1 V). Fig. 2(a) and (b) shows ΔV_{th}, ΔV_{gm} (or ΔV_{Cngng}) versus T_{ILD}, respectively. When T_{ILD} is over 50 nm, and for current technologies where the gate length is below 30 nm, ΔV_{th}, ΔV_{gm}, and ΔV_{Cngng} are below 25 mV, and thus the coupling in the structures can be ignored. However, when T_{ILD} is below 50 nm, the coupling must be considered. As T_{ILD} decreases, ΔV_{th} increases, but as T_{ox} or T_{Si} decreases, ΔV_{th} decreases. These results are similar to the classical coupling relation of asymmetric double-gate fully depleted (FD) silicon on insulator (SOI) MOSFET due to the variation of back-gate voltage [see the lines in Fig. 2(a)], which is given by [15], [16]

$$\Delta V_{\text{th}} \approx \left(\frac{T_{\text{ox}}}{T_{\text{ILD}}}\right)\left(\frac{\varepsilon_{\text{ILD}}}{\varepsilon_{\text{ox}}}\right)\frac{\Delta V_{pgs}}{1+\left(\frac{\varepsilon_{\text{Si}}}{\varepsilon_{\text{ILD}}}\right)\left(\frac{T_{\text{ILD}}}{T_{\text{Si}}}\right)} \approx \left(\frac{T_{\text{ox}}}{T_{\text{ILD}}}\right)\left(\frac{\varepsilon_{\text{ILD}}}{\varepsilon_{\text{ox}}}\right)\Delta V_{pgs}. \quad (1)$$

In (1), the interface-trap charges are neglected and the back-gate voltage is the same as the gate voltage V_{pgs} of the bottom pMOSFET in this brief.

TABLE II
ELECTRICAL AND PERFORMANCE PARAMETER DESCRIPTION

Symbols	Description
V_{ngs}	Gate-source voltage of the top NMOSFET
V_{nds}	Drain-source voltage of the top NMOSFET
V_{pgs}	Gate-source voltage of the bottom PMOSFET
V_{pds}	Drain-source voltage of the bottom PMOSFET
I_{nds}	Drain-source current of the top NMOSFET
g_m	Transconductance of the top NMOSFET ($g_m = dI_{nds}/dV_{ngs}$)
C_{ngng}	Gate capacitance of the top NMOSFET
$V_{th(NMOS)}$	Threshold voltage* of the top NMOSFET
$V_{th(PMOS)}$	Threshold voltage* of the bottom PMOSFET
ΔV_{th}	Difference of V_{th}s of the top NMOSFET at between $V_{pgs} = 0$ and -1 V
ΔV_{gm}	Difference of V_{ngs}s at maximum g_m of the top NMOSFET at between $V_{pgs} = 0$ and -1 V
ΔV_{Cngng}	Difference of V_{ngs}s at maximum dC_{ngng}/dV_{ngs} of the top NMOSFET at between $V_{pgs} = 0$ and -1 V
V_M	Switching threshold voltage of the M3INV
t_{pHL}	Propagation delay for the high-to-low transition of the M3INV
t_f	Fall time of the output voltage of M3INV

*The threshold voltage V_{th} is defined as V_{ngs} when $I_{nds} = 10^{-7}$ A.

III. DC AND TRANSIENT ANALYSIS OF M3INV GATE

To investigate how its dc/transient characteristics change by electrical coupling between stacked devices in M3INV, the

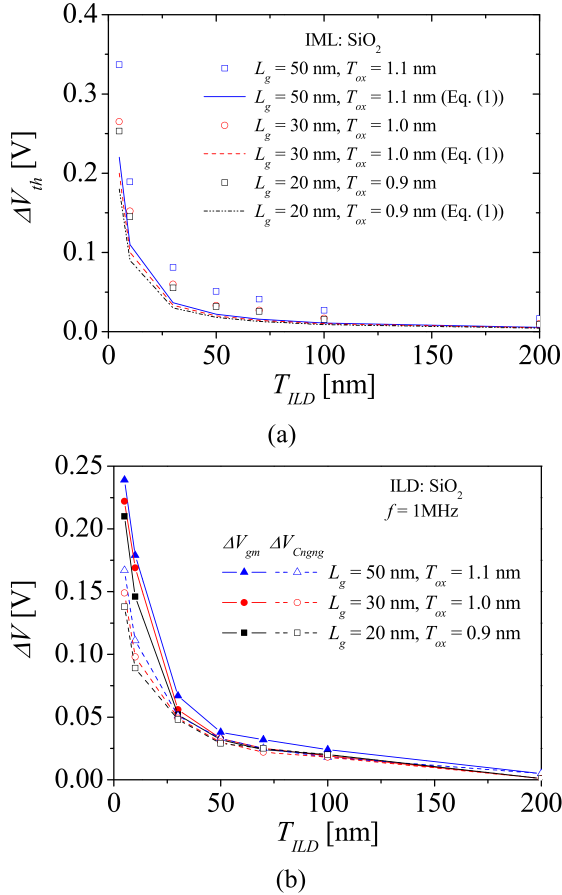

Fig. 2. (a) Threshold voltage shift and (b) top gate-voltage shift of transconductance (g_m) and transcapacitance (C_{ngng}) of the top transistor in the M3INV cell. Here, $V_{\text{ds}} = 0.1$ V, and frequency $f = 1$ MHz is applied for ac characterization.

3-D mixed-mode circuit simulation in ATLAS [14] is used. When there are no compact analytical models available for M3INV, it can be simulated with the mixed-mode simulation in ATLAS. Because an M3INV consists of two stacked devices that cannot be isolated electrically as shown in Section II, it must also be simulated as one device structure without separating two stacked devices by using the mixed-mode simulation in ATLAS. The M3INV is simulated with a 3-D device simulator at the determined bias, input voltage, and arbitrary output voltage, and then the I–V characteristics obtained from 3-D device simulation are applied to circuit simulation. Until the output voltage converges, the above procedure updating the output voltage is iterated. This mixed-mode simulation provides accurate descriptions of analog and digital circuits because the device characteristics with very high accuracy are obtained from the 3-D device simulator without using any compact models.

Fig. 3(a)–(c) shows the switching threshold voltage V_M, the propagation delay for the high-to-low transition t_{pHL} and fall time t_p of three types of M3INVs ($L_g = 20$, 30, and 50 nm). Here, the M3INV bias $V_{\text{DD}} = 1$ V, and output load capacitance $C_L = 1$ fF. The insets in Fig. 3(a) and (b) denote the voltage transfer characteristics and transient response of the M3INV cell ($L_g = 30$ nm, $T_{\text{Si}} = 6$ nm, and $T_{\text{ox}} = 1$ nm) with different T_{ILD}s, respectively. The insets

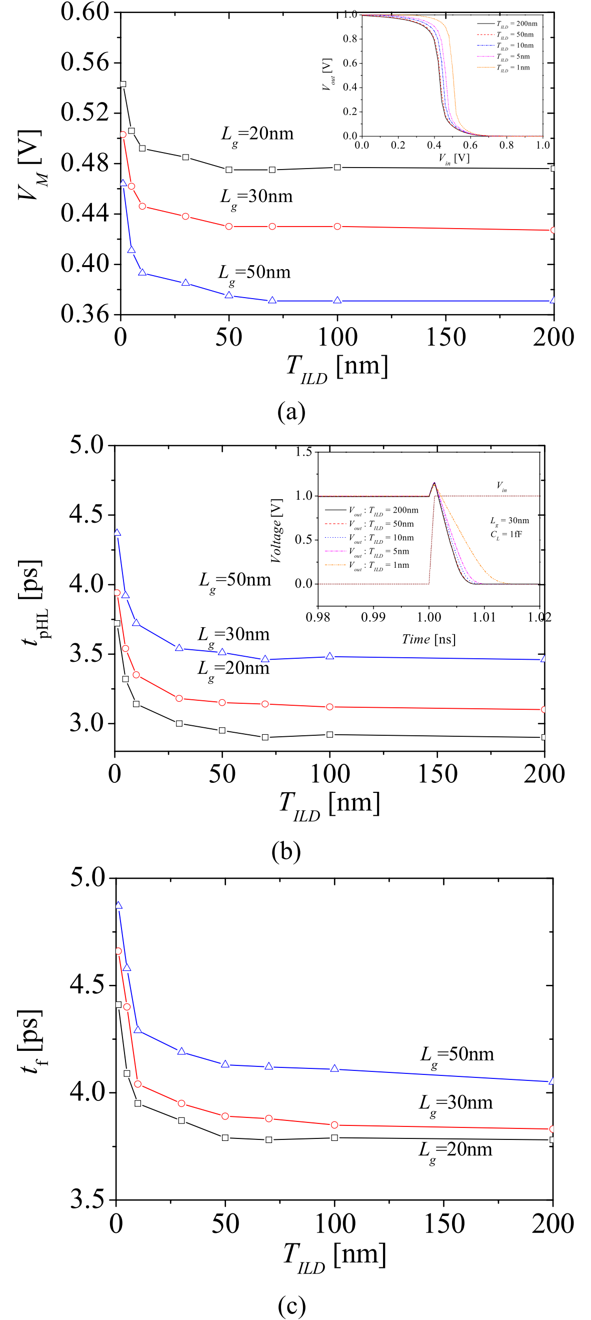

Fig. 3. Channel length dependence of the dc/transient response of M3INVs. (a) Switching threshold voltage V_M. (b) Propagation delay for the high-to-low transition t_{pHL}. (c) Fall time t_p. Squares, circles, and triangles denote the transient results of M3INVs with $L_g = 20$, 30, and 50 nm, respectively. The insets in (a) and (b) denote the voltage transfer characteristics and transient response of M3INV cell with $L_g = 30$ nm and different T_{ILD}s, respectively.

show typical inverter dc/transient characteristics. As T_{ILD} decreases, V_M, t_{pHL}, and t_f increase. When T_{ILD} is over 50 nm, V_M, t_{pHL}, and t_f are almost constant and thus the coupling in the structures can be ignored. However, when T_{ILD} is below 50 nm, V_M, t_{pHL}, and t_f increase rapidly and thus the coupling must be considered. V_M, t_{pHL}, and t_f are expressed as [17]

$$V_M = \frac{r(V_{\text{DD}} + V_{\text{th(pMOS)}}) + V_{\text{th(nMOS)}}}{1 + r} \tag{2}$$

$$t_{pHL} \approx \frac{C_L V_{\mathrm{DD}}}{\beta_n (V_{\mathrm{DD}} - V_{\mathrm{th(nMOS)}})^2} \tag{3}$$

$$t_f \approx \frac{C_L}{\beta_n (V_{\mathrm{DD}} - V_{\mathrm{th(nMOS)}})} \times \left\{ \frac{2(V_{\mathrm{th(nMOS)}} - 0.1 V_{\mathrm{DD}})}{V_{\mathrm{DD}} - V_{\mathrm{th(nMOS)}}} + \ln \left[19 - \frac{20 V_{\mathrm{th(nMOS)}}}{V_{\mathrm{DD}}} \right] \right\} \tag{4}$$

where r and β_n are process- and transistor size-dependent parameters, and $V_{\mathrm{th(pMOS)}}$ and $V_{\mathrm{th(nMOS)}}$ are the threshold voltages of pMOSFET and nMOSFET in the M3INV. Because $V_{\mathrm{th(pMOS)}}$ of the bottom pMOSFET is independent of $V_{n\mathrm{gs}}$ of the top nMOSFET but $V_{\mathrm{th(nMOS)}}$ of the top nMOSFET is dependent on $V_{p\mathrm{gs}}$ of the bottom pMOSFET in the M3INV (see Section II), V_M, t_{pHL}, and t_f are dependent on $V_{\mathrm{th(nMOS)}}$. When T_{ILD} decreases below 50 nm, ΔV_{th} increases drastically (see Fig. 2), and then $V_{\mathrm{th(nMOS)}}$ increases, and thus the increase in V_M, t_{pHL}, and t_f is relatively large (see Fig. 3).

IV. Conclusion

In this brief, we studied the electrical coupling between stacked MOSFETs in an M3INV and the impact of this coupling on the dc/transient characteristics of an M3INV circuit. To investigate the coupling between the stacked devices, the impact of channel length and thickness of ILD in the channel on the drain–source current, transconductance, and capacitances versus gate voltage curve of the bottom MOSFET in M3INV was simulated using a 3-D device simulator. If the M3INV has $T_{\mathrm{ILD}} \geq 50$ nm, we can neglect the interaction between the stacked MOSFETs.

Using a 3-D mixed-mode circuit simulation in ATLAS, the dc/transient characteristics of an M3INV are simulated to investigate the amount of coupling between stacked FETs. Because the switching threshold voltages, propagation delays, and fall times of each M3INV with $T_{\mathrm{ILD}} \geq 50$ nm are all almost identical, the coupling can be ignored, and each device in the M3INV can be isolated electrically. Thus, circuit simulation can use the SPICE SOI model [18], [19] for each device individually. In the case of M3INVs with $T_{\mathrm{ILD}} < 50$ nm, the coupling is relatively large, and new techniques may be required to simulate circuits consisting of coupled devices in conventional circuit simulators.

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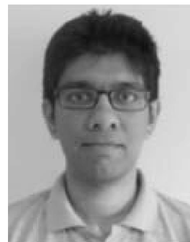

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