# Impact of Transistor Technology on Power Savings in Monolithic 3D ICs

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## ABSTRACT

In this paper, we discuss the impact of transistor technology on the power savings in monolithic 3D ICs over traditional 2D ICs. Our results are based on gate-level 3D IC partitioning and full RTL to GDSII design and analysis of a Low Density Parity Check (LDPC) benchmark circuit block with use of two different silicon validated foundry technologies. These two technologies have the same nominal operating voltage, but differ in terms of device performance, power, and gate capacitance. Our results show that monolithic 3D IC provides 37.5% more power savings for the technology with lower device power and input capacitance compared to that of a high power device technology.

## INTRODUCTION

Monolithic 3D IC (M3D) is an emerging technology enabled by sequential integration of device layers in the vertical direction. Gate-level monolithic 3D ICs provide significant power savings as well as potential cost savings over 2D ICs [1]. However, the magnitude of power savings of M3D is heavily dependent on the selection of device technology, process design kit (PDK), and the design benchmark circuit. In this work, we focus on the impact of transistor technology on 3D IC power savings.

Power in any digital integrated circuit can be divided into switching power, cell-internal power, and leakage power. Switching power can be further divided into switching of wires and switching of cell pins i.e. input gate capacitances of cells. Cell-internal power is the power dissipated inside of cells due to switching of internal node capacitances (excluding cell pins) and short circuit power during operation. Therefore, total power comprises of wire-switching power, cell-pin switching power, cell-internal power, and leakage power. M3D implementation helps in significantly reducing wire length and hence wire-power due to footprint reduction compared to 2D ICs. In addition, there is cell savings in terms of lesser timing buffer usage and use of smaller cell sizes because of reduction in back-end loading. The weighted sum of savings in these different power components contribute to the total M3D power savings.

## TECHNOLOGY DETAILS

We use two different silicon validated Foundry PDKs for our design study with LDPC (Figure 1). Both the technologies have a nominal operating voltage of 0.8V. We name them as Technology 1 and Technology 2, respectively, and use Technology 1 as the baseline during normalized comparison. Figure 2A and 2B show the power consumption and stage delay, respectively, of a minimum size inverter chain with fan out of 3. At the nominal voltage, Technology 2 consumes just 0.3x power of Technology 1 but is 2.7x times slower. Therefore, Technology 1 has higher drive strength but very high cell-internal power. The slopes of the curves in Figure 2B are also different indicating that the threshold voltage of Technology 2 is higher and therefore delay increases sharply with reduction in supply voltage. Figure 2C compares the input pin capacitance of three different standard cells of different drivability in the two technologies. Technology 2 has 35% lower pin capacitance compared to Technology 1. The contribution of interconnect vs. cell power in a digital integrated circuit is heavily dependent on these factors. In summary, Technology 1 has higher performance, higher power, and higher input pin capacitance, while Technology 2 is a low power technology, with relatively lower input pin capacitance.

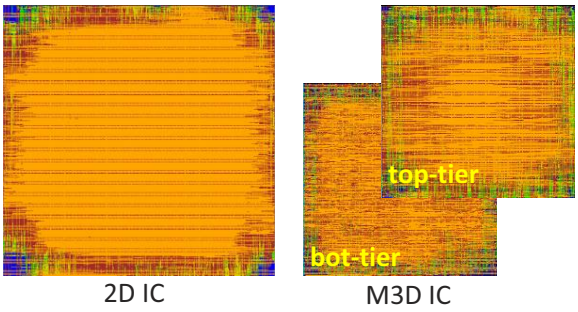


FIGURE 1: LDPC LAYOUTS W/ TECHNOLOGY 1

## RESULTS AND DISCUSSION

### *Design Methodology*

Our study and comparison is based on full RTL-GDSII design and analysis of interconnect dominated Low Density Parity Check (LDPC) benchmark. We use the gate-level monolithic 3D IC design methodology discussed in [2]. Both 2D and M3D designs are targeted for iso-frequency operation in the respective technologies and the relative savings in M3D are compared.

### *Power Comparison across Technologies*

Table 1 summarizes power in LDPC benchmark designed with these two different technologies. The power numbers are normalized w.r.t. the total 2D IC power in each technology. Figure 3A shows the contribution of the various components to the total power. As discussed earlier, Technology 1 has higher cell-internal power and higher cell pin capacitance. Therefore, cell internal power has highest contribution and switching of cell pins also add significantly to total power. It is to be noted that LDPC is interconnect dominated circuit. Nevertheless, cell-internal power still has maximum contribution in Technology 1. In contrast, Technology 2 has lower cell power and lower pin capacitance of cells. This not only increases the portion of wire power in total power, but also needs more timing buffers to satisfy timing constraints. The number of additional buffers required is higher in Technology 2, because the cells have relatively lower drive strength compared to Technology 1. As a consequence, the impact of reduction in interconnect length is expected to have higher impact in Technology 2 compared to that in Technology 1.

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TABLE 1: POWER COMPARISON

| Power Component | Technology 1 | | Technology 2 | |
|---|---|---|---|---|
| | 2D IC | M3D IC | 2D IC | M3D IC |
| Wire switching | 0.36 | 0.26 | 0.43 | 0.26 |
| Cell-pin switching | 0.27 | 0.21 | 0.25 | 0.17 |
| Cell-internal | 0.37 | 0.29 | 0.31 | 0.23 |
| Total | 1 | 0.76 | 1 | 0.67 |

*Monolithic 3D IC Savings*

Figure 3B and 3C show the detailed comparison of savings obtained in monolithic 3D ICs in the two different technologies in terms of capacitance and power. Firstly, Technology 1 has stronger cells and therefore, impact of interconnect on number of timing buffers and total power is less than that of Technology 2. The reduction of interconnect in M3D IC also has lesser impact in Technology 1 compared to Technology 2. Secondly, the input pin capacitance of cells in Technology 1 is much higher than that of Technology 2. Therefore, functional logic without any buffers has much more power contribution in Technology 1. As a result, the buffer and cell size savings in Technology 1 are less than that of Technology 2.

Relative wire length reduction due to footprint shrink is similar for both technologies. However, the reduction of higher number of cells in M3D IC in Technology 2 results in further reduction of number of nets and wire length. This results in additional wire-switching power savings in Technology 2 (39% in Technology 2 vs. 28% in Technology 1).

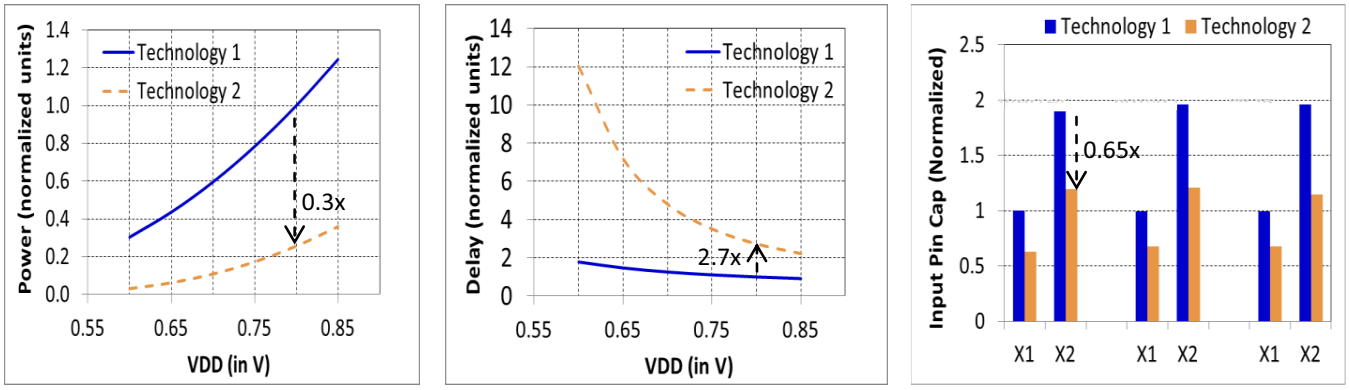
## CONCLUSION

We quantitatively compared the power savings in monolithic 3D ICs using two different foundry technologies with full RTL-GDSII layouts. Monolithic 3D ICs offer significant power savings in both the technologies but the benefits are higher in the technology with lower cell power contribution and smaller input pin cell capacitance. We observe 33% power savings in Technology 2 compared to 24% in Technology 1 in LDPC benchmark. M3D design in Technology 2 demonstrates higher savings both in cell and wire power.

## REFERENCES

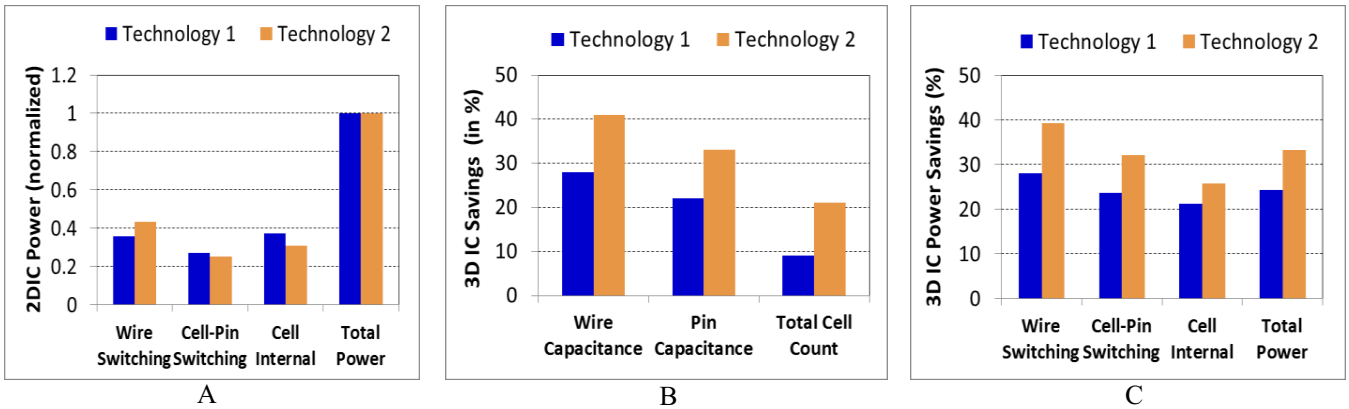
[1] D. Nayak et al.. "Power, Performance, and Cost Comparisons of Monolithic 3D ICs and TSV-based 3D ICs", IEEE S3S, 2015.

[2] S. Panth et al., "Design and CAD Methodologies for Low Power Gate-Level Monolithic 3D ICs", IEEE ISLPED 2014.




A B C

FIGURE 2: TECHNOLOGY COMPARISON (A) POWER OF INVERTER CHAIN
(B) STAGE DELAY IN INVERTER CHAIN (C) PIN CAPACITANCE FOR DIFFERENT CELLS AND DRIVABILITY




A B C

FIGURE 3: LDPC DESIGN RESULTS (A) CONTRIBUTION OF POWER COMPONENTS IN 2D IC
(B) RELATIVE 3D IC SAVINGS IN CAPACITANCE AND CELLS (C) RELATIVE 3D IC POWER SAVINGS