# Probe-Pad Placement for Prebond Test of 3-D ICs

Shreepad Panth, *Member, IEEE*, and Sung Kyu Lim, *Senior Member, IEEE*

***Abstract*— 3-D integrated circuits (3-D ICs) are emerging as a promising alternative to continue the scaling trajectory. They need to be tested before bonding (prebond) to ensure high stack yields. Several techniques exist for prebond test of 3-D ICs, and all of them require large probe pads for power delivery. We present the first probe-pad-aware 3-D IC placement framework, and this provides up to a 2% reduction in the wirelength and significant improvement with regard to testability metrics. In addition, we study several probe-pad configurations, and present a configuration that reduces the probe-pad count by 50% compared with adding a probe pad at every power/ground through-silicon-via location, while still being well within IR-drop constraints.**

***Index Terms*— 3-D ICs, Placement, Prebond Test, Probe Pads.**

## I. Introduction

3-D integrated circuits (3-D ICs) have emerged as a promising solution to the interconnect scaling problem. Although there are several categories of 3-D ICs, the most common type is through-silicon-via (TSV) based. In this category, two or more dies are first fabricated separately. They are then thinned and bonded together, and electrical connection between the dies is provided through TSVs. A typical structure of a TSV-based 3-D IC is shown in Fig. 1.

Although 3-D ICs shorten interconnects, the additional process steps introduced complicate design-for-test. The dies can be tested either before bonding them together (prebond) or after bonding is complete (postbond) [1]. While postbond test is necessary to guarantee a working chip, performing prebond test is a question of economics. Yields of the 3-D stack will be higher if only known-good-die is stacked, but this increases the cost of testing this IC. However, since yields increase exponentially if prebond test is performed, this paper assumes that it is a necessary step.

As discussed in Section II, prebond test can be carried out using a variety of methods, and each method has several test architectures available. These include noncontact testing, built-in-self-test (BIST), direct probing of the TSV microbumps, or adding oversized probe pads for probe needle touchdown. A probe pad is a large metal pad on the top metal layer that is large enough to support good contact between the probe needle and the die. A given test methodology may or may not require probe pads for test signaling, but probe pads are always required for prebond power delivery.

Manuscript received August 26, 2015; revised November 17, 2015; accepted December 1, 2015. Date of publication January 26, 2016; date of current version April 1, 2016. Recommended for publication by Associate Editor B. Dang upon evaluation of reviewers' comments.

S. Panth is with Altera Corporation, San Jose, CA 95134 USA (e-mail: shreepad.panth@gmail.com).

S. K. Lim is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: limsk@ece.gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCPMT.2015.2513756

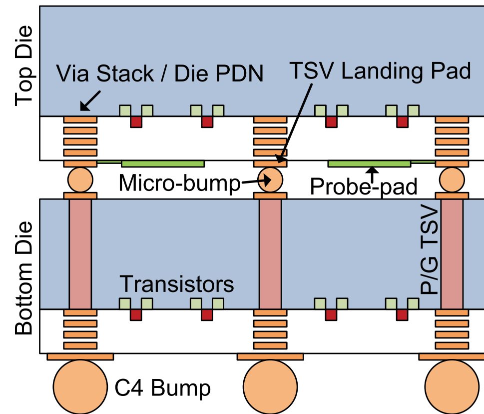


Fig. 1. PDN structure of a TSV-based 3-D IC.

Although power probe pads are always necessary for prebond test, there has been very little work in studying the best configuration to add them or their impact on the layout [2], [3]. As shown in Fig. 1, if probe pads are added into the layout, no TSV can be placed at that location. This is because TSV landing pads and probe pads compete for the same space, and overlaps would cause shorts between signals and power/ground. Any 3-D IC placement tool needs to account for probe-pad locations during TSV placement, and no previous work has provided such a tool. Panth and Lim [2], [3] simply manually pushed TSVs away from probe-pad locations as a postprocess to an existing 3-D IC placement.

This paper identifies suitable probe-pad placement schemes, and determines an appropriate probe-pad pitch, such that the number of probe pads is minimized while still meeting IR-drop constraints during prebond test. It also studies the overhead of adding probe pads into the layout in terms of both layout and test metrics. In addition, it provides a 3-D IC placement framework that builds probe-pad awareness into the global placement stage to obtain better quality of results.

## II. Literature Survey

Several challenges facing the test of 3-D ICs were enumerated in [4]. Early work focused mainly on postbond test, aiming to reduce the test time under certain constraints. 3-D scan chain construction based on genetic algorithm and integer linear programming approaches was presented in [5]. However, recent efforts have focused on prebond test as it can significantly increase stack yields. Providing test access to each prebond die is a challenge, as the dies are quite thin,

2156-3950 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

and some sort of carrier die is usually required. In addition, test access requires some point of contact between the tester and the die, and these potential points (the microbumps or TSVs) are quite small, and their pitch is rapidly decreasing [6].

Two techniques exist to avoid probing the TSVs directly—BIST and noncontact testing. BIST techniques for prebond TSV test are presented in [7]. However, these methods tend to use large on-die components, such as voltage dividers per TSV and tuned sense amplifiers. These, along with wiring complexity, require significant die area. This problem is exacerbated by the fact that a chip can have thousands of TSVs with densities approaching 10 000/mm$^2$. In addition, these BIST architectures do not support prebond logic testing. Noncontact testing has also been proposed, and it connects the tester to the die through inductive or capacitive coupling [8]. However, these techniques also require large area overhead for components, such as antennae or transceivers. Furthermore, both BIST and noncontact testing require some sort of test probe access for power delivery, which no existing work has addressed.

An alternate to the above techniques is to probe the prebond die, but this faces its own sets of challenges. Modern cantilever probes can reach a pitch of 35 $\mu$m, but TSVs have a much finer pitch [9]. A solution to this problem is to add large probe pads for needle touchdown, and a scan-island-based architecture for prebond test that relied on probe pads was presented in [10]. This was quite similar to the IEEE 1500 standard, and a test architecture based on the IEEE 1500 was formalized in [11], and several later works have assumed this architecture. Sharing test access mechanism wires between prebond and postbond tests under a prebond test pin count (and hence probe pad) constraint was discussed in [12].

There has also been recent efforts in using low contact-force spring-loaded probe cards to probe the microbumps directly [13]. Damage was shown to be nearly nonexistent for forces sufficient to ensure good contact. However, this paper limited the TSV pitch to 40 $\mu$m, and requires that the TSVs be placed, such that they align with the probe card. Although recent probe cards reduce the constraint on the TSV pitch [14], probe cards are expected to scale much slower than TSVs [6].

There has been recent work that bridges the gap between microbump and probe card scaling. Noia *et al.* [15] provide an architecture that supports multiple microbumps being shorted by a single probe needle, removing the need for probe card and TSV pitch matching. This architecture supports the testing of on-die logic as well as TSV testing, and it relies on changing the boundary scan registers of [11] to gated-scan registers. However, this architecture still does not remove the need for large probe pads for critical signals, such as clock and power. While prebond testable clock trees have been discussed in [16], very limited work has been done on power delivery during prebond test.

As discussed in this section, there has been extensive work on prebond testing, with the emphasis being on test architectures and technology (probe card) scaling. However, all the architectures discussed here require power delivery during prebond test. There has been very limited effort in this field, with only Panth and Lim [2], [3] discussing it. However, these existing works did not perform a comprehensive study on different configurations to add probe pads. In addition, they did not perform a detailed analysis about the impact of these probe pads on both layout and test metrics. Furthermore, as shown in Fig. 1, probe pads block TSVs from being placed over them. Both [2] and [3] simply took an existing 3-D IC placement, and moved TSVs away from probe pads as a postprocess. This paper provides a probe-pad aware placement framework that makes TSVs avoid probe-pad regions during global placement, which significantly improves the quality of results.

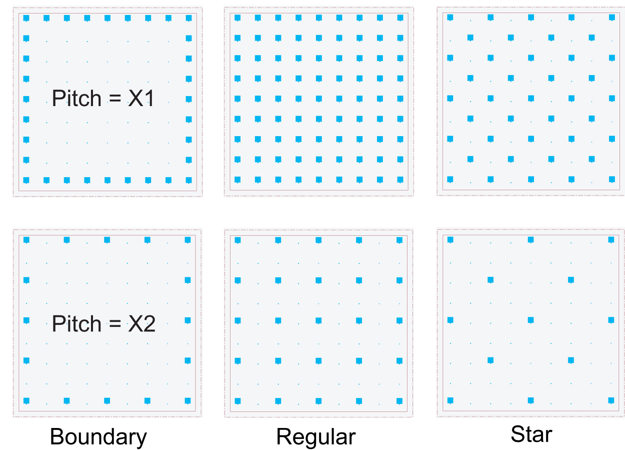


Fig. 2. Layout shots of the different probe-pad configurations with different pad pitches.

## III. Adding Probe Pads Into the 3-D IC Layout

This section first discusses several possible power/ground probe-pad configurations, each with its own pros and cons. Next, it discusses how the 3-D IC placer can be modified to account for the fact that TSVs cannot overlap with these probe pads. Finally, it discusses methods to quantify the impact of adding these probe pads on both layout and test metrics.

### *A. Probe-Pad Configurations*

As discussed in Section II, probe pads need to be added into the layout to provide power and ground connections during prebond test of the top die, irrespective of the test architecture. However, there has been no comprehensive study on the optimal probe-pad configurations to minimize the number of probe pads, while ensuring that the IR-drop constraint is met during prebond test. This paper studies three configurations of probe pads, and three different ways to connect the added probe pads to power/ground TSVs.

This paper assumes that the power TSVs are added in a regular fashion throughout the layout. The local power delivery network (PDN) on the top die is fed directly from these locations, so they are the primary tap points. We consider three different configurations of probe pads, as shown in Fig. 2. The first is a boundary configuration, where the probe pads are placed along the periphery of the chip. The next style is a regular configuration, where the probe pads are distributed with a constant pitch throughout the layout. The third technique is termed star configuration, which doubles the pitch of the regular placement, but also places an inner interleaved

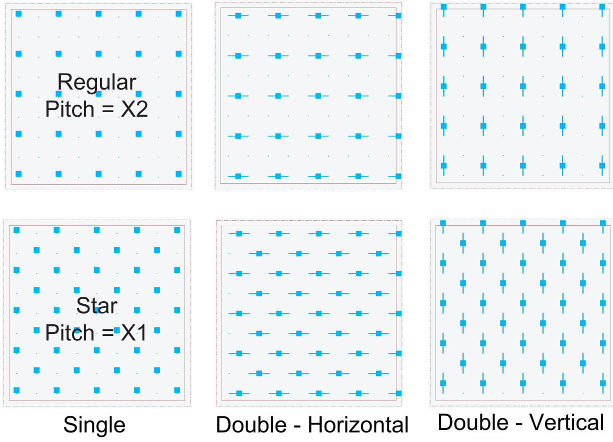


Fig. 3. Layout shots showing that a probe pad can connect to a single TSV or two TSVs in two different configurations.

pad array with the same doubled pitch. Clearly, among all the configurations, the boundary configuration will have the fewest number of pads, but the die may suffer from high IR-drop in the center. The regular placement has the best IR-drop at the cost of a lot of probe pads. The star configuration offers a good compromise of number of pads and IR-drop.

To standardize the pitch naming conventions across different configurations, we label the pitch in terms of the minimum possible pitch for that configuration. For example, an $X1$ pitch regular configuration implies that each and every power TSV is connected to a probe pad. In contrast, an $X1$ pitch star configuration is the minimum possible pitch for the star configuration, but it will not connect all TSVs. An $X2$ pitch implies double the $X1$ pitch, and so on.

So far, it has been assumed that each probe pad connects to a single TSV only. However, it is possible to connect each probe pad to multiple TSVs using the same metal layer as the probe pad (and TSV landing pads). This provides a low resistance tap point to multiple TSVs from the same probe pad, increasing the robustness of the PDN. However, this connection will block the placement of TSVs over it, so the amount of metal used has to be minimized. In addition, we should be careful not to short power and ground TSVs, as they will both use this same top metal for probe pad to TSV connections. The simplest method to do this is to connect each probe pad to two neighboring TSVs only. A probe pad can be placed at the midpoint of two TSVs, and connected to either the left and right TSVs (double horizontal connection), or to the top and bottom TSVs (double vertical connection). Layout shots of these configurations are shown in Fig. 3.

### *B. Probe-Pad-Aware 3-D IC Placement*

As discussed in Section I, signal TSVs cannot overlap with probe pads; otherwise, they will be shorted to the power supply. This section discusses how the global placement framework can be modified to support probe pads. Our placer is based on a force-directed placer that was extended to support 3-D IC design [17]. In addition, it assumes that all power and ground TSVs are preplaced before starting placement, and the location of all probe pads is known beforehand.

This analytic placer tries to minimize the wirelength in both the $x$- and $y$-dimensions $\Gamma = \Gamma_x + \Gamma_y$. Since the $x$- and $y$-dimensions are independent, only the $x$-dimension is described here, and a similar approach is applicable to the $y$-dimension as well. If $\mathbf{x} = [x_1, x_2, \ldots, x_N]^T$ is the vector of the $x$ locations of all the cells, then $\Gamma_x = 0.5\mathbf{x}^T C_x \mathbf{x} + \mathbf{x}^T d_x +$ constant, where $C_x$ defines the connections between movable cells and $d_x$ defines the connections between fixed and movable cells. A net force that pulls the modules together is defined as the gradient of the above equation, $F_x^{\text{net}} = \nabla_x \Gamma_x = C_x \mathbf{x} + d_x$.

Another force-the move force is added to help remove overlap caused by the net force. Let $D(x, y)$ be the density function of the chip. This is computed by simply summing the number of cells at each point $(x, y)$ within the chip, and subtracting a constant value $t_d$ at each point. $t_d$ is computed, such that the sum of $D$ over all $(x, y)$ equals zero. Therefore, if a point has a negative value, it can hold a cell, and if it has a positive value, it has too many cells in it. The density becomes balanced (or there is no cell overlap) if it becomes zero at every $(x, y)$ location in the chip. The function $D$ can be interpreted as a charge distribution and creates a charge distribution given by Poisson's equation $\nabla^2 \Phi(x, y) = -D(x, y)$. After solving this differential equation, we get target $(\mathring{x}_i, \mathring{y}_i)$ points for each cell, such that all overlaps are removed if cells are moved to these points. The move force in the $x$-direction for this cell is then given by $F_{x,i}^{\text{move}} = \mathring{w}_i(x_i - \mathring{x}_i)$. Here, $\mathring{w}_i$ is a weight for the move force, and is adjusted, such that it balances with the net force. There is an additional force not discussed here—the hold force, which is used to decouple placement iterations.

In summary, the move force tries to remove cell overlap, and the net force moves connected cells together. For 3-D IC placement, the cells are prepartitioned to obtain their $z$ location, and TSVs are inserted into the netlist as large cells. The net force is then applied across all dies, and the move force is applied on a per-die basis to only remove $(x, y)$ overlaps between cells and TSVs in that particular die.

Now, if a power TSV is preplaced, it serves as a blockage for both cells and TSVs, and $D$ can simply be modified to accommodate them. However, if probe pads are added, they act as TSV-only blockages, and act across different dies. For example, if a probe pad is added in the top die (Fig. 1) at a given $(x, y)$ location, cells can be placed at that location in the bottom die, but the TSVs in the bottom die need to avoid those locations. Therefore, the move force cannot readily be modified. To solve this issue, we introduce another TSV-only density function per die $D_{\text{TSV}}(x, y)$. It is constructed quite similar to $D(x, y)$, except that this function has only TSVs and probe pads of the adjacent die within it, and no cells. Therefore, it can be used to obtain a TSV-only move force $F^{\text{move,TSV}}$. Now, each TSV is part of two force systems—one where overlap between all cells and TSVs is removed and one where overlaps between TSVs and probe pads of the adjacent die is removed. The effective move force for each TSV $t$ can be written as

$$F_{x,t}^{\text{move,eff}} = \alpha F_{x,t}^{\text{move,TSV}} + (1 - \alpha) F_{x,t}^{\text{move}} \tag{1}$$

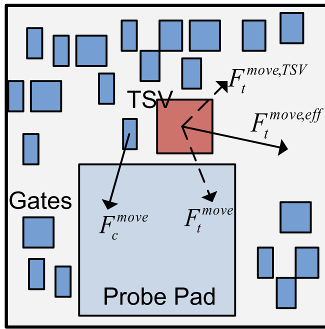


Fig. 4. Cells have only one move force. In addition to this, TSVs have a TSV-only move force that moves them away from the probe pads placed in the adjacent die.

where $\alpha$ is termed the pad-TSV move effort. The higher the value of $\alpha$, the more effort is spent removing probe pad rather than a cell overlap. This may or may not be desirable, as probe pads are quite large compared with cells. Once global placement iterations terminate, any remaining pad-TSV overlap is handled during detailed placement. An illustration of the move force acting on cells and TSVs is shown in Fig. 4.

### C. Quantifying the Overhead of Adding Probe Pads

The impact of adding probe pads on the regular functional mode is quite straightforward to determine. We can measure the impact that pads have on various layout metrics, such as wirelength, timing, and power. However, quantifying the impact on test is not as straightforward. Conventional metrics, such as fault coverage for stuck-at or transition tests, are affected only by the logical functionality of the design. Since adding probe pads have no impact on the logic of the design, these metrics do not change. However, these fault models only check for large catastrophic defects on the chip. Today's circuits are also prone to small-delay defects (SDDs), which may cause the parametric failure of the chip. A metric that captures the effectiveness of test patterns is the statistical delay quality level (SDQL), and it has been demonstrated that TSV-induced stress can change the SDQL of a 3-D IC [18].

The SDQL depends on the timing slack through every net in the design and the probability of timing degradation (fault) on that net. We use the same fault distribution as [18], which is given as

$$F(s) = \begin{cases} 1.97e^{-2.1s} + 0.005, & 0 \leq s \leq 10 \\ 0, & \text{otherwise.} \end{cases} \quad (2)$$

A more intuitive metric is the defective parts per million (DPPM), which is obtained by dividing the SDQL by $N$, the total number of potential SDD faults as reported by Automatic Test Patten Generation (ATPG).

Clearly, adding probe pads into the layout shifts the timing slacks of the paths through affected TSVs and, hence, the DPPM. Therefore, it quantifies the impact of probe pads on test-related metrics. It should also be noted that we only perform SDD testing during postbond test. It is unlikely that parametric delay testing will be performed prebond, as all the 3-D timing paths are incomplete. In addition, this increases the cost of testing the 3-D chip, and stuck-at and transition tests during prebond are likely to be sufficient.

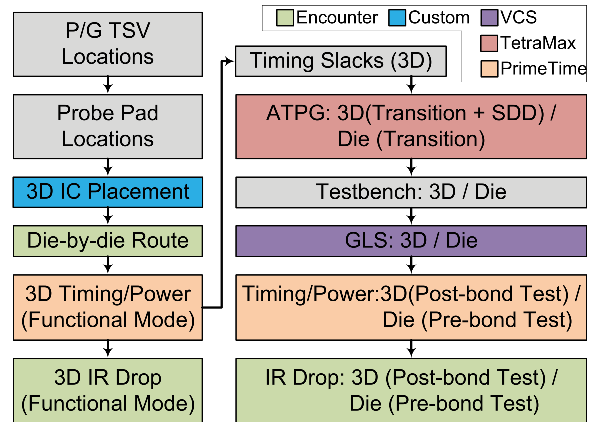


Fig. 5. Design and analysis methodology used in this paper. Each step in the right column is performed for both postbond test and prebond test.

## IV. Design and Analysis Flow

An overview of the design flow used in this paper is shown in Fig. 5. Given the 3-D partition of all the gates and power/ground TSV locations, we choose a given configuration of probe pads. This is run through the 3-D IC placer to get the $x$, $y$, and $z$ locations for every cell and TSV in the design. Separate Verilog and design exchange format (DEF) files are then created for each die, so that they can be opened in separate windows of commercial 2-D IC tools. Each die is routed separately using a commercial router to obtain a 3-D routed design. 3-D timing and power analysis is performed in Synopsys PrimeTime, and 3-D IR-drop analysis is performed using Cadence Encounter, as described next.

To perform 3-D timing and power analysis, we first extract the parasitics of each die separately, and also create a 3-D parasitics file that contains only the parasitics of the TSVs themselves. We also create a 3-D netlist that contains only the interdie connections. We import all the netlists and parasitics into Synopsys PrimeTime, and use tcl scripts to stitch them together. Since this is a timing tool, it requires no physical $(x, y, z)$ information, and we can obtain 3-D timing numbers. In addition, we perform statistical power simulation for the functional mode, to obtain power numbers for every gate in the design.

Now that the power numbers are obtained, we need to perform 3-D IR-drop analysis. We duplicate the metal layers in the interconnect technology (ICT) file to obtain a 3-D ICT. The TSV is treated as a large via in this stackup. This stackup is then fed through Cadence Techgen to generate a technology (tch) file that can be used for 3-D IR-drop analysis. To obtain a 3-D layout, we dump the layout for each die in the DEF format. Suffixes are then added to the metal layers in each DEF file. For example, metal1 on the bottom die is labeled metal1_0, and metal1 on the top die is labeled metal1_1. This is then loaded into Cadence Encounter along with the already created 3-D netlists and modified tch file. The location of the power TSVs (or C4 bumps) along with the power

TABLE I
BENCHMARK STATISTICS. $W/H$ STAND FOR WIDTH/HEIGHT

| Ckt | # Cells ($\times 10^3$) | # Flops ($\times 10^3$) | Cell Area ($mm^2$) | Clk. P. ($ns$) | 3D W/H ($\mu m$) | # TSV | |
|---|---|---|---|---|---|---|---|
| | | | | | | Signal | P/G |
| fft | 253.1 | 75.6 | 0.725 | 3 | 800 | 1591 | 25/16 |
| jpeg | 580.1 | 37.0 | 0.892 | 4 | 950 | 3063 | 36/25 |
| mult | 1177.7 | 68.8 | 1.636 | 6 | 1300 | 7803 | 81/64 |

numbers obtained from PrimeTime is then used to perform 3-D IR-drop analysis on this design.

In addition to the functional mode, we also need to perform these analyses for prebond test and postbond test. Since we perform SDD testing in addition to transition fault testing for postbond test, information about the timing slack through each path is required. This information is obtained from Synopsys PrimeTime, and fed to Synopsys TetraMax for joint SDD and transition fault test pattern generation. The output is a testbench for the design, which simulates the design for each test pattern. Gate-level simulation (GLS) is then performed using Synopsys VCS for only the capture cycle to obtain the switching activity for each gate on a per-pattern basis. This can then be used to compute the 3-D power and IR-drop similar to the functional mode. Since it is infeasible to compute the power and IR-drop for every pattern, we perform two simulations only—the first one computes the power and IR-drop for the pattern with the maximum switching activity as reported by Synopsys TetraMax and the second computes the power and IR-drop where the activity of each gate is averaged across all patterns. In this fashion, we can obtain both worst case and average behavior.

Now, for prebond test, the bottom die has the C4 bumps to provide power, so it is not expected to have any IR-drop problems. Therefore, we only consider the top die, as it is the only die that needs to be fed power through probe pads. This die in isolation follows the existing 2-D IC methodologies. We perform transition fault ATPG and GLS as before, and compute the maximum and average IR-drop behavior across all test patterns. In addition, the power sources are now the probe pads, not the TSV/C4 bump locations.

It should be noted that in all the above test steps, no particular test architecture is assumed. This is to keep the analysis in this paper as general as possible and applicable across different test architectures, such as BIST or direct microbump probing.

## V. EXPERIMENTAL RESULTS

The placement framework is written in C++ and all other scripts and utilities are written in python/tcl. We use the Nangate 45-nm library to implement three benchmarks, the statistics of which are shown in Table I. The first two are taken from the OpenCores benchmark suite, and the third is a custom pipelined multiplier. The fast Fourier transform (FFT) benchmark performs a 256 point FFT, with a precision of 8 b on both the real and imaginary components of a floating point number. The JPEG benchmark takes in the raw red, blue, and green pixel values, and creates a bitstream necessary to build a JPEG image. Finally, the multiplier first takes two 256-b integers, and performs a 256 $\times$ 4 multiplication as its first stage. The partial products are then added together in a binary tree.

TABLE II
IMPACT OF PAD-TSV MOVE EFFORT ($\alpha$)

| $\alpha$ | 3D Routed WL ($m$) | Functional Power ($mW$) | DPPM | Max. Post-bond Test Pow. ($mW$) |
|---|---|---|---|---|
| **fft** | | | | |
| 0 | 10.64 (1.00) | 203.8 (1.00) | 25.3 (1.00) | 401.1 (1.00) |
| 0.25 | 10.42 (0.98) | 204.3 (1.00) | 23.9 (0.95) | 409.8 (1.02) |
| 0.5 | 10.91 (1.03) | 206.8 (1.01) | 24.6 (0.97) | 404.2 (1.01) |
| 0.75 | 10.62 (1.00) | 204.8 (1.00) | 24.8 (0.98) | 404.8 (1.01) |
| 1 | 10.66 (1.00) | 204.0 (1.00) | 24.3 (0.96) | 399.5 (1.00) |
| **jpeg** | | | | |
| 0 | 10.25 (1.00) | 457.5 (1.00) | 77.4 (1.00) | 578.5 (1.00) |
| 0.25 | 10.29 (1.00) | 457.1 (1.00) | 76.0 (0.98) | 548.5 (0.95) |
| 0.5 | 10.20 (1.00) | 455.7 (1.00) | 77.8 (1.01) | 552.4 (0.95) |
| 0.75 | 10.20 (1.00) | 450.7 (0.99) | 82.2 (1.06) | 562.6 (0.97) |
| 1 | 10.35 (1.01) | 452.0 (0.99) | 82.6 (1.07) | 566.1 (0.98) |
| **mult** | | | | |
| 0 | 24.36 (1.00) | 409.7 (1.00) | 3468.4 (1.00) | 792.5 (1.00) |
| 0.25 | 25.00 (1.03) | 412.9 (1.01) | 3460.7 (1.00) | 804.8 (1.02) |
| 0.5 | 23.97 (0.98) | 408.1 (1.00) | 3873.6 (1.12) | 790.9 (1.00) |
| 0.75 | 24.69 (1.01) | 408.8 (1.00) | 3478.7 (1.00) | 793.5 (1.00) |
| 1 | 24.26 (1.00) | 407.1 (0.99) | 3552.1 (1.02) | 789.6 (1.00) |

TABLE III
IMPACT OF PROBE-PAD COUNT

| Pitch | # Pads (P+G) | 3D Routed WL ($m$) | Functional Power ($mW$) | DPPM | Max. Post-B. Test P. ($mW$) |
|---|---|---|---|---|---|
| **fft** | | | | | |
| $\infty$ | 0 | 10.38 (1.00) | 200.8 (1.00) | 23.4 (1.00) | 197.5 (1.00) |
| X2 | 13 | 10.55 (1.02) | 202.2 (1.01) | 23.4 (1.00) | 198.4 (1.00) |
| X1 | 41 | 10.64 (1.03) | 203.0 (1.01) | 24.1 (1.03) | 201.0 (1.02) |
| **jpeg** | | | | | |
| $\infty$ | 0 | 10.13 (1.00) | 451.9 (1.00) | 84.0 (1.00) | 498.5 (1.00) |
| X2 | 18 | 10.27 (1.01) | 451.6 (1.00) | 79.3 (0.94) | 498.5 (1.00) |
| X1 | 61 | 10.24 (1.01) | 453.8 (1.00) | 83.4 (0.99) | 499.6 (1.00) |
| **mult** | | | | | |
| $\infty$ | 0 | 24.99 (1.00) | 410.0 (1.00) | 4097.1 (1.00) | 737.9 (1.00) |
| X2 | 41 | 25.74 (1.03) | 410.1 (1.00) | 3474.0 (0.85) | 741.0 (1.00) |
| X1 | 145 | 25.80 (1.03) | 410.3 (1.00) | 4209.6 (1.03) | 737.4 (1.00) |

Each design is prepartitioned into two dies, and the number of signal TSVs is chosen, such that they occupy roughly 20% of the area in the bottom die. This number of TSVs comes from the fact that Pathak *et al.* [19] have demonstrated a sweet spot in terms of design quality versus TSV count. Adding too few TSVs does not fully utilize the benefit that 3-D ICs offer, and adding too many TSVs increases die area, thereby increasing wirelength. To achieve this target TSV count, we use a modified min-cut partitioner as in [17]. This starts with a random partition, and begins iteratively minimizing the cut-size (and hence TSV count). However, unlike the traditional min-cut partitioners, we terminate iterations when the target cut-size is reached, instead of proceeding all the way to min-cut.

The TSV (including landing pad) is assumed to have a width of 5 $\mu$m. It is assumed to have a resistance of 50 m$\Omega$ and a capacitance of 30 fF. The power and ground TSVs are placed with a pitch of 150 $\mu$m each, which is large enough that they can directly align with C4 bumps, as shown in Fig. 1. The number of ground TSVs is fewer as they are interleaved in-between the power TSV array.

TABLE IV
IMPACT OF DIFFERENT PROBE-PAD CONFIGURATIONS

| Config | # Pads (P+G) | 3D Routed WL ($m$) | Functional Mode (3D) | | Pre-bond Test (Top Die) | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Power ($mW$) | IR Drop ($mV$) | Max. Pow Pattern | | Avg. Pow Pattern | |
| | | | | | Power ($mW$) | IR Drop ($mV$) | Power ($mW$) | IR Drop ($mV$) |
| **fft** | | | | | | | | |
| Regular - X1 | 41 (1.00) | 10.54 (1.00) | 201.5 (1.00) | 43 (1.00) | 239.6 (1.00) | 95 (1.00) | 232.6 (1.00) | 98 (1.00) |
| Regular - X2 | 13 (0.32) | 10.69 (1.01) | 203.5 (1.01) | 44 (1.02) | 273.1 (1.14) | 291 (3.06) | 234.3 (1.01) | 252 (2.57) |
| Boundary - X1 | 28 (0.68) | 10.23 (0.97) | 198.9 (0.99) | 50 (1.16) | 447.7 (1.87) | 308 (3.24) | 226.4 (0.97) | 156 (1.59) |
| Boundary - X2 | 12 (0.29) | 10.42 (0.99) | 201.0 (1.00) | 44 (1.02) | 401.9 (1.68) | 483 (5.08) | 230.1 (0.99) | 277 (2.83) |
| Star - X1 | 21 (0.51) | 10.56 (1.00) | 201.5 (1.00) | 45 (1.05) | 234.7 (0.98) | 120 (1.26) | 229.9 (0.99) | 121 (1.23) |
| Star - X2 | 7 (0.17) | 10.42 (0.99) | 200.2 (0.99) | 23 (0.53) | 378.6 (1.58) | 399 (4.20) | 231.9 (1.00) | 247 (2.52) |
| **jpeg** | | | | | | | | |
| Regular - X1 | 61 (1.00) | 10.20 (1.00) | 454.0 (1.00) | 48 (1.00) | 331.2 (1.00) | 56 (1.00) | 295.5 (1.00) | 55 (1.00) |
| Regular - X2 | 18 (0.30) | 10.21 (1.00) | 452.5 (1.00) | 48 (1.00) | 346.8 (1.05) | 259 (4.63) | 296.4 (1.00) | 208 (3.78) |
| Boundary - X1 | 36 (0.59) | 10.23 (1.00) | 454.2 (1.00) | 49 (1.02) | 351.5 (1.06) | 213 (3.80) | 296.6 (1.00) | 185 (3.36) |
| Boundary - X2 | 16 (0.26) | 10.16 (1.00) | 450.2 (0.99) | 46 (0.96) | 317.3 (0.96) | 281 (5.02) | 296.4 (1.00) | 238 (4.33) |
| Star - X1 | 31 (0.51) | 10.19 (1.00) | 453.1 (1.00) | 49 (1.02) | 327.6 (0.99) | 87 (1.55) | 297.9 (1.01) | 85 (1.55) |
| Star - X2 | 10 (0.16) | 10.18 (1.00) | 449.2 (0.99) | 47 (0.98) | 341.0 (1.03) | 395 (7.05) | 295.0 (1.00) | 320 (5.82) |
| **mult** | | | | | | | | |
| Regular - X1 | 145 (1.00) | 25.76 (1.00) | 410.2 (1.00) | 44 (1.00) | 504.7 (1.00) | 97 (1.00) | 448.2 (1.00) | 54 (1.00) |
| Regular - X2 | 41 (0.28) | 25.74 (1.00) | 410.0 (1.00) | 44 (1.00) | 455.9 (0.90) | 297 (3.06) | 449.3 (1.00) | 293 (5.43) |
| Boundary - X1 | 60 (0.41) | 25.74 (1.00) | 410.1 (1.00) | 44 (1.00) | 465.3 (0.92) | 412 (4.25) | 448.5 (1.00) | 396 (7.33) |
| Boundary - X2 | 28 (0.19) | 25.74 (1.00) | 410.0 (1.00) | 44 (1.00) | 513.3 (1.02) | 608 (6.27) | 446.8 (1.00) | 533 (9.87) |
| Star - X1 | 73 (0.50) | 25.75 (1.00) | 410.2 (1.00) | 44 (1.00) | 465.2 (0.92) | 116 (1.20) | 448.6 (1.00) | 115 (2.13) |
| Star - X2 | 21 (0.14) | 25.73 (1.00) | 410.0 (1.00) | 44 (1.00) | 500.9 (0.99) | 453 (4.67) | 446.5 (1.00) | 414 (7.67) |

In the remainder of this section, we first discuss selecting an appropriate value of the pad-TSV move effort $\alpha$. We then quantify the impact of increasing the number of probe pads, and demonstrate that fewer pads are desirable. Next, we compare and contrast different probe-pad configurations and pad to TSV connection options.

### *A. Choosing the Pad-TSV Move Effort*

For this experiment, we assume a regular probe-pad configuration, with an X1 pitch. We vary the value of $\alpha$ from 0 to 1 in increments of 0.25, run through the entire design flow, and tabulate the statistics in Table II. Only the postbond test-related metrics are tabulated, since SDD testing is performed only during the postbond test, as discussed in Section III-C. An $\alpha$ of 0 implies regular placement without any pad-TSV move effort, and overlaps are removed only during the detailed placement stage. This mimics the approach in [2] and [3]. Similarly, an $\alpha$ of 1 implies that any TSV-cell overlap is not considered during global placement, and overlap is removed during detailed placement.

From Table II, we observe that $\alpha = 0$ never gives the best results in terms of wirelength or DPPM. Therefore, probe-pad-aware global placement is necessary. We also observe up to a 2% reduction in the routed wirelength, and a 5% reduction in the DPPM of the design depending on the choice of $\alpha$. To get best results, $\alpha$ would need to be tuned on a per-benchmark basis, but this is impractical. From Table II, we observe that $\alpha = 0.25$ gives the best average behavior across all benchmarks. We observe almost no change in the average wirelength or functional mode power, with a 2.4% improvement in the DPPM.

### *B. Impact of Probe-Pad Count*

Section V-A determined an appropriate value of $\alpha$ that can be used for global placement. Using this value, we now quantify the impact of the number of probe pads, assuming a regular configuration and a single pad-TSV connection. We run the placer without pads (pitch $= \infty$), and also for the X1 pitch and the X2 pitch, and tabulate the results in Table III.

From this table, we observe that increasing the number of probe pads leads to up to a 3% increase in the wirelength and 1% increase in the functional power, and a 2% increase in the postbond test power for the pattern with maximum switching activity. The DPPM is not monotonic, and this is because it is a complex quantity that depends on the slack distribution through every TSV. Simply displacing a TSV does not imply that DPPM will increase. We also observe that the X2 pitch always has lower DPPM than the X1 pitch, and is desirable. This is also true from the perspective of the tester, as fewer needles required for test to reduce the cost of the probe card.

### *C. Impact of Probe-Pad Configuration*

We now study the impact of different probe-pad configurations on the IR-drop during prebond test. We consider only the top die, assume in this section that each probe pad connects only to a single TSV, and assume that the IR-drop target is 10% of $V_{DD}$ or 110 mV. The baseline configuration is Regular-X1, which connects a pad for every power and ground TSV. The results are shown in Table IV.

As shown in Table IV, doubling the pitch of the regular configuration reduces the probe-pad count by up to 72%. However, this leads to up to a 5.43× worse average pattern IR-drop, which is far beyond the tolerable margin. Note that the IR-drop of the worst pattern is not entirely predictable as it depends on which gates ATPG chooses to switch during that particular test. Reducing the worst pattern IR-drop, if far worse than the average pattern IR-drop, can be achieved through power-aware ATPG, and is beyond the scope of this paper.

Next, we observe that the Boundary-X1 configuration can reduce the pad count by up to 60%, which is actually

TABLE V
IMPACT OF CONNECTING A SINGLE PROBE PAD TO MULTIPLE TSVs. NUMBERS IN BRACKETS ARE NORMALIZED TO THE REGULAR-X1 CONFIGURATION IN TABLE IV

| Config | # Pads (P+G) | 3D Routed WL ($m$) | Functional Mode (3D) Power ($mW$) | Functional Mode (3D) IR Drop ($mV$) | Pre-bond Test (Top Die) Max. Pow Pattern Power ($mW$) | Max. Pow Pattern IR Drop ($mV$) | Avg. Pow Pattern Power ($mW$) | Avg. Pow Pattern IR Drop ($mV$) |
|---|---|---|---|---|---|---|---|---|
| **fft** | | | | | | | | |
| Regular - X2 - Double Hor. | 13 (0.32) | 10.68 (1.01) | 201.7 (1.00) | 41 (0.95) | 243.9 (1.02) | 244 (2.57) | 235.9 (1.01) | 233 (2.38) |
| Regular - X2 - Double Vert. | 13 (0.32) | 10.60 (1.01) | 201.3 (1.00) | 47 (1.09) | 241.4 (1.01) | 128 (1.35) | 228.3 (0.98) | 120 (1.22) |
| Star - X1 - Double Hor. | 19 (0.46) | 10.47 (0.99) | 202.7 (1.01) | 46 (1.07) | 395.6 (1.65) | 195 (2.05) | 232.1 (1.00) | 113 (1.15) |
| Star - X1 - Double Vert. | 19 (0.46) | 10.48 (0.99) | 202.3 (1.00) | 45 (1.05) | 247.5 (1.03) | 111 (1.17) | 232.4 (1.00) | 102 (1.04) |
| **jpeg** | | | | | | | | |
| Regular - X2 - Double Hor. | 18 (0.30) | 10.28 (1.01) | 454.3 (1.00) | 49 (1.02) | 319.2 (0.96) | 189 (3.38) | 295.4 (1.00) | 176 (3.20) |
| Regular - X2 - Double Vert. | 18 (0.30) | 10.15 (0.99) | 452.0 (1.00) | 47 (0.98) | 294.5 (0.89) | 108 (1.93) | 301.9 (1.02) | 101 (1.84) |
| Star - X1 - Double Hor. | 28 (0.46) | 10.24 (1.00) | 451.0 (0.99) | 47 (0.98) | 328.7 (0.99) | 88 (1.57) | 295.4 (1.00) | 79 (1.44) |
| Star - X1 - Double Vert. | 28 (0.46) | 10.21 (1.00) | 451.6 (0.99) | 47 (0.98) | 324.7 (0.98) | 78 (1.39) | 300.7 (1.02) | 63 (1.15) |
| **mult** | | | | | | | | |
| Regular - X2 - Double Hor. | 41 (0.28) | 25.74 (1.00) | 410.0 (1.00) | 44 (1.00) | 494.0 (0.98) | 292 (3.01) | 496.0 (1.11) | 263 (3.55) |
| Regular - X2 - Double Vert. | 41 (0.28) | 25.74 (1.00) | 410.1 (1.00) | 44 (1.00) | 568.0 (1.13) | 119 (1.23) | 451.0 (1.01) | 120 (1.62) |
| Star - X1 - Double Hor. | 69 (0.48) | 25.75 (1.00) | 410.2 (1.00) | 44 (1.00) | 536.0 (1.06) | 105 (1.08) | 507.5 (1.13) | 89 (1.20) |
| Star - X1 - Double Vert. | 69 (0.48) | 25.75 (1.00) | 410.1 (1.00) | 44 (1.00) | 551.0 (1.09) | 101 (1.04) | 503.6 (1.12) | 89 (1.20) |

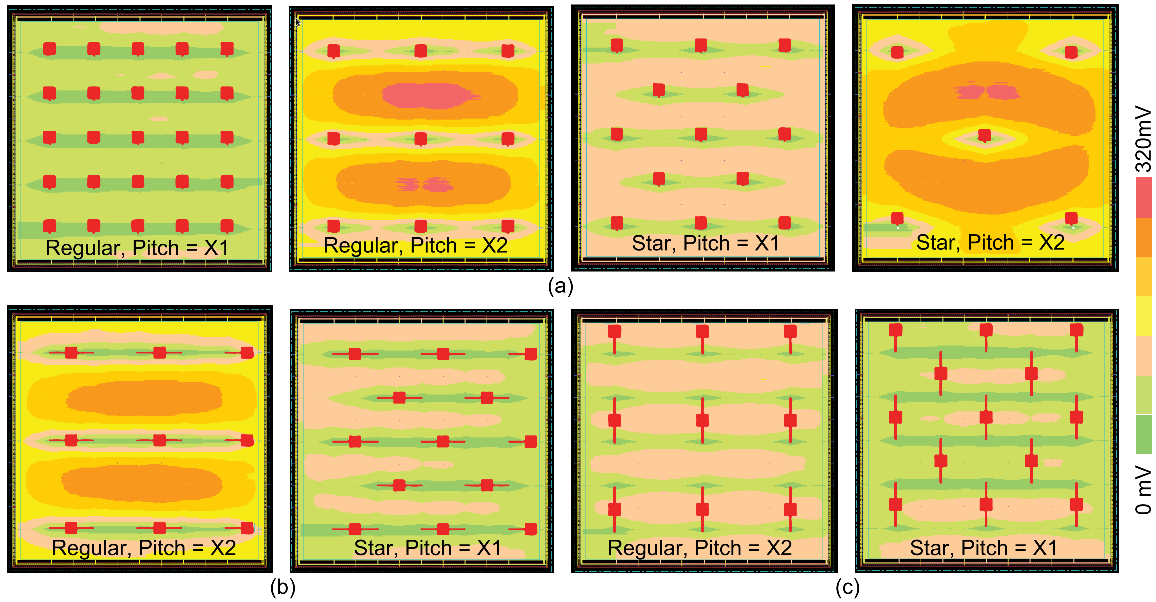


Fig. 6. IR-drop maps of various probe-pad configurations of the FFT benchmark. Red squares: probe-pad locations. (a) Single connection. (b) Double connection (horizontal). (c) Double connection (vertical).

less than that offered by the Regular-X2 configuration. However, in large circuits, the IR-drop is much (up to 7.3×) worse, and therefore, the boundary configuration is not tenable as far as IR-drop is concerned (except for very small circuits).

Finally, we explore the star configuration. As observed, the Star-X1 configuration offers up to a 50% reduction in the probe-pad count, and this reduction is consistent across all circuit sizes, unlike the boundary configuration. In fact, in smaller circuits, the Star-X1 configuration actually uses fewer pads than the Boundary-X1 configuration. In addition, the worst IR-drop of the Star-X1 configuration is only 2.13× worse than the Boundary-X1 and Regular-X2, so it is a suitable candidate. The IR-drops in the three circuits are 121, 85, and 115 mV, which are all fairly close to the 110-mV constraint. The Star-X2 configuration has much worse IR-drop, and is not considered further. We now discuss how to reduce the IR-drop of these configurations further.

### *D. Impact of Probe Pad to TSV Connection Style*

In terms of IR-drop, the best option is Regular-X1, but this uses a significant number of pads. The two next best options are Star-X1 and Regular-X2. Both use much fewer pads, but the IR-drop is over the design budget. We now explore how connecting a single pad to multiple TSVs can improve the IR-drop of these configurations.

We add pads in both the double-horizontal and double-vertical configurations, and tabulate the results in Table V. The numbers in brackets are normalized to the Regular-X1 configuration in Table IV. In addition, sample IR-drop maps for select configurations of the FFT benchmark are shown in Fig. 6.

The first thing we observe is that the double-vertical configuration always provides results far superior to the double-horizontal configuration. This effect is more pronounced with the Regular-X2 configuration, and sometimes produces results with IR-drop up to 49% better. This is due to the fact that the standard cells are usually connected with horizontal rails at the lowest metal level. The double horizontal configuration merely provides multiple connections along the same rail, leading to a high IR-drop on the unconnected rails. In contrast, the double-vertical configuration connects multiple standard cell rails, leading to a greater number of rails that have direct connection to probe pads. For example, in the Regular-X2 of Fig. 6, the double-horizontal configuration connects three rails, while the double-vertical configuration connects five rails.

Next, we observe that the Star-X1 double-vertical connection always produces results less than the IR-drop constraint and always uses less than 50% of the pads of the Regular-X1 configuration. The Regular-X2 double-vertical configuration uses even fewer probe pads, but the IR-drop is sometimes up to 18 mV over the budget. Since the Star-X1 always produces designs under the constraint, it is the preferred choice.

## VI. Conclusion

In this paper, we have first presented a probe-pad-aware placement framework for 3-D ICs. We have also presented a design and analysis methodology that can provide signoff timing, power, and testability results. We have demonstrated that our placement framework provides up to a 2% and 5% reduction in the 3-D routed wirelength and DPPM, respectively. Next, we demonstrated that fewer pads are desirable, and presented probe-pad configurations that can reduce the pad count. We have demonstrated that a star configuration with a single pad to TSV connection can reduce the pad count by up to 50%, while almost meeting the IR-drop constraint. We have also demonstrated that connecting a single probe pad to two TSVs in a vertical configuration can bring the IR-drop within the constraint, without any impact on the pad count.

## References

[1] E. J. Marinissen and Y. Zorian, "Testing 3D chips containing through-silicon vias," in *Proc. Int. Test Conf. (ITC)*, Nov. 2009, pp. 1–11.

[2] S. Panth and S. K. Lim, "Scan chain and power delivery network synthesis for pre-bond test of 3D ICs," in *Proc. IEEE VLSI Test Symp.*, May 2011, pp. 26–31.

[3] S. Panth and S. K. Lim, "Transition delay fault testing of 3D ICs with IR-drop study," in *Proc. IEEE VLSI Test Symp.*, Apr. 2012, pp. 270–275.

[4] H.-H. S. Lee and K. Chakrabarty, "Test challenges for 3D integrated circuits," *IEEE Des. Test*, vol. 26, no. 5, pp. 26–35, Sep./Oct. 2009.

[5] X. Wu, P. Falkenstern, K. Chakrabarty, and Y. Xie, "Scan-chain design and optimization for three-dimensional integrated circuits," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 5, no. 2, Jul. 2009, Art. ID 9.

[6] Y. Ohara *et al.*, "10 $\mu$m fine pitch Cu/Sn micro-bumps for 3-D super-chip stack," in *Proc. IEEE Int. Conf. 3D Syst. Integr.*, Sep. 2009, pp. 1–6.

[7] C. Wang *et al.*, "BIST methodology, architecture and circuits for pre-bond TSV testing in 3D stacking IC systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 139–148, Jan. 2015.

[8] J. J. Kim *et al.*, "Non-contact wafer-level TSV connectivity test methodology using magnetic coupling," in *Proc. IEEE Int. 3D Syst. Integr. Conf.*, Oct. 2013, pp. 1–4.

[9] K. Lee, "Trends in test," in *Proc. IEEE Asian Test Symp.*, Dec. 2010.

[10] D. L. Lewis and H. S. Lee, "A scanisland based design enabling prebond testability in die-stacked microprocessors," in *Proc. IEEE Int. Test Conf.*, Oct. 2007, pp. 1–8.

[11] E. J. Marinissen, J. Verbree, and M. Konijnenburg, "A structured and scalable test access architecture for TSV-based 3D stacked ICs," in *Proc. IEEE 28th VLSI Test Symp.*, Apr. 2010, pp. 269–274.

[12] L. Jiang, Q. Xu, K. Chakrabarty, and T. Mak, "Integrated test-architecture optimization and thermal-aware test scheduling for 3-D SoCs under pre-bond test-pin-count constraint," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 9, pp. 1621–1633, Sep. 2012.

[13] K. Smith *et al.*, "Evaluation of TSV and micro-bump probing for wide I/O testing," in *Proc. IEEE Int. Test Conf.*, Sep. 2011, pp. 1–10.

[14] O. Yaglioglu and B. Eldridge, "Direct connection and testing of TSV and microbump devices using NanoPierce contactor for 3D-IC integration," in *Proc. IEEE VLSI Test Symp.*, Apr. 2012, pp. 96–101.

[15] B. Noia, S. Panth, K. Chakrabarty, and S. K. Lim, "Scan test of die logic in 3-D ICs using TSV probing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 2, pp. 317–330, Feb. 2015.

[16] X. Zhao, D. L. Lewis, H.-H. S. Lee, and S. K. Lim, "Low-power clock tree design for pre-bond testing of 3-D stacked ICs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 5, pp. 732–745, May 2011.

[17] D. H. Kim, K. Athikulwongse, and S. K. Lim, "A study of through-silicon-via impact on the 3D stacked IC layout," in *IEEE/ACM Int. Conf. Comput.-Aided Design-Dig. Tech. Paper*, Nov. 2009, pp. 674–680.

[18] S. Deutsch, K. Chakrabarty, S. Panth, and S. K. Lim, "TSV stress-aware ATPG for 3D stacked ICs," in *Proc. IEEE Asian Test Symp.*, Nov. 2012, pp. 31–36.

[19] M. Pathak, Y.-J. Lee, T. Moon, and S. K. Lim, "Through-silicon-via management during 3D physical design: When to add and how many?" in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2010, pp. 387–394.

**Shreepad Panth** (S'11–M'15) received the B.S. degree from Anna University, Chennai, India, in 2009, and the M.S. and Ph.D. degrees from the Georgia Institute of Technology, Atlanta, GA, USA, in 2011 and 2015, respectively.

He is currently a Design Engineer and member of the Technical Staff with Altera Corporation, San Jose, CA, USA. He has authored over 20 publications. His current research interests include all aspects of physical design for current and next-generation 3-D ICs.

Dr. Panth received the best paper award at the Asian Test Symposium in 2012 and the International Interconnect Technology Conference in 2014, and nominations for the best paper award at the International Symposium on Physical Design in 2014 and the Design Automation Conference in 2014.

**Sung Kyu Lim** (S'94–M'00–SM'05) received the B.S., M.S., and Ph.D. degrees from the University of California at Los Angeles, Los Angeles, CA, USA, in 1994, 1997, and 2000, respectively.

He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, in 2001, where he is currently the Dan Fielder Professor of Electrical and Computer Engineering. He led the Cross-Center Theme on 3-D Integration for the Focus Center Research Program with Semiconductor Research Corporation, Durham, NC, USA, from 2010 to 2012. His research on 3-D IC reliability was featured as Research Highlight in the Communication of the Association for Computing Machinery in 2014. He has authored the book entitled *Practical Problems in VLSI Physical Design Automation* (Springer, 2008). His current research interests include the architecture, circuit design, and physical design automation for 3-D ICs.

Prof. Lim was a member of the Design International Technology Working Group of the International Technology Roadmap for Semiconductors. He received the best paper award from the Techno Security & Forensics Investigations Conference in 2011 and 2012, the Asian Test Symposium in 2012, and the International Interconnect Technology Conference in 2014. His work was nominated for the best paper award at the International Symposium on Physical Design in 2006, the International Conference on Computer-Aided Design in 2009, the IEEE Custom Integrated Circuits Conference in 2010, the Design Automation Conference in 2011, 2012, and 2014, and the International Symposium on Low Power Electronics and Design in 2012.