Power, Performance, and Cost Comparisons of Monolithic 3D ICs and TSV-based 3D ICs

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***Abstract*— Power, performance, area, and cost analysis of TSV, mini-TSV, and monolithic 3D ICs is presented. Power savings for TSV, mini-TSV, and monolithic 3D ICs are 21%, 25%, and 37%, respectively, compared to that of a 2D IC. It is shown that monolithic 3D can deliver one node PPC benefit, whereas TSV 3D or mini-TSV 3D can only achieve a half node PPC advantage.**

Keywords—3D IC, Monolithic 3D, TSV, PPA, PPC, Cost

I. INTRODUCTION

Three-dimensional ICs (3D-ICs) have been shown to provide attractive solutions to extend Moore's Law [1-3]. In a 3D IC, multiple layers of ICs are connected by vertical vias that can vary in size from 5µm (Through Silicon Via, TSV) to 0.05µm (Monolithic Inter-Tier Vias, MIVs), offering a wide range of granularity in vertical connections. TSVs are used in block-level connections, whereas MIVs have a potential to offer vertical connections with a density reaching over 10 million/mm^2. In this work, we present a comprehensive study of power, performance, area, and cost comparisons among TSVs, mini-TSVs (TSV with diameter ~1µm), and MIVs. We show that MIVs are the most promising in terms of system-level power, performance, and cost benefit, with one node PPC (= Performance / (Power × Cost)) gain, whereas mini-TSVs and TSVs can only deliver a half-node PPC advantage.

II. DESIGN FLOW AND PPA COMPARISON

A. 3D IC Design Implementation

We first carry out RTL-to-GDSII implementation of interconnect-dominated LDPC benchmark in 2D, TSV-based 3D, mini-TSV-based 3D, and monolithic 3D using a 28nm technology (see Fig. 1). We use the 3D IC CAD tools presented in [4-5] that are shown to outperform commercial 2D IC design quality. All designs meet 1.1GHz target frequency (0.9ns clock period) so that we perform iso-performance power comparison among the four design options. The 3D IC footprint is exactly half the 2D IC, and hence, the total silicon area used remains the same. In addition to 2D vs 3D IC design comparisons, we also investigate the impact of the number of monolithic inter-tier vias (MIVs) on power saving. The {diameter, capacitance, resistance} used for TSV, miniTSV, and MIV in our experiments are {5µm, 20fF, 40mΩ}, {1µm, 2fF, 60mΩ}, and {0.1µm, 0.2fF, 200mΩ}, respectively.

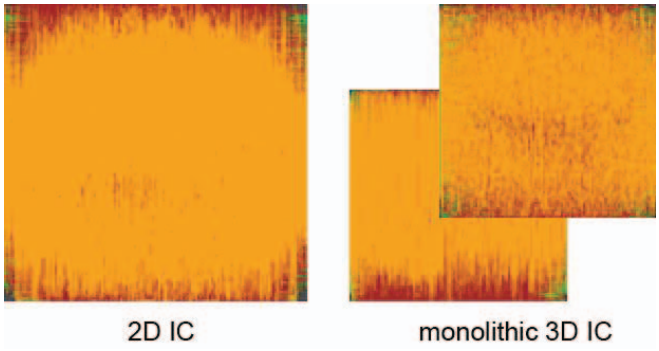

Fig. 1. GDSII layouts of 2D IC and monolithic 3D IC for interconnect-dominated LDPC (low density parity-check code) benchmark.

Table I. Power comparison across different implementations of LDPC. All power numbers are in mW.

	# timing buffer	net pwr	cell pwr	total pwr	# via
2D	74,000	585.7	82.3	702	-
TSV	56,962	470.2	70.6	558	6,989
mini-TSV	54,403	441.2	65.6	524	6,989
monolithic	47,098	363.2	56.6	442	45,528

B. Design Results and Power Comparison

Power comparison of the four different implementations is shown in Table I. It is well-known that 3D ICs offer a significant reduction in wire length. Since LDPC design is interconnect-dominated, these wire length savings directly translate to interconnect switching power and the total power savings: 21% for TSV 3D, 25% for mini-TSV 3D, and 37% for Monolithic 3D (M3D). Due to shorter wires, the number of timing buffers is also reduced in 3D ICs, therefore, reducing the cell power further.

A large number of MIVs with small capacitance provides the maximum benefits for M3D. Such a large number of vias cannot be used in TSV-based designs because of the significant area penalty and high TSV capacitance. However, it is also found that too many MIVs can also lead to routing congestion in the bottom tier metal layers, which increases wire length and power (see Fig. 2).

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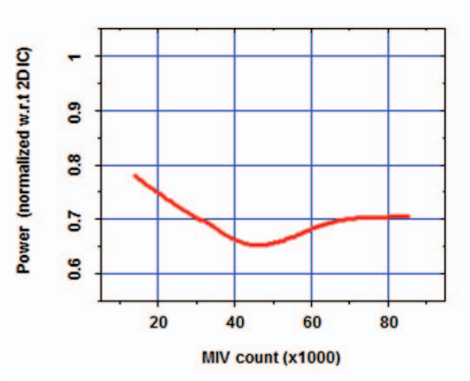

Fig. 2. Impact of MIV count on the overall power reduction in monolithic 3D IC for LDPC benchmark.

III. Node Advancement Benefits of 3D ICs

Besides the size of inter-tier vias, the PPC quality of 3D ICs also depends heavily on the total usage that is determined by tier-partitioning. In each 3D IC via option shown in Table II, three different via usages are used: "few", "medium" and "many" refer to the total via count relative to the total gate count in the design. For monolithic 3D, cost advantage is clearly seen, as the bottom tier uses only 2 to 4 metal layers. But, other options (TSV and mini-TSV) use almost all metal layers (full). For the "many" TSV option, our study shows that the number of metal layers needed is high (full+1), while the footprint becomes excessively large.

TABLE: II. Metal layer usage in three different via count options for a 1M gate design.

bottom tier metal layers			
MIV/TSV	many ~100K	medium ~10K	few ~1K
M3D	2	2	4
mini-TSV	full-1	full	full
TSV	full+1	full	full
top tier metal layers			
MIV/TSV	many	medium	few
M3D	full-2	full-1	full
mini-TSV	full-1	full	full
TSV	full+1	full	full

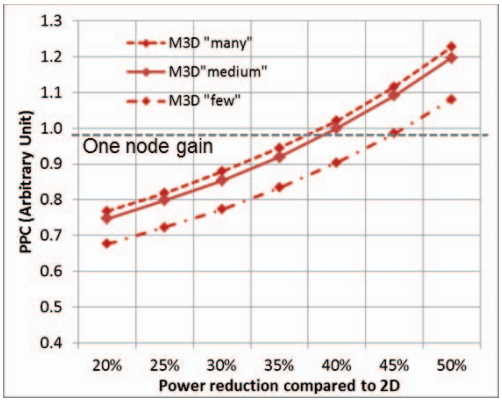

Fig. 3. PPC comparison for monolithic IC under three via counts.

Fig. 3 shows PPC comparison for M3D using three via count options. Assuming we achive a 40% power reduction with M3D ("many" and "medium") against its 2D IC counterpart, PPC gain becomes equivalent to one technology node advancement. That means an M3D built in 14nm technology node, if die partitioning and physical design are highly optimized, can match the PPC performance of a 2D IC built in 10nm. Next, we observe that going from "medium" to "many" has little impact on M3D PPC. However, when the via count reduces from "medium" to "few", PPC drops by 10%.

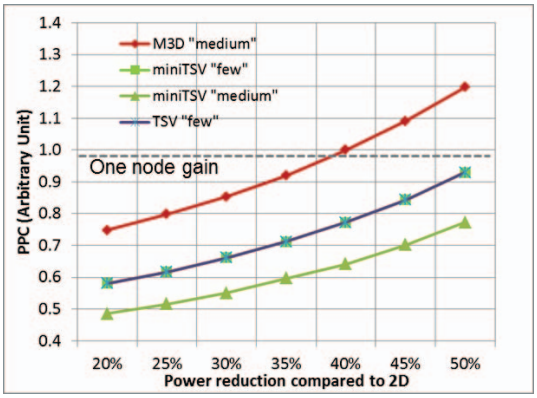

Fig. 4. PPC comparison among M3D, mini-TSV, and TSV.

We compare three different via technologies in Fig. 4. We first observe that mini-TSV and TSV deliver only a half-node PPC advantage even with rigous power optimization. Second, the PPC sensitivity to via count in mini-TSV is opposite to that found in M3D case (Fig. 3). PPC value in mini-TSV degrades by 17% when more vias are used, which is mainly due to its area overhead. Lastly, both TSV and mini-TSV, if their via usage is "few", show comparable PPC. This is because both design options do not exploit the full benefits of 3D IC vias.

IV. Summary

Three design options are analysed for 3D IC implementation. It is shown that monolithic 3D can deliver one node PPC advantage, whereas TSV-based 3D designs achieve only half a node benefit.

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