Full-Chip Signal Integrity Analysis and Optimization of 3-D ICs

Taigon Song, *Student Member, IEEE*, Chang Liu, Yarui Peng, *Student Member, IEEE*, and Sung Kyu Lim, *Senior Member, IEEE*

***Abstract*— Through-silicon-via (TSV)-to-TSV coupling is a new phenomenon in 3-D ICs, and it becomes a significant source of signal integrity problems. The existing studies on its extraction and analysis, however, become inaccurate when handling more than two TSVs on full-chip scale. In this paper, we investigate the multiple TSV-to-TSV coupling issue and propose a model that can be efficiently used for full-chip extraction. Then, we perform an analysis on the impact of TSV parasitics on coupling and delay. Unlike the common belief that only the closest neighboring TSVs affect the victim, this paper shows that nonneighboring aggressors also cause nonnegligible coupling noise. Based on these observations, we propose an effective method of reducing the overall coupling level.**

***Index Terms*— 3-D IC, coupling, crosstalk, full chip, signal integrity (SI), through-silicon via (TSV).**

I. Introduction

THROUGH-SILICON-VIA (TSV) and 3-D integrated circuits (3-D ICs) are expected to be the key technology trend in high-performance and low-power systems [1]. In 3-D ICs, dies are stacked vertically, and transistors in different dies are connected by TSVs. TSVs are smaller than off-chip wires, thereby enabling ultrawide bandwidth and high-speed communication between dies. Industries have started designing 3-D DRAMs using TSVs [2], and academia are reporting the impact of TSVs on 3-D ICs in [3] and [4].

One of the essential signal integrity (SI) characteristics in studying TSVs is coupling. In 2-D ICs, metal-to-metal is the main source of noise coupling. Two adjacent metal wires form a parallel capacitor, and noise voltage travels from an aggressor to a victim through close metal wires (capacitive coupling). However, in 3-D ICs, two adjacent TSVs form a complex coupling network due to its surroundings. TSV-to-TSV coupling forms not only a capacitive coupling network but also other complex coupling networks. These coupling networks cause significant coupling noise between two adjacent TSVs. Therefore, a signal path that includes TSVs can suffer from significant noise in 3-D ICs.

In this paper, therefore, we study the multiple TSV-to-TSV coupling effect inside 3-D ICs on a full-chip level. We describe the true phenomena that take place inside the ICs, and propose a compact model that captures the coupling effect among multiple TSVs. Then, we propose a methodology that performs an analysis of multiple TSV coupling on a full-chip level. Based on our methodology, we also study the critical factors that affect noise coupling and delay in 3-D ICs.

The main contributions of this paper include the following.

1) *Nonneighboring Aggressor Impact on TSV-to-TSV Coupling*: Unlike on-chip wires, we show that TSV coupling is affected by both the closest and nonneighboring aggressors.
2) *A Compact Multiple TSV-to-TSV Coupling Model and an Extraction Algorithm*: To the best of our knowledge, we propose the first compact multiple TSV-to-TSV coupling model and an extraction algorithm that can be applied on a full-chip level.
3) *Impact of Process Parameters on Noise and Delay*: We show that the full-chip noise/delay does not increase significantly as in single-net studies, and that 3-D net delay is not sensitive to neighbor TSV distance as in 2-D net.
4) *TSV Coupling Optimization*: We propose a design optimization methodology that reduces TSV-to-TSV coupling in large-scale full-chip 3-D IC designs.

II. Motivation

This section describes the motivation of this paper and shows our findings. We also show why [5] is inaccurate. In this paper, we use the TSVs with a diameter of 5 μm, a height of 60 μm, a SiO_2 liner of 0.5 μm, and a minimum pitch of 15 μm.

A. Maximum Coupling Capacitance

Liu *et al.* [5] assumed that the silicon substrate capacitance depends only on the distance between two TSVs. However, when a victim TSV is surrounded by more than one aggressor, the total coupling capacitance of the silicon substrate has a maximum limit, and does not increase linearly. Many TSV modeling papers [5], [6] claim that the silicon substrate

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T. Song, Y. Peng, and S. K. Lim are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: taigon.song@gatech.edu; yarui.peng@gatech.edu; limsk@ece.gatech.edu).

C. Liu is with Broadcom Corporation, Irvine, CA 92617 USA (e-mail: changliu@broadcom.com).

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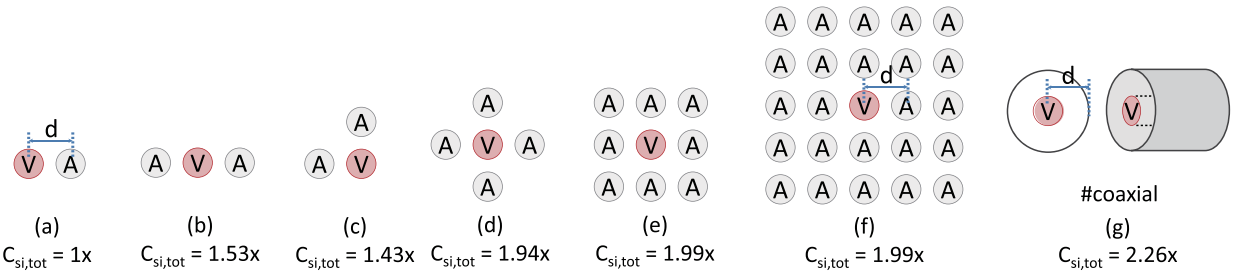

Fig. 1. Illustration showing (a)–(f) nonlinear capacitance increase when the number of aggressors increases and (g) maximum limit of coupling capacitance of a TSV.

capacitance follows (1), which is the capacitance between two parallel, circular conducting wires:

$$C_{\text{si}} = \frac{\pi \epsilon_0 \epsilon_{\text{si}} L}{\ln[(P/2r) + \sqrt{(P/2r)^2 - 1}]} \tag{1}$$

where ϵ_{si}, L, P, and r are the permittivity of the silicon substrate, the height of the TSVs, the pitch between the TSVs, and the radius of the TSVs, respectively. By (1), when the coupling capacitance between an aggressor and a victim in a certain pitch is $1\times$, the victim will see $8\times$ coupling capacitance when there are eight aggressors in every direction.

However, (1) is correct only when there are no other neighbors near the two TSVs. When TSV aggressors are close to another aggressor, the total substrate capacitance that a victim sees will increase, but it will not increase linearly. Fig. 1 illustrates this when the radius is 2 μm and the pitch between the TSVs is 10 μm. We simulated the total coupling capacitance using Synopsys Raphael when different numbers of aggressors are near a victim TSV. Fig. 1 shows that, although more TSVs are near the victim, the increase in the total coupling capacitance is minor. For example, Fig. 1(d) has two more aggressors than Fig. 1(c), but the total capacitance increase is only $0.51\times$. For Fig. 1(e), four more aggressors are added than Fig. 1(d), but the capacitance increase is only $0.05\times$. From this paper, we show that (1) cannot be used for a multiple TSV coupling analysis. We also emphasize that, even when there are the same numbers of aggressors, TSV coupling capacitance changes when aggressors are in different locations. For example, Fig. 1(b) and (c) has the same numbers of aggressors, but the total capacitance is different by $0.1\times$. This is because the E-field that forms capacitance changes due to the different locations of the TSVs. Thus, we conclude that the coupling capacitance is a function of aggressor locations, as well as a function of distance.

We show that a maximum substrate capacitance limit exists for a TSV victim when the radius (r) and the minimum pitch (P) are given. Even when an infinite number of aggressors are near a victim, the maximum substrate capacitance cannot be larger than that of a coaxial TSV, whose inner conductor radius is r, and the outer conductor's inner radius is $P - r$. We show this formula of a coaxial TSV in (2) [7]

$$C_{\text{si,max}} = \frac{2\pi \epsilon_0 \epsilon_{\text{si}} L}{\ln((P-r)/r)}. \tag{2}$$

Regardless of how many aggressors surround a victim TSV, the total sum of TSV coupling capacitance will be smaller than (2). In other words, no matter how many aggressors surround a victim [as shown in Fig. 1(f)], the E-field between the victim and the aggressors cannot be formed as strongly as a coaxial TSV [Fig. 1(g)]. Although the values of the maximum coupling capacitance will vary on different TSV radii and pitches, when the radius is 2 μm and the minimum pitch between the TSVs is 10 μm, the maximum capacitance will be $\sim 2.26\times$.

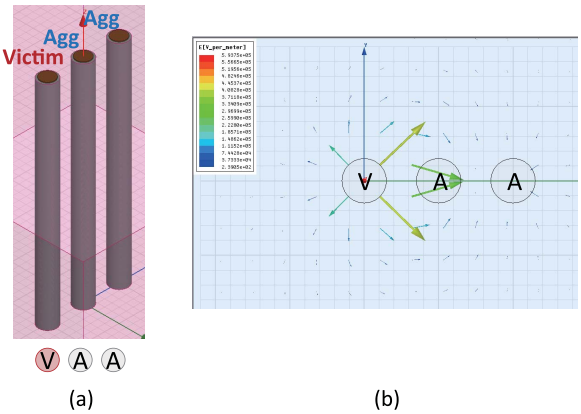

Fig. 2. Neighbor effect. (a) Two-aggressor model in HFSS. (b) E-field distribution between the TSVs.

B. Neighbor Effect on TSV Coupling

Unlike the common belief that only the nearest aggressors impact TSV coupling, TSV coupling occurs even between the nonneighboring aggressors. Assume that a simple layout where a victim TSV is neighboring two aggressor TSVs in a straight line [see Fig. 2(a)]. We performed modeling using the proposed model in Section III-A, and the model was validated using the Ansys High Frequency Structural Simulator (HFSS). We intuitively think that the far aggressor will not affect coupling, because a closer neighbor is nearby. However, Fig. 3 shows that the far aggressor affects as much coupling voltage (139.6 mV) as the close aggressor (184.6 mV) when 1-GHz signal is applied in 45-nm transistors. This is because the far aggressor also has a nonnegligible amount of capacitance between the victims (close aggressor: 9.46 fF and far aggressor: 4.14 fF) [see Fig. 4 (Case 3)]. Though the close aggressor shields some of the E-field between the victim and the far aggressor, the E-field detours the first aggressor and forms the capacitance between the far aggressor and the victim [see Fig. 2(b)

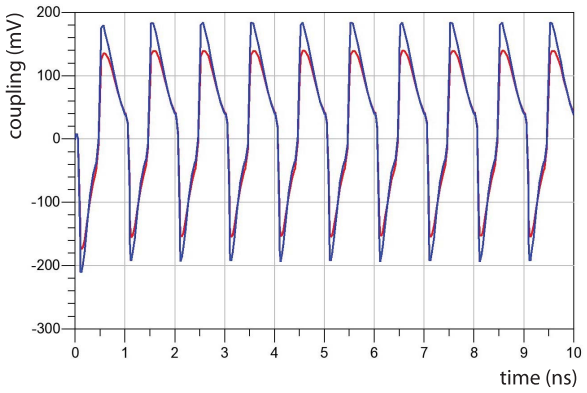

Fig. 3. Coupling voltage of the near (blue) and far (red) aggressors shown in Fig. 2.

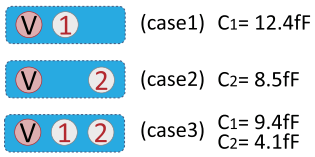

Fig. 4. Neighbor effect case study on how neighbor TSVs affect other aggressors.

field distribution simulated using Ansys Q3D]. In addition, despite the far aggressor has <50% capacitance of the close aggressor, V_{far} reduces by only 40 mV. This is because of the complex coupling network that TSVs compose explained in [8].

In addition, neighbor TSVs reduce the capacitance of other TSVs. Fig. 4 describes the far aggressor impact on capacitance. Assume that there are only two TSVs as Case 1 and Case 2. Each capacitance is 12.4 fF (near aggressor) and 8.5 fF (far aggressor). However, when two aggressors are together (Case 3), the coupling capacitance of both the aggressors decreases to 9.4 and 4.1 fF. This is because the TSVs correlate to each other and create a new E-field distribution. We call this the neighbor effect. Therefore, we conclude that the coupling capacitance is a function of distance, location, and also a function of neighbors [9], [10].

III. Multi-TSV Coupling Extraction

In this section, we propose a multiple TSV-to-TSV coupling model and an extraction algorithm for a full-chip analysis.

A. Compact Multi-TSV Coupling Model

Chang *et al.* [11] proposed a multiple TSV model that can be used when performing a coupling analysis. However, this model consists of many *RLC* components even when modeling few TSVs. Thus, we propose a compact multiple TSV-to-TSV coupling model that can be easily used on a full-chip analysis. Fig. 5(a) and (b) shows the original model and our proposed model, respectively. Since modern digital systems operate in a clock frequency below 10 GHz, we target our model to be valid in this range.

1) Silicon Substrate (C_{si} and R_{si}) and Model Simplification: We explain the concepts used in [11] to describe the formulas used in our model. Assume that three aggressors ($N = 3$)

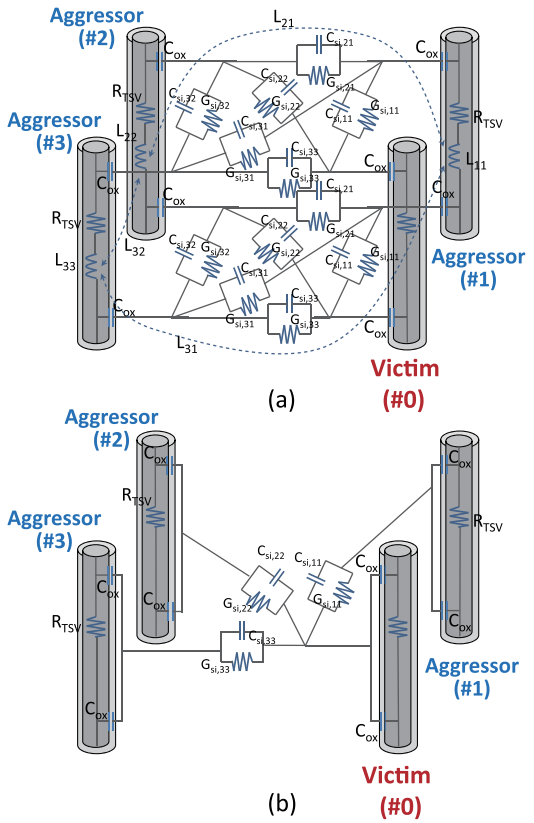

Fig. 5. (a) Original model proposed in [11]. (b) Our proposed compact TSV model for a full-chip analysis.

are near a victim. An $N + 1$ system considers to become an N-conductor transmission line. Using the multiconductor transmission line theory, a TSV must be assumed as the reference. Thus, we will assume this to be the victim TSV (#0). Therefore, the victim TSV does not have inductance, but it only has resistance. A TSV is expressed as a resistor (R_{TSV}) and an inductor (L_{TSV}) in series. A SiO_2 liner surrounds the TSV for isolation, and is expressed as a capacitor (C_{ox}). A silicon substrate can be expressed as a resistor ($R_{\text{si},ij}$) and a capacitor ($C_{\text{si},ij}$) in parallel, of which is the resistance and the capacitance between aggressor i and aggressor j. When $i = j$, it is the resistance and the capacitance of the substrate between the victim and the aggressor.

For $R_{\text{si},ii}$ and $C_{\text{si},ii}$, we start by calculating $L_{\text{si},ij}$, which is the substrate inductance between two TSVs. $\mathbf{L}_{\text{si}}$ is expressed in matrix ($[L_{\text{si}}]$), and consists of self-loop inductance and mutual-loop inductance. By definition, $L_{\text{si},ii}$ indicates the substrate inductance between the victim and the aggressor i. The following equations describe how to calculate these values:

$$L_{\text{si},ii} = \frac{\mu L}{\pi} \ln\left[\frac{P_{i0}}{r + t_{\text{ox}}}\right] \tag{3}$$

$$L_{\text{si},ij} = \frac{\mu L}{2\pi} \ln\left[\frac{P_{i0} P_{j0}}{P_{ij}(r + t_{\text{ox}})}\right] \tag{4}$$

where P_{i0} is the pitch between the victim TSV (#0) and the aggressor TSV(#i), and P_{ij} is the pitch between two aggressor TSVs (#i and #j). By the relation between the inductance matrix and the capacitance matrix in a homogeneous

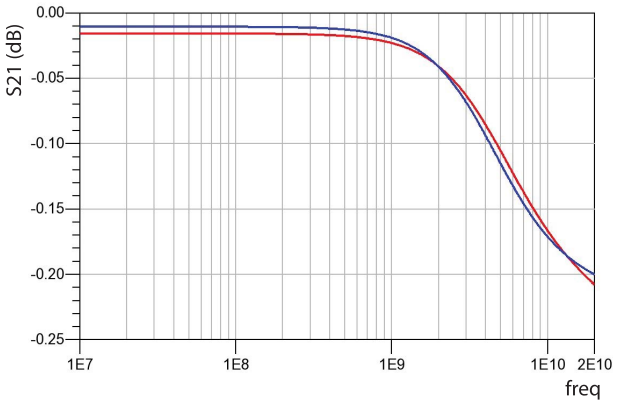

Fig. 6. S-parameter comparison between our model and HFSS. Red curve: HFSS. Blue curve: our model.

medium [12], we calculate matrix $\mathbf{C}_{\rm si}$

$$\mathbf{C}_{\rm si} = \mu_0 \epsilon_0 \epsilon_{\rm si} L^2 {\mathbf{L}_{\rm si}}^{-1} \tag{5}$$

where $\mathbf{C}_{\rm si}$ and its inner components $C_{{\rm si},ij}$ are defined as

$$[C_{\rm si,ij}] = \begin{bmatrix} \sum_{k=1}^{N} C_{1k} & -C_{12} & \dots & -C_{1N} \\ -C_{21} & \sum_{k=1}^{N} C_{2k} & \dots & -C_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ -C_{N1} & C_{N2} & \dots & \sum_{k=1}^{N} C_{Nk} \end{bmatrix} \tag{6}$$

and the conductance matrix $\mathbf{G}_{\rm si}$ is defined

$$\mathbf{G}_{\rm si} = \frac{\sigma}{\epsilon_0 \epsilon_{\rm si}} \mathbf{C}_{\rm si}. \tag{7}$$

In our model, we only use $C_{{\rm si},ii}$ and $G_{{\rm si},ii}$ ($R = 1/G$). The other RLC components are reduced. This is reasonable, because we only consider the impact between a victim and an aggressor and not the impact between two different aggressors. Using our model, we reduce the RLC count by 60% when $N = 3$. The RLC count reduces more as N increases. Despite the RLC reduction, our model is shown accurate, as described in Section III-A5.

2) Inductance Modeling (L_{ij}): We remove self-inductance and mutual inductance in our TSV model. This is reasonable due to the following reasons. First, the TSV inductance, which is in few tens of pH range, has a negligible impact on delay and coupling noise on the frequency range of digital circuits (<10 GHz). For example, the impact of TSV inductance (self and mutual) on delay and coupling noise is <2% in 1-GHz clock. This means that, in digital circuits, capacitive coupling is the dominant coupling factor, and inductive coupling is almost negligible. This is shown in Fig. 6 that even though inductance is removed in our model, the S-parameter comparison shows a good correlation between the 3-D EM simulator model and our simplified model. Despite that TSV scaling leads to the possibilities of TSV inductance increase due to pitch decrease, note that the TSV size also scales as the TSV pitch reduces. Thus, TSV inductance remains in the pH range despite the technology scaling. Due to these reasons, since inductive coupling is almost negligible, we remove inductance from our model.

3) Resistance of the TSV (R_{TSV}): In TSVs, a skin effect occurs on theac current that flows inside. Thus, as frequency increases, $R_{\rm TSV}$ starts increasing from a certain frequency point. Equation (8) describes the formula for $R_{\rm TSV}$

$$R_{\rm TSV} = \frac{L}{2\pi r}\sqrt{\frac{\pi f \mu_0}{\sigma_c}} \tag{8}$$

where μ_0 denotes the permeability of free space, f is the frequency, and σ_c is the conductivity of copper. For example, in a 5-μm diameter TSV, the resistance starts increasing from 700 MHz due to the skin effect. As the TSV diameter scales, the frequency that starts increasing $R_{\rm TSV}$ due to the skin effect will increase. This is because smaller TSVs (in diameter) will approach the skin depth in a higher frequency than in larger TSVs.

4) Capacitance of the Liner (C_{ox}): For $C_{\rm ox}$, SiO_2 liner surrounding the TSV can be modeled as the capacitance of the liner itself and the MOS capacitance [13] of the TSV in parallel

$$C_{\rm ox} = \frac{C_{\rm dep} C_{\rm liner}}{C_{\rm dep} + C_{\rm liner}} \tag{9}$$

$$C_{\rm liner} = \frac{2\pi \epsilon_0 \epsilon_{\rm ox} L}{\ln\left(\frac{r+t_{\rm ox}}{r}\right)} \tag{10}$$

$$C_{\rm dep} = \frac{2\pi \epsilon_0 \epsilon_{\rm si} L}{\ln\left(\frac{r+t_{\rm ox}+t_{\rm dep}}{r+t_{\rm ox}}\right)} \tag{11}$$

where $t_{\rm dep}$ is the thickness of the depletion region. In our assumption, when the substrate doping is $10^{15}/{\rm cm}^3$, note that a depletion region always exists around TSVs in digital systems that operate between 0 V and VDD.

5) Model Validation: To validate our model, we first place aggressor TSVs around the victim TSV randomly in a fixed space. Then, we perform modeling using 3-D EM solver HFSS, and also generate a SPICE netlist based on our compact model. We generate ten layouts for each sample case, and then compare the S-parameter of these two and report the maximum error of insertion loss. Fig. 6 shows the S-parameter comparison when $N = 3$, and Table I shows the validation result. We show that our model is very accurate, even in a multiple TSV structure, by reporting the maximum difference in insertion loss less than 0.02 dB.

B. Extraction Algorithm

In our previous discussions (Sections II-A and II-B), we showed that TSV coupling capacitance is a function of distance, location, and neighbor aggressors. To extract TSV-to-TSV coupling capacitance accurately, an approach considering only the closest neighbor or limiting the maximum target distance to calculate coupling capacitance cannot be used. Therefore, we propose an algorithm that considers distance, direction, and neighbor effect all in a holistic manner when extracting the coupling capacitance for all nets in the layout for a full-chip analysis. Algorithm 1 describes this.

Algorithm 1 Multiple TSV-to-TSV Capacitance Extraction

```
Algorithm: Multiple TSV-to-TSV capacitance extraction
Locate all TSVs by its coordinate (x,y);
while for all victim TSVs do
    For all neighbor TSVs, calculate the Euclidean
    distance and sort by the closest distance to the victim;
    Choose N aggressors that is closest to the victim;
    Calculate the coupling capacitance of the
    N aggressors using the formula in Section III-A;
    if The calculated TSV capacitance is higher than C
    then
        Generate a coupling network between the
        aggressor and the victim;
    else
        Assign the TSV coupling capacitance to be zero;
    end
end
```

TABLE I
MODEL VALIDATION ON GENERAL LAYOUTS

TSV dimensions (μm)			# TSVs	Average err (dB)	Max. err (dB)
Radius	Pitch	Height			
2	5	30	6	0.008	0.016
			8	0.011	0.015
			10	0.008	0.014
			12	0.011	0.015
		60	6	0.009	0.015
			8	0.011	0.016
			10	0.011	0.015
			12	0.008	0.014
4	10	30	6	0.010	0.016
			8	0.009	0.014
			10	0.011	0.017
			12	0.011	0.018
		60	6	0.010	0.017
			8	0.009	0.014
			10	0.010	0.015
			12	0.008	0.014

In an actual layout, any TSV can become a victim from noise. Therefore, our full-chip 3-D SI analysis flow described in Section IV-A analyzes the coupling noise in every net of the chip. Thus, our algorithm must be performed for every TSV. From a given layout, we first extract the (x, y) coordinate of each TSV. Starting from the very first TSV of the layout, we assume this to be a victim and sort all neighbor aggressor TSVs by the closest Euclidean distance to the victim. Then, we choose N neighbor aggressor TSVs (N: a significantly large number) from the sorted result that are closest from the victim and calculate the capacitance between the victim and the chosen aggressors. Once we calculate the capacitance of the aggressors, we create a coupling network between the victim and the aggressor that the capacitance is higher than a certain value (e.g., C $>$ 0.01 fF). This step is repeated for every TSV in the layout, and we create the corresponding coupling network for each victim TSV.

IV. FULL-CHIP ANALYSIS

Using our extraction flow, we perform a full-chip SI analysis in this section, and compare our results with those in [5].

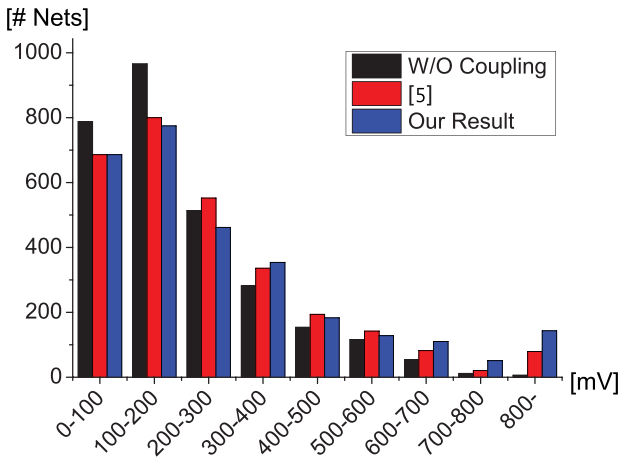

Fig. 7. Coupling analysis results. x-axis: noise voltage bins. y-axis: number of nets contained in the specific bin.

A. Full-Chip 3-D SI Analysis Flow

Since the existing SI analysis tools cannot analyze 3-D circuits accurately, we modified the 3-D SI analysis flow in [5] to implement our results. First, we extract the standard parasitic exchange format (SPEF) file for each die using an *RC* extraction tool. Then, we run our script that implements the algorithm developed in Section III-B to create the SPEF file of TSV parasitics. Then, we create a top-level verilog file. Once these files are prepared, we use Synopsys PrimeTime to read the verilog file, and create a top-level stitched SPEF file that contains the *RC* information of all dies and the TSVs. This step inserts the extracted coupling network from Section III-B into the SPEF file. Then, we analyze the stitched SPEF file and generate a SPICE netlist for each individual net for performing coupling noise simulation. The SPICE netlist has all the coupling information, including wire coupling, TSV coupling network by the extraction algorithm, and the aggressor signal, and the victim driver models. We run HSPICE on each net one by one, assuming the aggressors are switching and reporting the peak noise at each port.

B. Design and Analysis Results

We designed fast Fourier transform (FFT) 256-8, which is a 256-point with 8-bit precision, real and imaginary, FFT as a test circuit. The circuit has 140k gates and 211 TSVs. The design is a two-tier 3-D IC based on the Nangate 45-nm technology. The designs were based on our Cadence Encounter design flow to generate 3-D layouts [14]. In Fig. 7 and Table II, the coupling analysis results of top-hierarchy nets, which are around 3k, are shown. We compare our results with those in [5]. For example, in Fig. 7, without coupling analysis shows ~800 nets in the 0–100-mV bin, and [5] and our results show ~700 nets in the 0–100-mV bin.

Based on the results, we see the following impacts. First, for coupling noise, both the approaches calculate higher coupling noise than without TSV coupling (590 V). Total coupling noise is the sum of coupling noise voltage that is

TABLE II

TSV COUPLING IMPACT ON CROSSTALK AND TIMING. COUPLING NOISE IN VOLT, LPD IN NANOSECOND, AND TNS IN NANOSECOND

	W/O coupling	W/ coupling [5]	W/ coupling (Our results)
Footprint (mm^2)	0.7954	0.7954	0.7954
Tot. coupling noise	590.77 V	732.75 V	787.42 V
Longest path delay	2.734 ns	3.165 ns	2.852 ns
Total negative slack	-61.65 ns	-115.07 ns	-75.24 ns

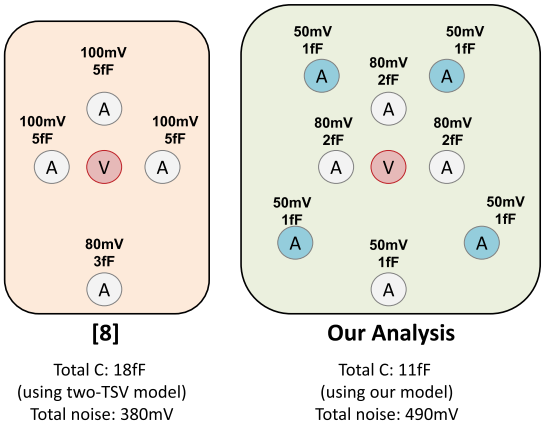

Fig. 8. Why delay and noise trend is different. Left: analysis in [5]. Right: our analysis.

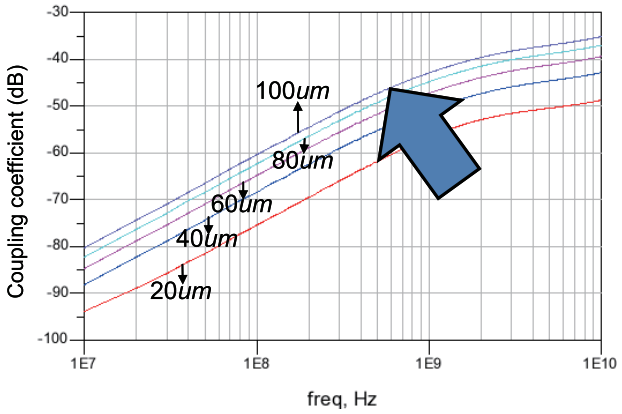

Fig. 9. S-parameter simulation of coupling coefficient with different TSV heights (20–100 μm).

TABLE III

FULL-CHIP 3-D NOISE: IMPACT OF TSV PARAMETERS

TSV height	20μm	40μm	60μm	80μm	100μm
3D noise (V)	155.1	169.2	180.3	189.5	197.1
Ratio (%)	0	9.0	16.2	22.1	27.1
Liner thickness	0.1μm	0.2μm	0.3μm	0.4μm	0.5μm
3D noise (V)	204.2	194.9	188.6	184.0	180.3
Ratio (%)	0	-4.6	-7.6	-9.9	-11.7
TSV diameter	2μm	4μm	6μm	8μm	10μm
3D noise (V)	180.3	199.6	226.0	251.2	256.1
Ratio (%)	0	10.7	25.3	39.3	42.0

occurred on each net. Note that, when noise voltage occurring on a particular net exceeds a certain threshold, the logic value will be inverted leading to erroneous behaviors inside circuits. More total coupling noise in a layout means that the particular design is more prone to logic failures statistically. Despite [5] overestimating the coupling capacitance by linear superposition, our results show higher total noise voltage. The total coupling noise is 732 V using the flow in [5] and 787 V in our results. This is because our model considers more neighbor aggressors than [5] that should not be ignored. Note that 196.65 V (787.42 V − 590.77 V) is the noise that has been generated due to TSV coupling. In this paper, we will define this TSV-induced noise as 3-D noise.

Second, for a timing analysis, because [5] overestimates the total coupling capacitance, it also overestimates the timing degradation by TSVs as well. We save a significant timing margin using an accurate TSV model. Note that the longest path delay (LPD) and the total negative slack (TNS) depend on the total capacitance formed between the aggressor TSVs, and the coupling noise depends on the number of aggressors formed between the victims. TNS is the sum of the negative slack for all the paths that fail any timing constraint. LPD tells the designer what the maximum clock period could be, and TNS shows how far the circuit is from reaching timing closure. Fig. 8 shows how noise and delay trend is different compared with [5]. In terms of timing, the most important factor is the total capacitance. Despite [5] considering less aggressors, it overestimates capacitance. Thus, the total capacitance formed from aggressors are larger than that of our analysis (18 fF > 11 fF). However, in terms of noise, the most important factor is the number of effective aggressors. Note that a small capacitance formed between the aggressor and the victim could lead to a big coupling voltage (Section II-B). Since our analysis considers more effective aggressors, we analyze more coupling noise than in [5].

V. IMPACT OF PROCESS PARAMETERS ON TSV COUPLING

This section studies the impact of process parameters on TSV coupling in terms of coupling coefficient and full-chip impact. For the full-chip results, we vary the TSV parameters on the design performed on Section IV to gain understanding of how these parameters impact the full-chip design.

A. TSV Height

We first study the impact of TSV height. TSV height is determined by the die thickness. With a shorter TSV height, the TSV resistance and capacitance reduce, which is good for reducing TSV-induced coupling. Therefore, die thinning is one of the keys to a good TSV technology. In this paper, we analyze when the TSV height is from 20 to 100 μm. We see that the coupling coefficient increases monotonically with the TSV height as expected (Fig. 9). This is because all TSV parasitics are linearly proportional to TSV height. In terms of full-chip results (Table III), TSV height increase leads to additional 3-D noise. Notice that the 5× TSV height increase does not lead to the 5× coupling noise increase due to the complicated TSV coupling network [8]. Comparing

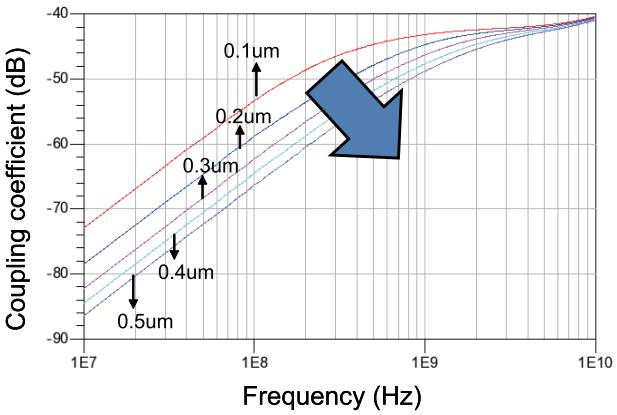

Fig. 10. S-parameter simulation of coupling coefficient with different liner thickness (0.1–0.5 μm).

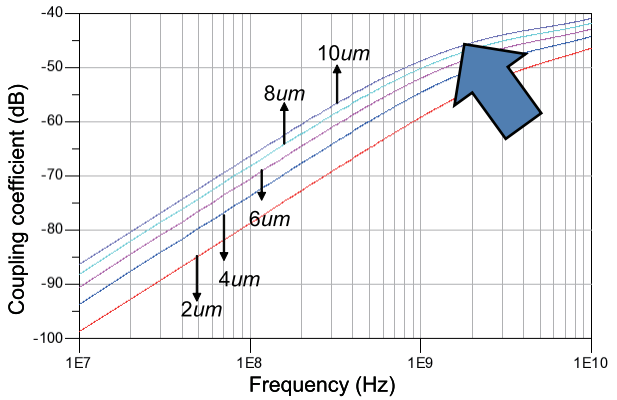

Fig. 11. S-parameter simulation of coupling coefficient with different TSV diameters (2–10 μm).

20 and 100 μm TSVs, we see 27.1% 3-D noise increase due to the TSV height increase.

B. Liner Thickness

TSV liner also has a significant impact on TSV capacitance. The thickness of the TSV liner varies from 0.1 to 0.5 μm, and we report the coupling coefficient. In Fig. 10, as we increase the liner thickness, the coupling coefficient decreases in the low-frequency region but not in the high-frequency region. Liner capacitance contributes only in the low-frequency region due to its size and geometry inside the coupling network. Thus, coupling impact due to liner capacitance will reduce as the operating frequency increases. In our full-chip study (Table III), changing the liner thickness from 0.1 to 0.5 μm leads to -11.7% 3-D coupling noise difference.

C. TSV Diameter

TSV diameter affects both the TSV capacitance and the resistance. A bigger TSV diameter helps to reduce the TSV resistance. However, due to the increased TSV oxide area, the TSV capacitance will increase significantly. Usually, the TSV resistance is very small (50 mΩ). Thus, the TSV capacitance (50 fF) is usually the dominant factor of the TSV parasitics. Since the TSV capacitance has a dominant role in the TSV coupling, we predict that a bigger diameter will increase the coupling noise. Fig. 11 shows the analysis results. With a bigger TSV diameter, coupling coefficient increases as expected. In full-chip results (Table III), the TSV radius change showed the highest noise difference (42%) within the given range of variation. In addition to the TSV capacitance increase when the TSV diameter increases, note that TSV-to-TSV distance also reduces, which further enhances the TSV-to-TSV coupling.

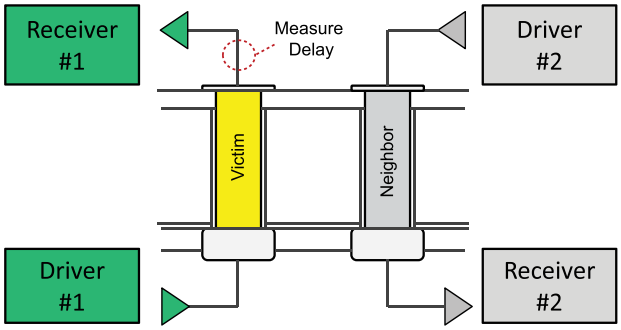

Fig. 12. Single net-delay analysis model of a TSV having one neighbor TSV.

VI. Impact of Process Parameters on Delay

This section studies the impact of TSV process parameters on timing and delay. To analyze the TSV impact on delay, we propose an impedance load analysis method.

A. Analysis Structure for Single Net-Delay Study

Fig. 12 shows our structure for the single net-delay study on 3-D TSV. In our model, Driver (standard cell) #1 on the bottom-left drives the victim TSV, and we measure the delay at the node on Receiver #1. We include a neighbor TSV and its driver and a receiver on its right to see the impact of neighbor TSVs on delay. Note that Driver #2 is not switching. The Driver #1 size varies from the minimum ($1\times$) to the biggest ($16\times$), and the receiver size is the same as the driver size.

B. Impact of TSV Height, Liner Thickness, and TSV Radius

Fig. 13(a)–(c) shows the delay impact of TSV height, liner thickness, and TSV radius, respectively. As described in Section V, we see a similar trend in delay too. When the TSV height increases, both the TSV resistance and the TSV capacitance increase. Thus, the delay increases as the TSV height increases, as shown in Fig. 13(a). When the SiO_2 liner thickness increases, the TSV resistance remains the same, but the TSV capacitance reduces. Thus, the delay decreases as the liner thickness increases, as shown in Fig. 13(b). When the TSV radius increases, despite that TSV resistance reduces, the TSV capacitance increases significantly. Thus, the delay increases as the TSV radius increases, as shown in Fig. 13(c). Note that the delay in drivers stronger than $8\times$ is not significant from parameter changes. In other words, the drivers must be strong enough to minimize the delay impact on 3-D TSV nets.

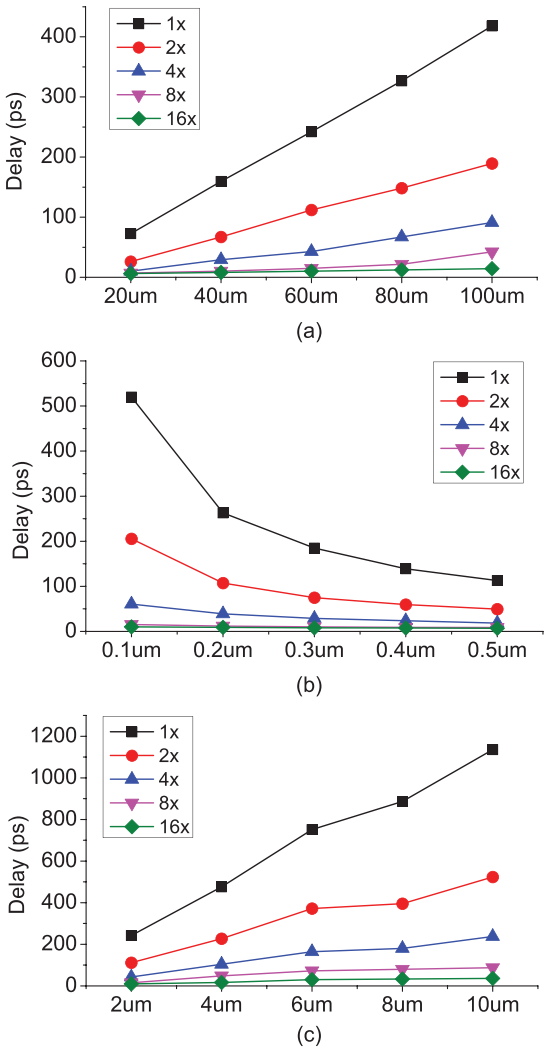

Fig. 13. Delay impact on various TSV parameter changes when the driver (standard cell) size changes (1× to 16×). (a) TSV height. (b) Liner thickness. (c) TSV radius.

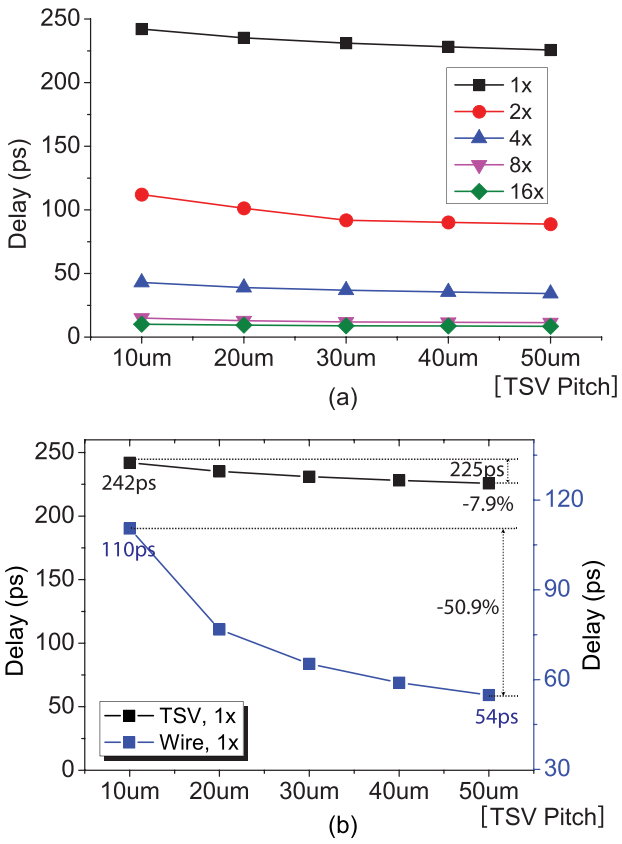

Fig. 14. Delay impact when TSV pitch changes. (a) Driver sizes from 1× to 16×. (b) Comparison between 3-D (black boxed line) and 2-D (blue boxed line) nets when having the same dimensions.

C. Impact of TSV Pitch

We perform the same single-net experiment, changing the pitch between TSVs from 10 to 50 μm. In Fig. 14(a), we see that changing TSV pitch does not impact much on reducing the delay of the victim receiver (−7.9% reduction in 1× driver). However, this is different when a 2-D net is distanced from an aggressor. To compare the impact of delay reduction in 2-D and 3-D due to neighbor pitch change, we perform an experiment, where a 2-D wire has the same dimension as a TSV, in which the permitivity of the dielectric is the same as the silicon substrate. Fig. 14(b) shows our 3-D versus 2-D delay comparison. We use both 1× driver sizes in both the experiments. In this experiment, we will define TSV delay as 3-D delay, and 2-D wire delay that has the same dimensions as the TSV as 2-D delay, respectively. Here, we report two important findings. First, at the same pitch, 3-D delay is always higher than 2-D delay. In 10-μm neighbor pitch, the 3-D delay is ∼2× of 2-D delay (242 ps > 110 ps), and this difference increases as the pitch increase. In 50-μm pitch, this delay difference is >4× (225 ps > 54 ps). Second, unlike in 2-D delay, 3-D delay does not significantly reduce from increasing the pitch. When the neighbor pitch increases from 10 to 50 μm, 3-D delay reduces by only 7.9%, but 2-D delay reduces >50%. This means that 3-D delay is not sensitive to neighbor TSVs, unlike in 2-D delay. Note that we see a trend similar to this in various 2-D wire and 3-D TSV sizes: 3-D delay is always bigger than 2-D delay in the same size and less sensitive to distance change. We discuss the reason of this in Section VI-D3.

D. Impedance Load Analysis for Delay Estimation

Calculating the *RC* delay is a good approach when we estimate the delay of a net in normal 2-D systems [15]. When calculating the delay, a net is composed of the resistance of the path and various capacitive loads. These loads are the capacitance load of the receiver, capacitance formed to the GND, and coupling capacitance between the paths, as shown in Fig. 15(a). When excluding the resistance for the path, we can think of these capacitive loads as the total load that a driver sees in a net, as shown in (12), for delay estimation

$$\text{Load}_{\text{Driver}} = C_{\text{receiver}} + C_{\text{GND}} + C_{\text{coup}}. \quad (12)$$

The capacitive load concept is applicable in normal load conditions, where the coupling neighbors are perfectly isolated

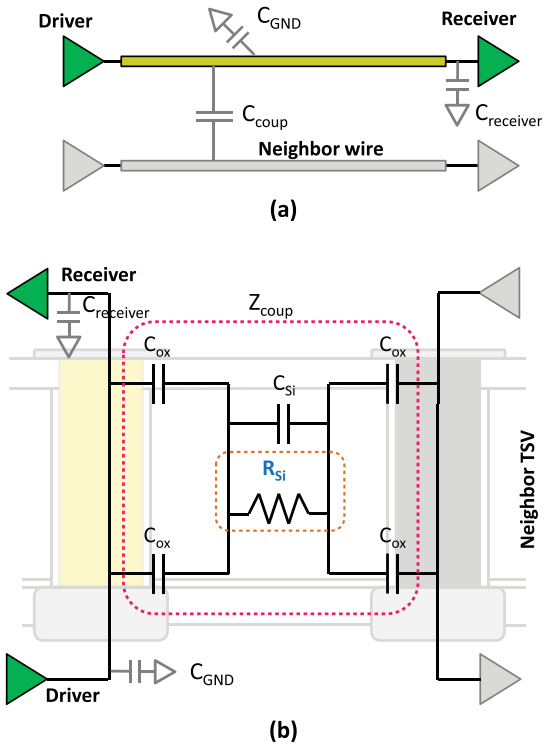

Fig. 15. All loads (GND, receiver, and coupling) in (a) 2-D net and (b) 3-D TSV net.

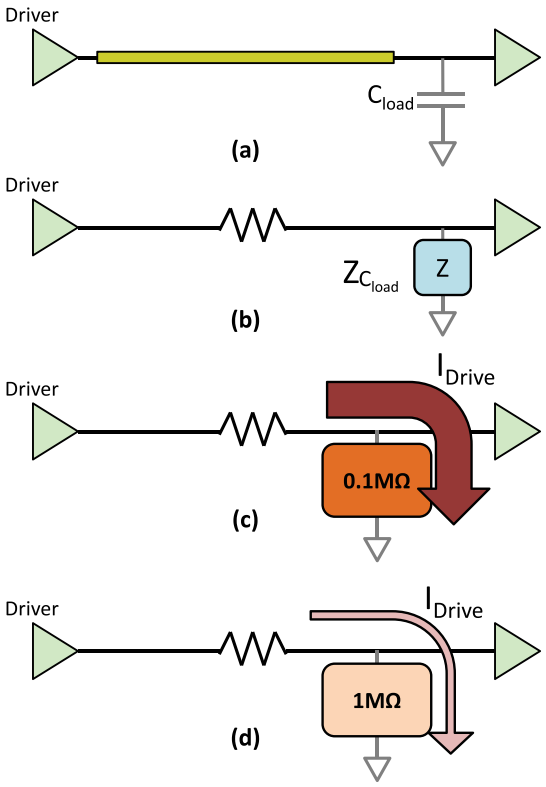

Fig. 16. Impedance load concept. (a) Capacitive load translates into (b) impedance load. (c) Low-impedance load suffers from more delay than (d) high-impedance load.

by a dielectric that its conductivity is almost negligible. However, this cannot be applied to a 3-D net with TSVs. In a 3-D net, a silicon substrate lies between the neighbor TSVs that its conductivity is nonnegligible. Because of this, the silicon substrate introduces an impedance path that is modeled as a resistance [R_{si}, see Fig. 15(b)]. Therefore, we propose a method for analyzing the delay of a 3-D path called the impedance load.

Using the impedance load, (12) changes to

$$Z_{\text{Load}_{\text{Driver1}}} = Z_{\text{receiver}} + Z_{\text{GND}} + Z_{\text{coup}} \tag{13}$$

where all the capacitance loads transform into the impedance loads. When the loads are expressed as capacitances, we cannot analyze the impact of R_{si}, but now, we can analyze using the impedance load analysis method.

1) Understanding the Impedance Load for Less Delay: We describe a 2-D net example in Fig. 16 to understand how the impedance load concept is used. As shown in Fig. 16(a), we see that the driver sees a load of C_{load}. In the impedance load analysis, this capacitive load becomes an impedance load $\text{Z}_{\text{C}_{\text{load}}}$ ($Z = 1/sC$), as shown in Fig. 16(b). For example, at 1 GHz, the following holds.

1) $\text{C}_{\text{load1}} = 1/2\pi$ fF becomes $\text{Z}_{\text{C}_{\text{load1}}} = 1\text{M}\Omega$.
2) $\text{C}_{\text{load2}} = 10/2\pi$ fF becomes $\text{Z}_{\text{C}_{\text{load2}}} = 0.1\text{M}\Omega$.

Under the impedance load analysis, a $10\times$ bigger capacitance load ($\text{C}_{\text{load2}} = 10 \times \text{C}_{\text{load1}}$) becomes a $0.1\times$ smaller impedance load ($\text{Z}_{\text{C}_{\text{load2}}} = 0.1 \times \text{Z}_{\text{C}_{\text{load1}}}$) in magnitude. To translate this into a physical meaning, we note that a smaller Z_{load} derives more delay. In the perspective of a driver, the voltage swing is a function of the current driving and the load that a driver sees ($\Delta V = \Delta I Z$). This means that it requires more current to drive (=change the voltage) a smaller impedance (= higher capacitance) load than a higher impedance (= less capacitance) load. However, since a driver has a limited amount of current driving capability (ΔI), it will take more time to drive a small impedance load than a high impedance load, at which small impedance load suffers from more delay.

2) Impedance Load Analysis of a Timing Path: Using the impedance load, we derive the equations for 2-D and 3-D coupling loads. As shown in (12), a coupling load C_{coup} now becomes Z_{coup}. For a 2-D wire, since $Z_{\text{2-D,coup}}$ is simply the coupling capacitance between two wires isolated through a dielectric, this can be expressed as

$$Z_{\text{2-D,coup}} = Z_{\text{C}_{\text{wire-to-wire}}}. \tag{14}$$

However, for a 3-D TSV, $Z_{\text{3-D,coup}}$ becomes a complicated network considering the liner capacitance, substrate capacitance, and substrate resistance, as shown in Fig. 15(b)

$$Z_{\text{3-D,coup}} = Z_{C_{\text{ox}}} + (Z_{R_{\text{si}}} // Z_{C_{\text{si}}}) + Z_{C_{\text{ox}}} \tag{15}$$

$$Z_{\text{3-D,coup}} = \frac{2Z_{C_{\text{ox}}}\left(Z_{R_{\text{si}}} + Z_{C_{\text{si}}}\right) + Z_{R_{\text{si}}} Z_{C_{\text{si}}}}{Z_{R_{\text{si}}} + Z_{C_{\text{si}}}}. \tag{16}$$

Using Agilent ADS, we compare $Z_{\text{3-D,coup}}$ and $Z_{\text{2-D,coup}}$ when the pitch is 10 μm (when the 2-D wire and the 3-D TSV have the same dimensions), as shown in Fig. 17. Red line denotes $Z_{\text{2-D}}$, and blue line denotes $Z_{\text{3-D}}$. We see that $Z_{\text{2-D}}$ is a linear curve, since we only see the capacitive load.

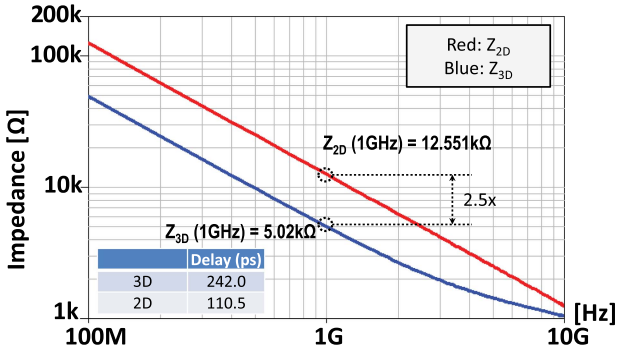

Fig. 17. Coupling load impedance $Z_{2\text{-}D}$ and $Z_{3\text{-}D}$ when TSV pitch is 10 μm.

However, $Z_{3\text{-}D}$ shows a nonlinear curve in the GHz region because of the conductive silicon substrate (R_{si}). R_{si} combined with C_{si} and C_{ox} forms a coupling network impacting in the GHz region. From Fig. 17, we report the following.

1) $Z_{3\text{-}D,coup}$ is always lower than $Z_{2\text{-}D,coup}$ in all the frequency regions. This means that the 3-D timing path will suffer from more delay than in the 2-D path.
2) The impedance ratio between $Z_{3\text{-}D,coup}$ and $Z_{2\text{-}D,coup}$ roughly leads to the delay ratio between 2-D and 3-D.

Note that the ratio between $Z_{2\text{-}D}$ and $Z_{3\text{-}D}$ is almost the same in a broad range of frequencies. At 1 GHz, $Z_{3\text{-}D,coup} = 5.02$ KΩ and $Z_{2-D,coup} = 12.5$ KΩ, and $\text{Delay}_{3\text{-}D} = 242.0$ ps and $\text{Delay}_{2\text{-}D} = 110.5$ ps. Within this broad spectrum, $Z_{2-D,coup}$ is 2.5× more than $Z_{3\text{-}D,coup}$, and this impedance difference roughly translates into the inverse of delay ratio.

3) Why 3-D Delay Is Not Sensitive to Neighbor Distance: We explain why 3-D delay is not sensitive to neighbor TSV distance by analyzing the impedance curve. Fig. 18(a) shows how $Z_{2\text{-}D,coup}$ changes when the pitch of a 2-D wire changes. We see that the impedance curve of 2-D increases monotonically as the pitch increases. Thus, as the pitch increases, higher $Z_{2\text{-}D}$ leads to less timing delay. As the TSV pitch increases, the coupling capacitance reduces. Lower coupling capacitance leads to less delay, which has the same meaning as the impedance analysis.

However, $Z_{3\text{-}D,coup}$ due to the pitch increase [see Fig. 18(b)] is not as in 2-D. The $Z_{3\text{-}D,coup}$ curve only changes on the high-frequency region and remains almost the same below 1 GHz. That is why 3-D delay is not highly impacted by the increase in the TSV pitch. In the equivalent model of TSVs in Fig. 15(b), we see that the TSV pitch increase only changes the values of $Z_{R_{si}}$ and $Z_{C_{si}}$. Since a high-capacitance C_{ox} exists in the impedance path of $Z_{3\text{-}D,coup}$ as in (16), the actual factor increases $Z_{C_{ox}}$ and not $Z_{C_{si}}$. We see that $Z_{C_{si}}$ and $Z_{R_{si}}$ change impacts on the high-frequency $Z_{3\text{-}D}$, but this impact is not significant to reducing much delay.

E. Full-Chip Impact on Timing and Power

As described in Section V, we vary the TSV parameters on the design performed in Section IV to gain the understanding of how TSV impacts the full-chip delay and powers when using an accurate TSV model. Table IV shows our full-chip timing/power analysis results. From our full-chip results, we emphasize the following important points.

1) As the TSV height increases, SiO_2 liner thickness decreases, and TSV radius increases, we see more LPD and TNS. This is because, as these parameters increase/decrease, the total capacitance increases and leads to more timing delay.

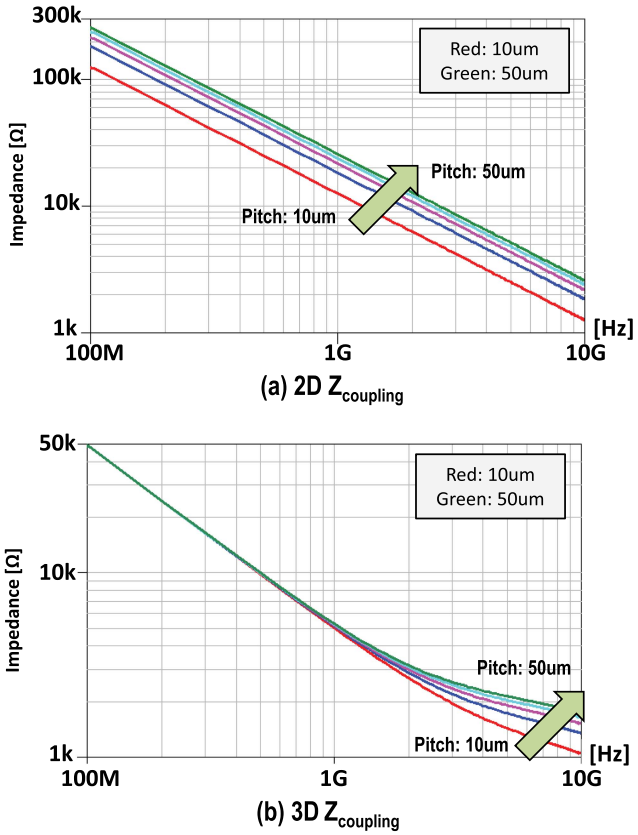

Fig. 18. Z_{coup} change when TSV pitch changes from 10 to 50 μm. (a) 2-D. (b) 3-D.

TABLE IV
FULL-CHIP TIMING REPORT: IMPACT OF TSV PARAMETERS

TSV height	20μm	40μm	60μm	80μm	100μm
LPD (ns)	2.761	2.788	2.816	2.844	2.871
TNS (ns)	-64.44	-67.32	-70.23	-73.29	-76.41
3D net power (mW)	1.72	1.75	1.78	1.81	1.83
Power increase	-	1.7%	3.4%	5.2%	6.3%
Liner thickness	0.1μm	0.2μm	0.3μm	0.4μm	0.5μm
LPD (ns)	2.832	2.827	2.823	2.819	2.816
TNS (ns)	-72.45	-71.73	-71.14	-70.65	-70.23
3D net power (mW)	1.80	1.79	1.79	1.78	1.78
Power increase	-	-0.6%	-0.6%	-1.2%	-1.2%
TSV radius	2μm	4μm	6μm	8μm	10μm
LPD (ns)	2.816	2.868	3.4	5.88	8.36
TNS (ns)	-70.23	-76.42	-107.9	-300.1	-492.3
3D net power (mW)	1.78	1.84	2.04	2.59	3.14
Power increase	-	3.3%	14.6%	45.5%	76.4%

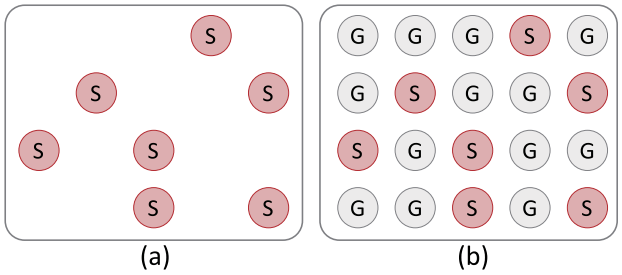

Fig. 19. TSV path blocking in a layout. (a) Before TSV path blocking. (b) After TSV path blocking.

2) Within the range of parameter change, the TSV radius increase leads to the worst results in increasing the LPD and TNS. This is a similar trend to what we observed in Section V.
3) The power increase of 3-D nets due to the TSV parameter change shows a similar trend to the LPD and TNS increase trends. Since the power consumption of each net is directly proportional to the capacitance increase, this is reasonable. Note that the total 3-D net power increases 74% when the TSV radius changes from 2 to 10 μm. Due to the TSV radius increase, not only does the TSV capacitance increases, but also the number of effective aggressors to a victim increases as well.

VII. TSV-to-TSV Coupling Reduction

Based on our findings, we propose a TSV-to-TSV coupling reduction method in a block-level and wide-I/O design.

A. TSV Path Blocking

For a layout that has an aggressor and a victim, both the capacitance of the aggressor and the additional TSV decrease when an additional TSV is included in the design (Section II-B). Thus, when a space between an aggressor and a victim exists, we add GND TSVs. We name our coupling reduction method TSV path blocking. By adding the GND TSVs, we block the E-field path between the aggressor and the victim, and thus, we reduce the coupling capacitance. Fig. 19 shows how this is applied in the layout. We may think that adding more TSVs will increase the total capacitance significantly. However, in a layout, a TSV is surrounded by many neighbors that the total coupling capacitance will saturate in a range around 2× (when $C_{\text{one victim}-\text{one aggressor}} = 1\times$). Thus, adding the GND TSVs near the neighbor does not have a big impact on increasing the total coupling capacitance (Section II-A) of a victim. The benefits of our method are as follows. First, it recycles any empty design space in the layout, so that it does not require extra silicon space just for shielding. Second, the neighbor TSV does not need to be in between the aggressor and the victim for coupling reduction. For example, let us assume one of the aggressors is a GND neighbor TSV, as shown in Fig. 1(b). Comparing Fig. 1(a) and (b), notice that the capacitance between a victim and an aggressor reduces by 23.5% (0.765× capacitance each), because two neighbor TSVs share the E-field around the victim. Last, selective coupling reduction is possible. If a victim needs more coupling reduction than other, placing more neighbor TSVs nearby helps.

TABLE V
Impact of TSV Path Blocking—Block Level Design

	W/O Path Blocking	W/ Path Blocking
Footprint (μm)	970 × 823	970 × 823
Total coupling noise (V)	787.42	726.04
Longest path delay (ns)	2.852	2.811
Total negative slack (ns)	-75.24	-79.62
3D coupling noise (V)	196.65	135.27

TABLE VI
Impact of TSV Path Blocking—Wide I/O Design

	Original array	Spread array	W/ Path Blocking
Area by TSV (μm)	160 × 140	320 × 140	320 × 140
Total coupling noise	824.26 V	797.9 V	742.37 V
Longest path delay	2.907 ns	2.963 ns	2.925 ns
Total negative slack	-77.26 ns	-74.51 ns	-82.04 ns
3D coupling noise	193.99 V	157.41 V	105.81 V

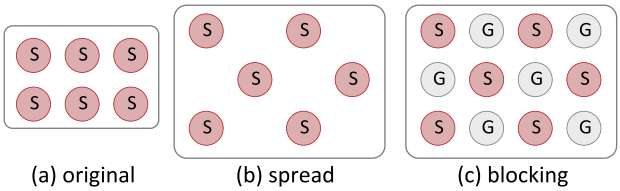

Fig. 20. (a) Initial wide-I/O design. (b) Wide I/O design with spread TSVs. (c) Wide-I/O design with TSV path blocking.

Table V shows our results. By adding TSVs inside the empty space, the total coupling noise reduces from 787 to 726 V. Considering only the 3-D noise, we reduce the 3-D coupling noise by 32% from 196 to 135 V. We report that the TSV path blocking has a minor impact on timing. When the GND TSVs are added, the total capacitance will slightly increase, since more TSVs are placed near the victim. By the increased capacitive load, the TNS increases, but the impact is minor, since the total capacitance has a maximum limit, and it is shared by the aggressor and the GND TSVs. We conclude that the TSV path blocking is an effective way for reducing TSV-to-TSV coupling that has a minor impact on timing performance.

B. Optimization for Wide-I/O Design

We designed three wide-I/O layouts: 1) Fig. 20(a) is our initial wide-I/O design (original); 2) Fig. 20(b) is the wide-I/O design with an increased area (spread); and 3) Fig. 20(c) is the wide-I/O design with our technique applied (blocking). Fig. 21 shows an actual layout applying our technique. For a fair comparison, we did not modify the placement of the modules, but we only increased the area used by TSVs. If the total die size changes due to the increased TSV area, the whole design will change. Thus, the die size is the same for all the cases.

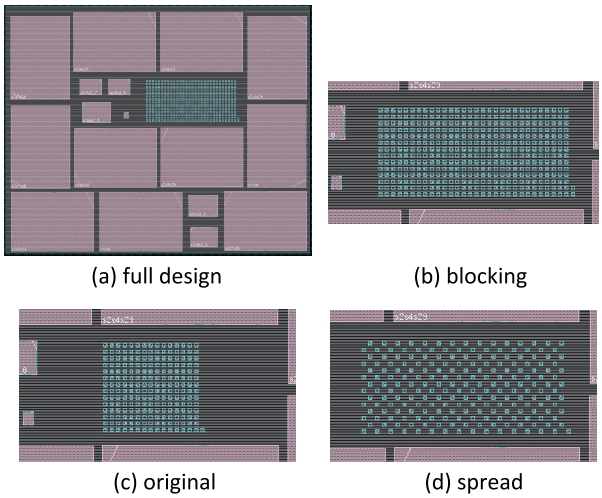

Fig. 21. (a) TSV path blocking in wide-I/O layout. (b) Zoom-in photo of (a). (c) Initial wide-I/O design. (d) Wide I/O with spread TSVs.

Table VI describes the impact of TSV blocking in wide I/O design. By our technique, we see that the TSV-occupied area doubles, but the total coupling noise reduces from 824 to 742 V. Considering only the 3-D noise, we reduce the 3-D coupling noise by 45% from 193 to 105 V. Note that just by spreading the wide I/O array, as shown in Fig. 21(d), the total coupling noise reduces too. However, if we include the GND TSVs, as shown in Fig. 21(b), we observe more TSV coupling reduction. The 45% reduced 3-D coupling noise would reduce the burden to the designers that requires putting significant effort to reduce the 3-D coupling noise using circuit techniques, e.g., wide-IO designs that consist of a complex coding scheme [16] with extra circuitry may not be needed at all due to the significant noise reduction from our technique. Wide I/O with spread TSVs shows less TNS, because the capacitance that a victim sees reduces due to the increased distance.

VIII. Conclusion

In this paper, we presented a thorough analysis of the TSV impact on full-chip SI. First, we showed that nonneighboring aggressors cause significant impact in 3-D ICs, which we call the neighbor effect. We developed a compact multiple TSV-to-TSV coupling model and an algorithm that accurately consider the impact of far-neighbors on a full-chip 3-D SI analysis. Second, we reported the TSV impact on 3-D net delay. We showed that 3-D net delay is not highly affected by the neighbor TSV distance based on our impedance load analysis method. To reduce the TSV-to-TSV coupling noise, we proposed a technique: TSV path blocking on a block-level and wide-I/O design. The experimental results show that, by the TSV path blocking, we achieve 45% 3-D coupling noise reduction.

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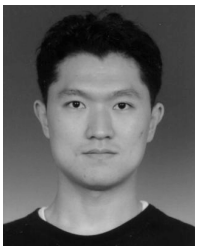
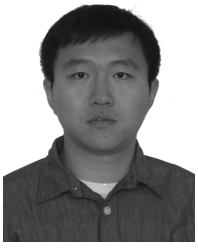


Taigon Song (S'09) received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 2007, and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2009. He is currently pursuing the Ph.D. degree with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA.

His current research interests include 2.5-D/3-D IC design and analysis.



Chang Liu received the B.S. and M.S. degrees in microelectronics from Peking University, Beijing, China, in 2006 and 2009, respectively, and the M.S. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2011.

He has been with Broadcom Corporation, Irvine, CA, USA, since 2012, where he is involved in multi-Gbps wireline transceivers for optical and backplane/cable applications.

Yarui Peng (S'12) received the B.S. degree from Tsinghua University, Beijing, China, in 2012, and the M.S. degree from the Georgia Institute of Technology, Atlanta, GA, USA, in 2014, where he is currently pursuing the Ph.D. degree with the School of Electrical and Computer Engineering.

His current research interests include physical design and analysis for 3-D ICs, including parasitic extraction and optimization for signal integrity, thermal, and power delivery issues.

Mr. Peng was a recipient of the Best in Session Award in SRCTECHCON in 2014.

Sung Kyu Lim (S'94–M'00–SM'05) received the B.S., M.S., and Ph.D. degrees from the Computer Science Department, University of California at Los Angeles (UCLA), Los Angeles, CA, USA, in 1994, 1997, and 2000, respectively.

He was a Post-Doctoral Scholar with UCLA, and a Senior Engineer with Aplus Design Technologies, Inc., Los Angeles, from 2000 to 2001. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, in 2001, where he is currently an Associate Professor. He has authored the book entitled *Practical Problems in VLSI Physical Design Automation* (Springer, 2008). His current research interests include the physical design automation for 3-D ICs, 3-D system-in-packages, microarchitectural physical planning, and field-programmable analog arrays.

Dr. Lim received the Design Automation Conference Graduate Scholarship in 2003, and the National Science Foundation Faculty Early Career Development Award in 2006. He was on the Advisory Board of the ACM Special Interest Group on Design Automation (SIGDA) from 2003 to 2008, and received the ACM SIGDA Distinguished Service Award in 2008. He is an Associate Editor of the IEEE TRANSACTIONS ON VLSI SYSTEMS and served as a Guest Editor of the *ACM Transactions on Design Automation of Electronic Systems*. He has served on the technical program committee of several ACM and IEEE conferences in electronic design automation.