Stacking Integration Methodologies in 3D IC for 3D Ultrasound Image Processing Application: A Stochastic Flash ADC Design Case Study

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***Abstract*—In three-dimensional integrated circuit (3D IC) systems that use through-silicon via (TSV) technology, a significant design consideration is the coupling noise to/from TSVs. In Analog/Mixed signal ICs, the TSV coupling effect can cause coupling noise disturbance and degrades the performance of sensitive analog devices. In this paper, two different stacking integrations for the sensor array and the 3D IC, are considered and compared. In the face-up stacking integration, the transducers' flip chip bonded pads are directly bonded to the integrated circuit. In face-down integration type, however, the connections from the sensor output signal to the front end electronics is done via the TSVs. The TSV coupling noise is compared for the two schemes using the existing TSV coupling noise model. To validate the impact of stacking integration on the coupling noise, an ADC case study was designed and implemented using 130nm device technology and Tezzaron TSV technology. The simulations results show that the face-up integration could suppress the coupling noise by $10db$. Moreover, a 23% reduction in footprint is achieved in this stacking integration.**

I. Introduction

Three-dimensional integrated Circuit (3d IC) technology has emerged providing advantages such as miniaturized footprint and lower power consumption owing to shorter interconnects [1]. Recently, many 3D CMOS imagers [2]–[4] have been presented. An imager system in general contains, transducer arrays which are combined with the integrated circuit containing the ADC, and signal processing. On the other hand, 3D ultrasound imagers have been demonstrated where the 2D ultrasound transducer is flip-chip bonded to the integrated circuit making a face-to-back bonding integration [5]. Combining the flip chip bonding integration of Ultrasound transducer and 3D IC, allows for better utilization of large arrays and improves receive sensitivity. As shown in Fig. 1.a, several circuit layers from the transducer element to analog front end, ADC and signal processing are stacked into one chip in 3D structure.

Recently, many digital 3D IC designs have been conducted, mostly by stacking memory or logic onto several layers. However, very little has been done for 3D analog or mixed-signal design [6]. Despite the great benefits of the 3D technology for the mixed signal circuits, there are challenges need to be overcome. Significantly on the mixed signal design, the effect of TSVs should be carefully evaluated as large noises, such as ground bounce noise and substrate noises are coupled through the TSV. There are several works on analyzing the TSV-induced noise impacts on 3D ICs [7]. The TSV-to-TSV TSV-to-active coupling effects in device or full-chip level have been studied. Substrate noise coupling is studied in [8], where the substrate noise comes from the digital circuit and propagated within the substrate is studied. In digital ICs, cross-talk induces some logic errors and timing violations which causes more power dissipation; however in mixed signal ICs, the TSV coupling effect degrades the performance of sensitive analog devices. Especially, in the ultrasound applications, where a very high dynamic range is required, the analog front end circuitry, plays a critical role in deciding the whole system SNR. As a result, the coupling noise suppression in the front end electronics becomes a critical design issue in TSV 3D integrations.

In this paper, two different stacking integrations are considered, and the coupling noises coupled to/from TSVs and silicon substrates under different 3D structures are compared. Fig. 1.b shows the configuration of block parallel ultrasound imaging system with 3-D stacked structure. The system consists of layers of the ultrasound transducer, analog front end circuit containing ADC and processing element array, where the layers are connected vertically via TSVs. Fig. 1.b compares two different stacking integrations of the two most front-end layers of the transducer arrays and the analog front end IC tier. In face-up stacking, the transducer's flip chip bonded pad is directly connected to the faced-up 3d IC electronics making a face-to-back connection. In the face-down, however, the connection between the faced-down 3d IC electronics and the ultrasound layers is carried out via the TSV, making a back-back connection between the layers. The connection types, therefore, affects the coupling behavior of the two different integration types.

In this work, a stochastic flash ADC is designed as a case study for 3D mixed-signal circuitry. The stochastic flash ADC is suitable for applications with reconfigurable, high speed/moderate resolution. The stochastic flash ADC was first proposed in [9], and a fully digitally synthesized ADC is proposed in [10].

The rest of this paper is organized as follows. Section II comprises TSV noise coupling model used for the coupling analysis. The main coupling paths in different stacking integrations are presented and compared. In section III the stochastic flash ADC case study is presented and the implementation in two different stacking integrations are compared. Conclusion is drawn in Section IV.

II. Modeling of TSV Induced Coupling Noise

A. Noise Coupling between the TSVs, and TSV and substrate

Fig. 2 illustrates two major paths of TSV noise coupling in a 3D IC that employs TSV technology: noise coupling between two TSVs, and noise coupling between a TSV and active circuit.

A TSV is a highly conductive metal that is surrounded by an insulation layer, such as $SiO2$ to isolate the DC leakage TSV and the highly conductive silicon substrate. This results in a high capacitance between the TSV and the silicon substrate which is referred to C_{TSV}. Therefore, high-frequency noise can be easily coupled from

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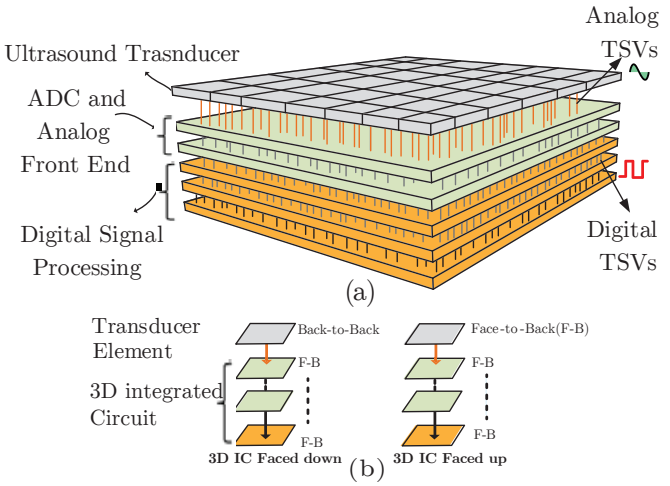

Fig. 1. a. Conceptual diagram of the 3D stacked system b. Diagram of different front end stacking integrations

TSV to TSV or from TSV to substrate and vice-versa, via substrate transmission path. The following equations which are the traditional TSV models [11] are used to extract the TSVs Oxide capacitance and resistance respectively:

$$C_{TSV} = \frac{1}{4}\frac{\pi\epsilon_0\epsilon_r L_{TSV}}{ln\frac{R_{TSV}+T_{ox}}{R_{TSV}}}, \quad R_{TSV} = \frac{L_{TSV}}{\sigma\pi R_{RSV}^2} \tag{1}$$

in which ϵ_r, L_{TSV}, and R_{TSV} are the permittivity of the silicon substrate, the height and radius of TSVs respectively, T_{ox} is the thickness of the insulator.

The TSV-to-TSV coupling is mainly through the SiO2 capacitor, and the silicon substrate which is RC parallel network, as illustrated in Fig. 2. By dividing the substrate into several cubes as proposed in [7], the parameters of substrate parameters is calculated by :

$$C_{sub} = \epsilon_{si}\frac{h_{sub}\times l_{sub}}{w_{sub}}, \quad R_{sub} = \frac{1}{\rho}\frac{w_{sub}}{h_{sub}\times l_{sub}} \tag{2}$$

where w_{sub}, l_{sub} and h_{sub} represent the width, length and height of the substrate unit.

For the TSV-to-Active coupling, the TSV high frequency noise is coupled to the SiO2 capacitor and silicon substrate parasitic network. As the CMOS devices is divided mainly into gate metals, substrate contacts, coupling between TSV and the substrate contact is dominant due to the direct connection through the bulk silicon. The substrate noise form the bulk is then coupled to the CMOS gate via the C_{gb}.

B. Noise Coupling path for face-up versus face-down stacking integration

The noise behavioral of the two 3D stacking integrations based on Fig. 1.b is studied. In Fig. 3.a, a the back-to-back (3D IC faced down) integration of the ultrasound array and the analog front-end is shown. An analog ultrasound signal first is delivered to the top tier via a TSV. Meanwhile, a semi-digital output signal from the top tier is fed to the bottom tier via the TSVs. The major coupling path from digital circuit to the ultrasound input is shown. The active-to-TSV coupling from the digital noise source coupled via the substrate RC path to the input analog signal. The small circuit equivalent of the ultrasound CMUT is used as the ultrasound signal source.

Fig. 3.b depicts a back-to-face(3D IC faced up) ultrasound integration, in which the ultrasound signal is directly connected to the electronics via the metal stack. The TSV-to-active coupling from the

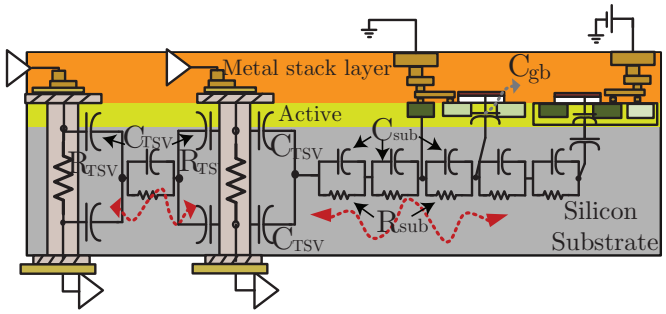

Fig. 2. Coupling effect between TSVs and the TSV and active area

digital TSV coupled via the substrate RC path to the input analog signal is depicted. The substrate noise is directly coupled to the gate substrate contact. The coupling to the CMOS gate metal, however is attenuated via the C_{gb} capacitance which is much smaller than the C_{TSV}. As a result, less coupling noise is expected for the face-up than the dace-down dies stacking. This is explained more in the next sub-section.

TSVs, are attached to landing pads in the bottommost and the topmost metal layers. The TSV landing pad for each different stacking integrations is different for each top and bottom die. This will be discussed more in the next section.

C. Coupling effect analysis

By the high-frequency noise transmission path between the TSV and the grounded substrate, the digital signal can have coupling effect on the sensitive analog device. To demonstrate the TSV coupling noise effect on the ultrasound signal, a single comparator block was implemented, where the kickback noise via the TSV coupling transmission path was investigated. In face-up die integration, the digital TSV coupling effect on the comparator input signal is dominated. In the face-down integration, however, the digital signal coupled to the analog TSV via the conductive substrate is dominated. Fig. 4 shows the post layout spice simulation, where the comparator kickback noise power due to the TSV coupling for different stacking integrations over different TSV parasitic capacitance is shown. As demonstrated, the TSV coupling effect for the face-down die stacking is much worse than the face-up die stacking. This is because the substrate noise in face-down is directly coupled to the input analog TSV. In the face-down die stacking, however, the substrate noise is attenuated by the gate-body capacitance which alleviates the coupling effect.

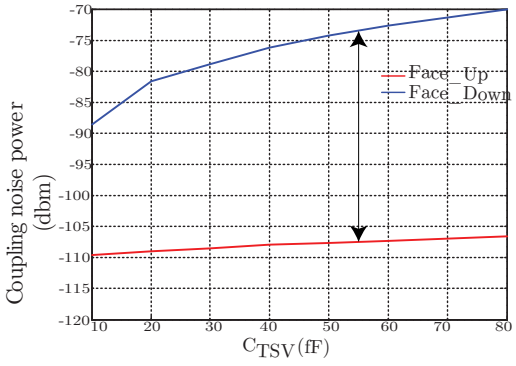

Fig. 4. Spice Simulation result for comparator kickback noise due to the TSV coupling for face-up versus face-down die stacking

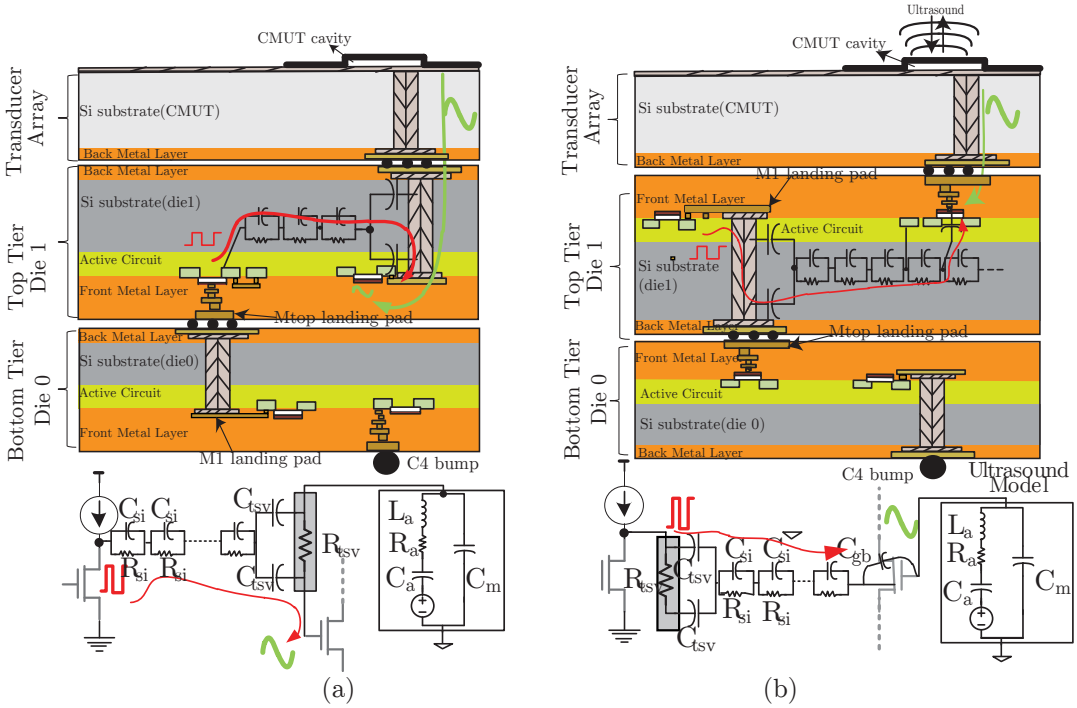

Fig. 3. figure showing noise coupling path in (a) face-down integration, between the high-frequency digital signals and the analog signal TSV (b) face-up integration, between the digital TSVs to analog input signal

III. Case Study

A. Stochastic flash ADC

In this work a stochastic Flash ADC with a 1024-comparators version implemented as case study. Fig. 5.a shows a schematic of a stochastic flash ADC. By employing many redundant identical comparators, this technique exploits the large random variation in the comparator offset in such a way that the number of comparators evaluating high follows a cumulative density function of a Gaussian comparator offset.

The ADC consists of two main building blocks, the comparator bank and a one's counter adder implemented by a pipeline wallace-tree adder. The adder is to count the number of comparators evaluating high. In this work, in order to take advantage of the 3D integration, we redesign the ADC by partitioning it into two stacked dies as shown in Fig. 5.b . The 3D stochastic ADC core netlist is partitioned in two dies mainly by considering separating the analog and the digital part. The analog part is basically the standard cell based comparator bank, and the digital part consists of the standard cell based full adders bank. This indeed separates substrate for the digital block and the analog front-end. Since the total gate area for the comparator and the adder is approximately the same, this partitioning type also proves to be efficient in terms of area balance between dies and connectivity between them.

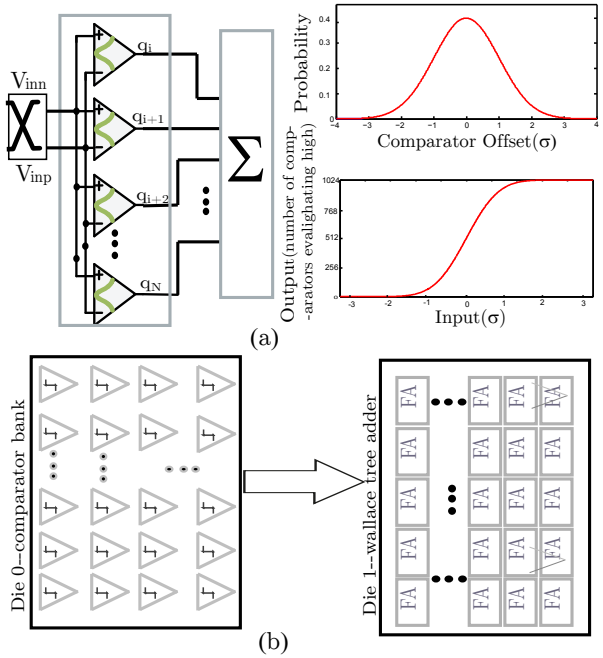

Fig. 5. a. block diagram of the stochastic flash ADC b. 3d partitioned flash ADC block diagram

B. Coupling results and discussion

The TSV technology in this design is from Tezzaron, with TSV size of 4um x 4um, parasitic resistance and capacitance of $10m\Omega$, $50fF$ respectively. Fig. 6 presents the vertical stacking diagram of 3D ADC and the CMUT array for the face-up and face-down dies stacking. The total TSVs are divided in three main groups: the I/O TSVs in face-up, which connect the ADC output signals to the C4 bumps, the intra-die TSVs which make the connection between two stacked dies, and the analog TSV in face-down which feeds the analog signal to the top die. The TSV landing pad for each different stacking integrations is different for each top and bottom die as shown in Fig. 6. This makes the footprint less efficient in one of the 3D integration types, especially if there is area imbalance between different dies. The 3D ADC layout design for two different integration is also depicted based on two stacked dies: comparator front-end top die and digital adder bottom-die. The design is implemented in GLOBALFOUNDRIES 0.13um six-metal standard CMOS process. For the TSVs insertion,

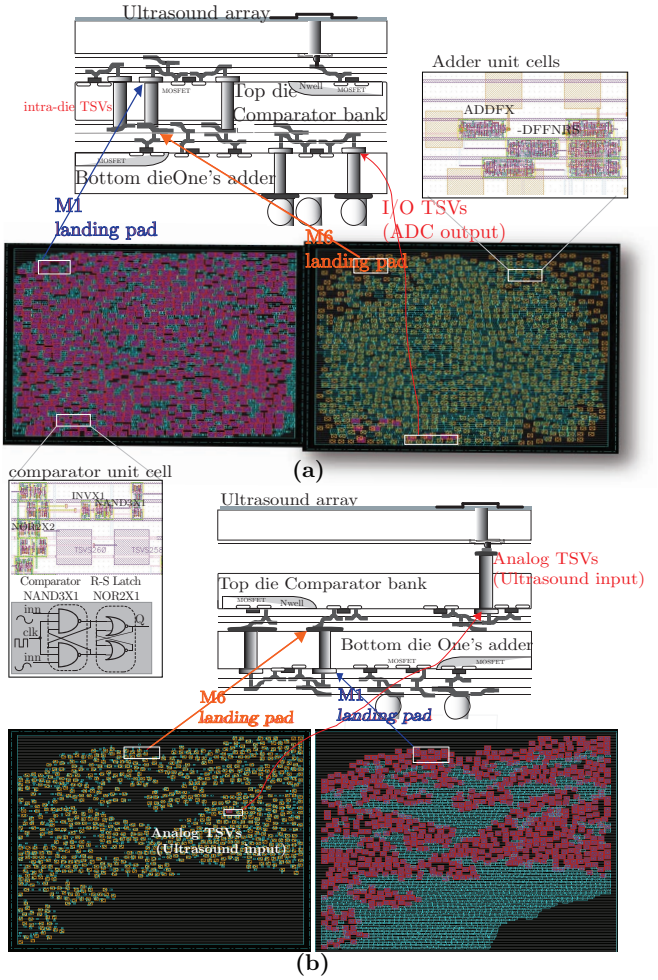

Fig. 6. Layout of the 3D stochastic ADC (a) face-up (b) face-down dies stacking integration

TABLE I
3D STOCHASTIC ADC VS. 2D PERFORMANCE COMPARISON

	3D-IC-face-up	3D-IC-face-down	2D
Power dissipation(mW)	8.1	8.1	10.2
TSV coupling Noise power(nw)	0.25	2.2	–
Footprint (mm^2)	0.13	0.17	0.21
Total TSVs count	1034	1025	–

the TSVs are treated as logic cells, an in-house 3D placer [12] is used to obtain the TSV placement and Cadence Encounter to obtain a fine placement and to route the design. As shown in Fig. 6, the face-down stacking demonstrates more empty space than the face-up stacking. Moreover, by using the standard cell as the comparator unit cell, the ADC was fully synthesized. Fig. 6 depicts the zoom shot, showing the unit cells used in the ADC design. The 2D and 3D design metrics for the face-up and face-down dies ADCs for 100MHz clock frequency are compared in Table I. By using the three dimensional integration a power reduction and footprint shrinkage was observed compared to the traditional 2D design.

IV. CONCLUSION

Coupling noise to/from TSVs reduction is a significant design challenge in the-dimensional Analog/Mixed-signal systems that use through-silicon via (TSV) technology. Two different 3D stacking integrations proposed, where the flip chip bonded transducer arrays are directly connected to the custom design integrated circuit in the first configuration, whereas the connection to the front end electronics is done via the TSVs in the second stacking integrations. The TSV coupling noise is compared for the two schemes using the existing TSV coupling noise model. A stochastic flash ADC case study was designed and implemented using 130nm device technology and Tezzaron TSV technology, to validate the impact of stacking integration on the coupling noise. The experimental results show that the face-up integration suppressed the coupling noise by $10db$. Moreover, a 23% reduction in footprint is achieved in this stacking integration.

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