Coupling Capacitance in Face-to-Face (F2F) Bonded 3D ICs: Trends and Implications

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Abstract

Face-to-face (F2F) is a bonding style in three-dimensional integrated circuits (3D ICs) that bonds ICs by using the top-metal (face) as the bonding side when stacking two ICs. As technology scales in F2F bonding, the distance between the ICs becomes as small as few microns. Due to this shorter distance, significant coupling occurs between these ICs. In this paper, we investigate the impact of coupling capacitance when ICs are bonded in a F2F manner. Using a field-solver-based modeling methodology, we examine three critical areas related to F2F parasitics: (1) physical and process factors that impact F2F coupling capacitance, (2) capacitance error when inter-die interactions are not considered, and (3) the impact of micro-bumps on F2F capacitance. The results indicate that F2F separation distances smaller than 10 microns will lead to significant inter-die capacitive interactions that must be considered when extracting F2F bonded 3D ICs.

I. Introduction

Three-dimensional integrated circuits (3D ICs) have gained significant attention over the past decade as a technology that can facilitate the continuation of the advances guided by the Moore's law. 3D ICs can provide significant power and performance benefits by stacking dies vertically [1]. Many studies have demonstrated the advantage of 3D ICs over conventional 2D ICs, and several companies have recently announced their plans to mass-produce commercial products based on 3D technology starting from 3D DRAMs [2]. Through-silicon vias (TSV) are one common approach for manufacturing 3D ICs. By drilling a hole inside the substrate and filling it with metal, vertical interconnections are implemented. Leveraging these vertical interconnections, shorter interconnects can be implemented, thereby leading to better performance with low power.

In addition to the TSV-based 3D IC, face-to-face (F2F) is a bonding style that also makes 3D IC possible. For 3D ICs that use TSVs, ICs are bonded by using the back side (the side where TSV is exposed) of one die and the face side (the side where top-metal is exposed) of another die. However, in F2F, the ICs are bonded by using both face sides as the bonding side using F2F bumps. Several studies indicated that F2F 3D ICs provide advantages over TSV-based 3D ICs in many applications since they do not use any silicon area [3].

Driven by the fact that scaled 3D interconnects (TSV and F2F bumps) provide denser I/Os, many studies have demonstrated how these interconnects are becoming smaller. To provide denser I/Os for F2F bonding, two technologies must scale: the F2F bump width (diameter) and distance between two dies. This is because if the distance between two dies remains the same but the bump width scales, the bump must be manufactured to have a taller height, which would lead to reliability issues. If bump width does not scale, we cannot obtain denser I/Os. Several studies have reported bump widths in the 1μm to 5μm range [4, 5, 6]. Furthermore, F2F distances on the order of 5μm [7] and 1μm have been reported [8]. Studies have also reported direct copper-to-copper bonding that does not require any distance between dies at all [9]. Above all, these scaled F2F bonding technology proved to be reliable. Reference [10] showed that more than 3000 I/O pads were successfully bonded with these small-sized F2F bumps.

Despite the rapid scaling in F2F bonding technology, F2F bonding impact on die-to-die coupling has not been thoroughly investigated. In this paper, we study inter-die capacitive interactions when a 3D IC is implemented using a F2F bonding style. Using a field solver-based modeling methodology, we examine three critical aspects of capacitance in F2F bonded 3D ICs:

1) We explore the various physical and process factors that affect F2F parasitics.
2) We quantify the level of error that occurs if inter-die interactions are not considered for various process and layout scenarios.
3) We study how the F2F bump, which is a defining feature of F2F 3D ICs, impacts capacitance.

The results indicate that inter-die capacitive interactions in F2F 3D ICs can be significant and depend on a number of geometric and process variables. Inter-die coupling between the top metal layers, which is typically not significant for TSV-based 3D ICs, becomes critical in F2F 3D ICs when the distance between the two dies becomes smaller than 10μm. The coupling capacitance between conductors in the top-metal layers of each die is also influenced due to the shielding of the inter-die conductors. Therefore, in these scenarios, significant capacitance error occurs when inter-die interactions are not considered during extraction. Furthermore, F2F bumps produce significant bump-to-metal capacitance and increase the error in top-metal capacitances. The results presented in this paper have important implications for both the interconnect extraction and design of F2F bonded 3D ICs with high density micro bumps.

Our paper is structured in the following manner: Section II explains the preliminaries of this work and how our field solver-based models are made. In Section III, we explore the various factors that affect F2F parasitics. In Section IV, we visualize the level of error that occurs when inter-die interactions are not considered. In Section V, we explore the impact of F2F bumps on the parasitic capacitance. Finally, the conclusions and acknowledgement are in Section VI and Section VII.

II. Preliminaries

A. Limitations on the Top-Metal for F2F Structures

To provide meaningful results through our study, we start with the following question: "How thick should the top metal be?" Top metals are used for various purposes such as signal routing, power delivery network design, and I/O pads for interconnection to package and PCB. When the top-metal is used for I/O pads, its thickness becomes very important. Since designed chips must go through testing, these top-metal I/O pads are the ones that are also used as probing pads during testing procedure. Note that testing probes can cause significant damage on the I/O pads. From Figure 1, it is shown that these I/O pads collapse more than 400nm after a single probe touchdown [11]. Therefore, despite the technology scaling expected on the interconnects of ICs, we assume that the top-metal will have certain limitations on the minimum thickness in order to become robust during testing. In other words, we will assume that the top-metal is thicker than 0.6µm (400nm + margin) in our test structures so that the top-metal do not break during testing.

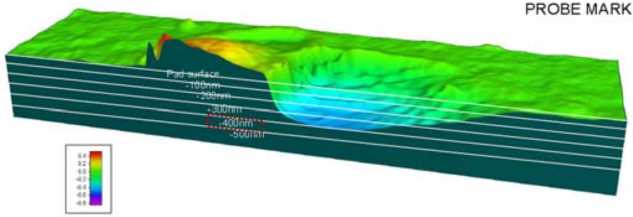

Figure 1. Damage caused to probe pad after testing [11].

Table 1. Metal dimensions used in this study

	Width	Spacing	Height
RDL (Thick top metal)	1.8 µm	1.8 µm	2.8 µm
M9 (Thin top metal)	0.36 µm	0.36 µm	0.85 µm
M8	0.18 µm	0.18 µm	0.5 µm

B. Top Metal Candidates

We perform our study based on a typical interconnect structure used in an industrial CMOS process technology. Table I shows the dimensions of the metal we use in our study. Figure 2 (a) shows the cross section of the top-metal interconnects in our CMOS technology, and (b) shows the cross section when two dies are stacked in F2F. Due to the damage caused to the top-metal by testing described on Section II-A (-400nm), we limit our study to see the impact of F2F coupling on the top metals that are thick enough. Thus, RDL and M9 are the top-metal candidates that we perform our study. From now on, we will describe RDL as "thick top metal (TK)" and M9 as "thin top metal (TN)". Note that we exclude M8 as a top-metal candidate for our study because it is not thick enough. Through our study, we will refer to the top-metal as "*T*" and the metal below the top metal as "*T-1*". For example, in TK case, RDL will be the top-metal (*T*), and M9 becomes the one below (*T-1*). In TN case, M9 becomes the top-metal, and M8 becomes the one below.

C. Test Structure

When chips stack in F2F, distance between metal layers is an important factor that impacts the coupling capacitance between dies. In this paper, we use "bump height" [Figure 2 (b)] as the metric that describes the distance between metal layers. The dielectric and passivation that covers the top-metal should be open so that F2F bumps can make connection between two top-metal layers. Thus, as these dielectrics are removed from the top-metal, the height of the bonded bumps will be the distance between top-metals in F2F stacking.

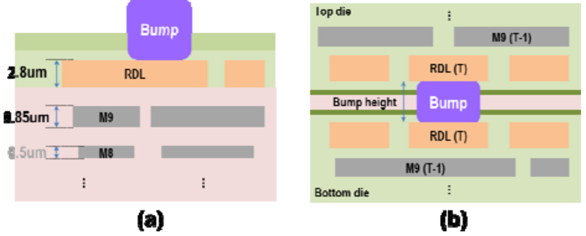

Figure 2. Interconnect structure used in our study. (a) Top metal layers in an individual die. (b) Two dies are stacked in F2F 3D IC. Bump height is the distance between two dies.

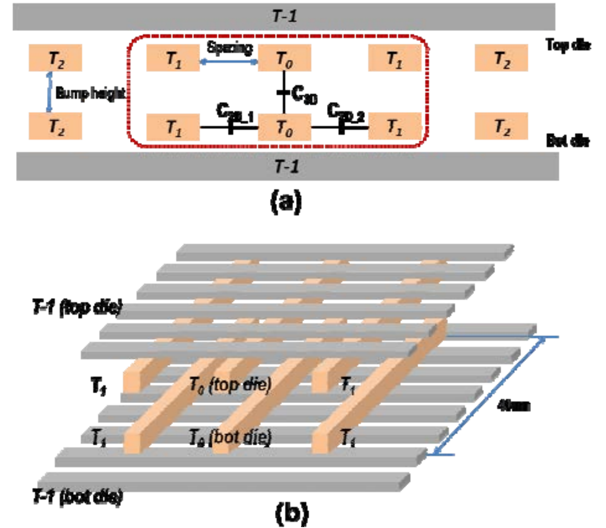

Figure 3. General test structure used in this study. (a): Cross-sectional view, (b): 3D view showing the top-metals inside the red box of (a).

Figure 3 depicts the general 3D test structure used in the experiments in this paper. Based on this test structure, we plan to see how the coupling capacitance changes between the top metal T_0 of the top die and bottom die (C_{3D}). To determine its significance, C_{3D} will be compared with the capacitance (C_{2D_1} and C_{2D_2}) between the top metals in the same die. The length of all top metal is 40µm. *T-1* wires are placed orthogonal to *T* wires and are placed on its minimum pitch. *T-1* wires are long and dense enough to cover all area occupied by the top metal. By this, we assume that the metal layers below the top-metal are fully occupied. This models the maximum field impact from *T-1* and below so that C_{3D} becomes the minimum. Using this test structure, we conduct analysis on two different top-metal cases: TK and TN.

We use Synopsys QuickCap NX [12] for our practical simulations. First, we build the model considering all details mentioned. Then, we extract the capacitances from the model. Using the extracted capacitances, we perform analysis in the following sections to examine the impact of F2F bonding.

III. F2F Capacitance

In this section, we analyze how significant F2F capacitance (C_{3D}) is compared to the capacitance formed between metals in the same die [$C_{2D} = (C_{2D_1} + C_{2D_2})/2$]. We also analyze the factors that impact C_{3D}. Here, we define *3D Cap. Ratio* as in Equation 1

$$3D\,Cap.\,Ratio = \frac{C_{3D}}{C_{2D}} \times 100[\%] \qquad (1)$$

Where C_{3D} and C_{2D} are the capacitances described in Figure 2 (a). "*3D Cap. Ratio* > 100%" means that the C_{3D} is bigger than C_{2D}. On the other hand, "*3D Cap. Ratio* < 100%" means that C_{2D} between wires is bigger than C_{3D} that F2F capacitance is less than C_{2D}. In the following subsections, we first analyze the impact of F2F bonding in thick top-metal (TK) and thin top-metal (TN). Then, we analyze other various scenarios that impact F2F capacitance in actual designs.

A. F2F Bonding Impact on Thick Top Metal (TK)

Figure 4 shows how the *3D Cap. Ratio* changes when various parameters of the top metal change: bump height, TK spacing, TK width, and TK thickness. Unless specified, the bump height and TK spacing is 5µm in all designs, and other design parameters follow the specifics of Table I. First, (a) shows how *3D Cap. Ratio* changes when the bump height changes from 3µm to 30µm. Results show that as bump height decreases, *3D Cap. Ratio* increases significantly (321% when bump height is 3µm). This is because bump height increase leads to both C_{2D} increase and C_{3D} reduction at the same time. In addition, when the bump height is over 10µm, *3D Cap. Ratio* becomes significantly lower than the 2D capacitance. This shows why in previous F2F bonding technologies, when the bump height was sufficiently tall (>10µm), F2F coupling was not a critical issue.

Second, Figure 4 (b) shows how *3D Cap. Ratio* changes when the spacing of TK varies from 1µm to 10µm (bump height: 5µm). Note that *3D Cap. Ratio* changes from 6.5% to more than 800% based on the top-metal spacing. When spacing between top metals increase, C_{2D} reduces, but C_{3D} increases at the same time. Depending on the spacing between top metals on the same die, C_{3D} becomes significantly higher than C_{2D}.

Third, Figure 4 (c) shows how *3D Cap. Ratio* changes when the TK width changes from 1µm to 10µm. As TK width increases, the *3D Cap. Ratio* increases as well. This is because when the width of the TK increases, it increases the surface capacitance between the top metals in both dies (C_{3D}). Notice that the impact of TK width on the *3D Cap. Ratio* is linear and not quadratic. C_{3D} is the only variable that changes, and TK width change has negligible impact on the change on C_{2D}. Fourth, Figure 4 (d) shows how *3D Cap. Ratio* changes when the TK thickness changes from 1µm to 5µm. As TK thickness increases, we see a steady decrease in the *3D cap. ratio*. When TK thickness increases, the capacitance between the top metal layers (C_{2D}) increase due to the increased coupling surface. However, this does not impact C_{3D} much since the coupling surface between TKs on the top and bottom die remains the same.

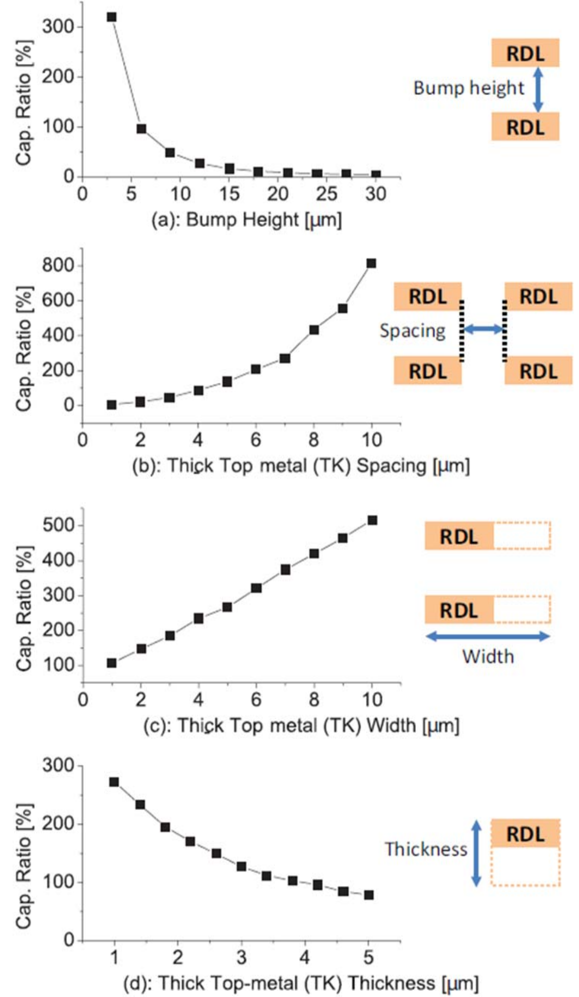

Figure 4. *3D Cap. Ratio* change due to various parameter changes in thick top-metal (TK). (a): Bump height, (b): TK spacing, (c): TK width, (d): TK thickness

B. F2F Bonding Impact on Thin Top Metal (TN)

Figure 5 shows the *3D Cap. Ratio* change when various parameters of the thin top-metal (TN) change: bump height, TN spacing, TN width, and TN thickness. Here, we use a more advanced bump height of 1µm. In addition to the bump height, we fix the spacing between TN to be 1µm in all experiments unless specified. Figure 5 shows a similar trend as in Figure 4, but few differences occur that are unique in TN. First, Figure 5 (a) shows that as bump height decreases, C_{3D} increases. However, notice that (1) the overall *3D cap. Ratio* is smaller than in the TK case, and (2) 3D capacitance do not become bigger than 2D capacitance until the bump height is 1µm. This shows that TN will not suffer from 3D capacitance as much as TK does. Second, Figure 5 (b) shows that when the spacing in thin top-metal increases, 3D capacitance increase. However, the 3D capacitance increase

ratio is steeper in TN compared to the TK case. This is because the bump height in TN is smaller than in TK. Detailed analysis regarding spacing-height relationship will be discussed in Section III-C. Third, Figure 5 (c) shows how *3D Cap. Ratio* changes when the width/thickness of thin top-metal changes. Despite that exact numbers of the 3D capacitance ratio are not same as in Figure 4 (c) and (d), a similar trend is shown.

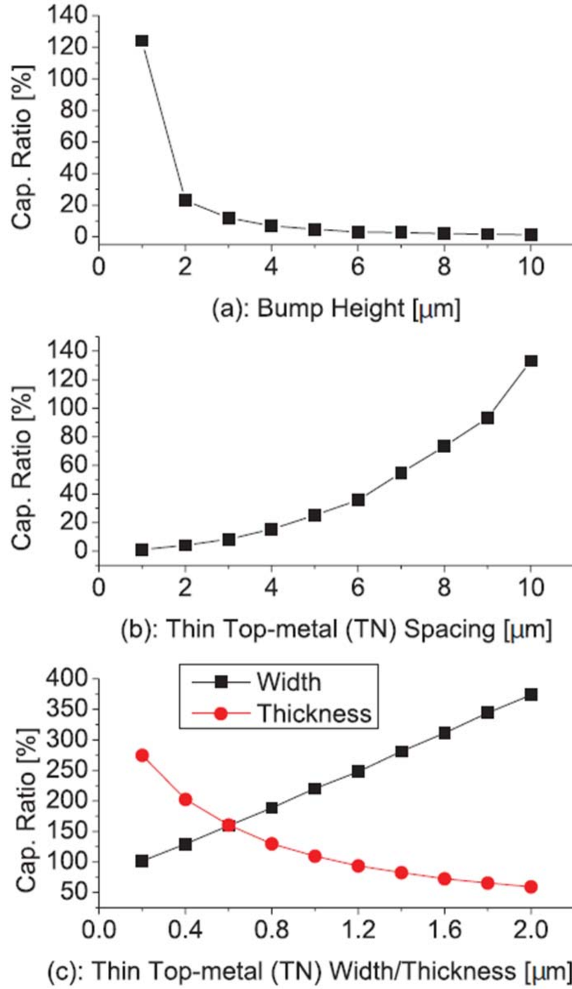

Figure 5. *3D Cap. Ratio* change due to various parameter changes in thin top-metal (TN). (a): Bump height, (b): TN spacing, (c): TN width/thickness

C. Spacing-Height Relationship on F2F Capacitance

Sections III-A and III-B showed a similar trend in bump height and top-metal spacing on *3D Cap. Ratio.* From this inspiration, we study how *3D Cap. Ratio* changes when bump height and the top-metal spacing changes at the same time. Figure 6 shows the results in thick top-metal case. We see from Figure 6 that *3D Cap. Ratio* is not affected by just one factor, but affected by both bump height and top-metal spacing at the same time. Note that when the bump height is the same as the metal spacing, *3D Cap. Ratio* becomes almost 1 (blue line). If the metal spacing is larger than the bump height, C_{3D} is always bigger than the C_{2D}. However, if bump height is larger than the metal spacing, C_{3D} always becomes smaller than C_{2D}. For example, when bump height is 1.4µm and TK spacing is 2.6µm, C_{3D} becomes 2.5x larger than C_{2D}. However, when bump height/TK spacing is 8.0/4.4µm, C_{3D} is only 40% of C_{2D}. Analyzing the results in Section III-A, notice that *3D Cap. ratio* was almost 100% when bump height was similar to the TK spacing [see Figure 4(b)]. Similar in Section III-B, 3D cap. reaches 100% when the bump height is the same as the spacing of the thin top metal (1µm) [Figure 5(b)].

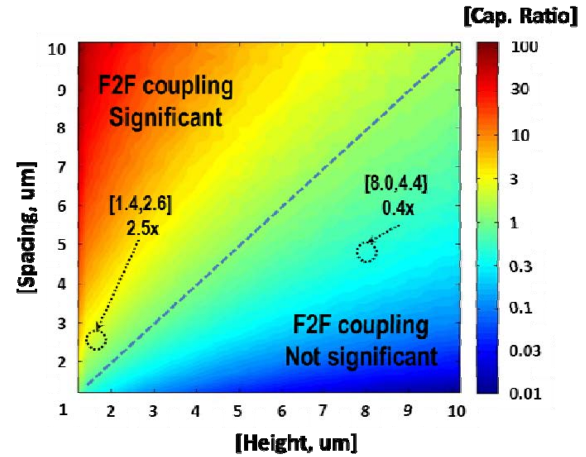

Figure 6. Impact of metal-spacing/bump-height on 3D capacitance on TK

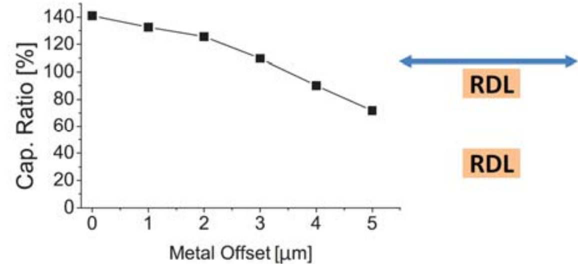

Figure 7. *3D Cap. Ratio* when offset of top-tier changes

D. Impact of Offset Variation

Figure 7 shows how *3D Cap. Ratio* changes when the offset of the top metal changes in TK. We vary the location of the top tier metals from 0 to 5µm and see how C_{2D} and C_{3D} changes when TK spacing/bump height are both 5µm. From the change of the offset, we see significant change in the *3D Cap. Ratio*. Note that the change of *3D Cap. Ratio* occurs purely from the change of C_{3D} since the offset variation will not affect any change in C_{2D}. Note that changing the offset of the chip will reduce C_{3D} of one top-bottom metal pair, but will increase C_{3D} formed by another top-bottom metal pair. Thus, rather than placing top and bottom tier to directly face each other, changing the offset of one tier by a few µm will reduce the 3D capacitance. However, changing the offset of a chip more than one pitch will not help reducing C_{3D}. For example, if the offset is altered by exactly one pitch, the impact will be neutralized and offset changing will not do any benefit.

E. F2F Coupling in Different Top-metal Directions

The previous sections discuss the impact of coupling on F2F structures when two top metals were facing the same

direction. We now examine F2F coupling when the directions of two top metals are different from one another. Figure 8 (a) shows how the test structure changes when the top-die is rotated by 90° in TK. The same dimensions are used as in Section III-A. Figure 8 (b) shows the extraction results in non-rotated case, and (c) shows the results in 90° rotated case. First, rotating the top tier by 90°, we see that C_{3D} per unit metal reduces. For example, in (b), C_{3D} between the top metals is 0.899fF. However, in (c), the biggest C_{3D} between the victim and one top-tier metal is 0.259fF. Notice that C_{3D} per net reduces in 90° rotated structure. However, the total C_{3D} that a victim sees in both orientations is similar. When measuring the total C_{3D} of the bottom tier victim ["V" in Figure 8 (b) and (c)], non-rotated case gives us 1.395fF and 90° rotated case gives us 1.479fF, which the total C_{3D} is similar in both cases.

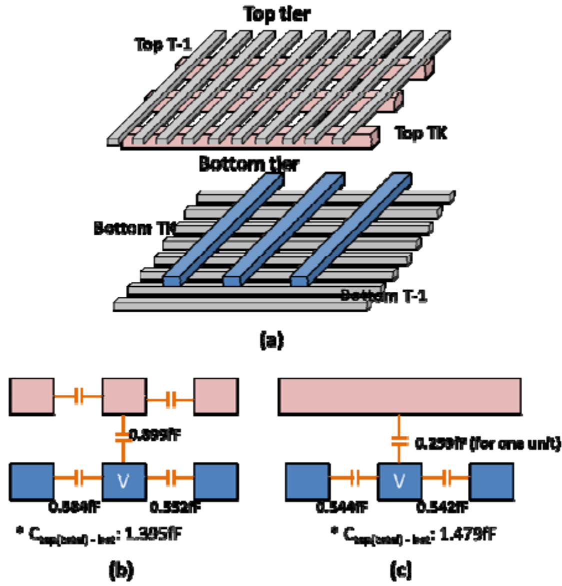

Figure 8. Top die rotated by 90°. (a) 3D view of the 90° rotated test structure. (b) Capacitance values in non-rotated structure. (c) Capacitance values in 90° rotated structure.

IV. Capacitance Error Caused by F2F Bonding

Conventional parasitic extraction on F2F bonded 3D ICs normally extracts the parasitics of each die separately and stitches them together as in Figure 9 (a) [3]. We will call this "Separate Extraction". However, when the F2F bump sizes become smaller, the accuracy of the extracted capacitances in Separate Extraction decreases. Therefore, extracting the F2F capacitance holistically [Figure 9 (b)] should be considered for accurate extraction. We will call this "Holistic Extraction". In this section, we first report how much error Separate Extraction causes in F2F structures, and then study how the error changes due to various parameter changes.

A. Case Studies in Different Bump Sizes

Using the same test structure as in Figure 3 (b), Table II shows two capacitance values in different extraction methodologies in thick top metal: (1) the total capacitance formed in the test structure, and (2) the capacitance sum of the top metal (C_{2D}). First we perform Separate Extraction on the 3D structure, and report the capacitance inside the whole structure. Here, we obtain 10.0fF for the total capacitance, and 2.0fF for the C_{2D} formed on the top-metal layers (sum in top and bottom die). Notice that this will be the capacitance value when a 3D F2F structure is extracted in Separate Extraction at any bump height. When the bump height is 5µm, however, the total capacitance is 10.2fF, and 2D top-metal capacitance is 1.3fF. This difference cannot be captured when using Separate Extraction. When the bump height is 1µm, the total capacitance becomes 15.3fF and 2D top-metal capacitance becomes 0.71fF. This means that when bump height becomes shorter, Separate Extraction will cause more unwanted error. Especially, e.g., when the bump height is 1µm, the error caused will be -34.6% (Separate Extraction estimates less capacitance then the correct value) in total capacitance, and 2.82x (Separate Extraction estimates more capacitance then the correct value) in the top-metal capacitance. Note that as C_{3D} increases in a F2F structure, C_{2D} will see positive error since Separate Extraction always overestimates, and the total capacitance will see negative error since Separate Extraction always underestimates it.

Table 2. Cap. of test structure on different bump height

Height	Sep. Extract	5µm	1µm
Total Cap. (fF)	10.0	10.2	15.3
2D Top-metal Cap. (fF)	2.0	1.3	0.71

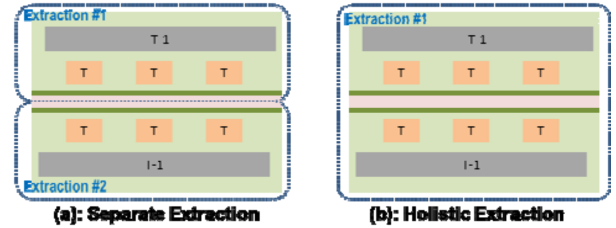

Figure 9. Illutration of two extraction schemes: (a) Separate Extraction, (b) Holistic Extraction

B. F2F Bonding Impact on Capacitance Error

Figure 10 shows how the capacitance error changes due to bump height and top metal spacing on thick top metal. Our baseline is Holistic Extraction in our test structure, and we compare how much difference occurs in Separate Extraction compared to Holistic Extraction. From Figure 10 (a), we see that the absolute capacitance error increases as the bump height decreases. First, we see significant C_{2D} error when the bump height is 1µm (180.7%) and even when bump height is 10µm (22.4%). This means that Separate Extraction miscalculates the capacitance between the top metals when dies become closer in F2F bonding. Second, despite the large C_{2D} error from Separate Extraction, the total capacitance error is not that significant. When bump height is taller than 2µm, the total capacitance error converges to 0. This is because as C_{2D} reduces, C_{3D} increase at the same time resulting in small total capacitance difference. Therefore, the total capacitance does not change significantly. However, when the bump height becomes very small (< 2µm), C_{3D} increases faster than

C_{2D} reduction. This is why the absolute total capacitance error increases significantly in small bump heights.

Figure 10 (b) shows how the capacitance error changes when the top metal spacing change in 2μm bump height. As the top metal spacing increases, both C_{2D} and total capacitance error (absolute value) increase, because TK spacing increase in fixed bump height increases C_{3D} and decreases C_{2D}. Since the results of C_{2D} in Separate Extraction assume no obstacles over the top metal, it disregards the increase of C_{3D} due to top metal spacing. Therefore, C_{2D} error increases as the top metal spacing increase, and this also leads to the error in total capacitance.

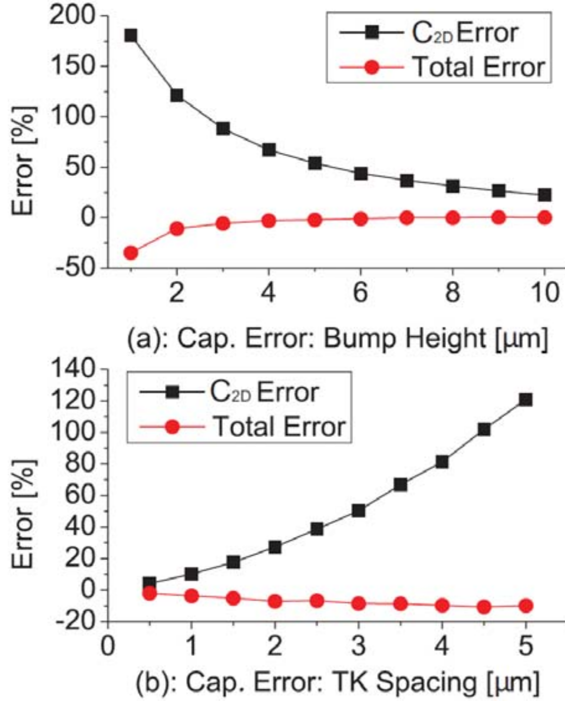

Figure 10. Capacitance error variation when using Separate Extraction scheme: (a) Bump height, (b) TK spacing

V. Impact of F2F Bumps on F2F Capacitance

In the previous sections, we assumed test structures where the bumps are not in between the top metal layers. However, knowing that F2F bumps highly affect the capacitance in F2F structures, we see how capacitance changes when F2F bumps are near the top metals.

A. Test Structure

We build a test structure to visualize the impact of F2F bumps on F2F capacitance using the same metal dimensions as in Section II. Figure 11 shows the details. Top metal lengths are 40μm, and the bump diameter varies from 1μm to 10μm. The bumps are placed in the middle of the top metal. In this test structure, we assume a bump that has not penetrated through the passivation and dielectrics. For example, in 10μm bump, we assume that bump-to-metal distance is 10% of the bump size (1μm). This means that the F2F distance between top metals is 10μm, but the actual bump height is 8μm due to the passivation. For 5μm and 1μm bump, the bump-to-metal distance becomes 0.5μm and 0.1μm. In this test structure, we add F2F bumps and see how C_{2D} and C_{Bump} (Capacitance between the bump and top metal as depicted in Figure 11) change when parameters vary. We define *Bump Cap. Ratio*, which is a similar metric to *3D Cap. Ratio*, to see how significant the F2F bump capacitance is to top-metal capacitance.

$$Bump\ Cap.\ Ratio = \frac{C_{Bump}}{C_{2D}} \times 100[\%] \qquad (2)$$

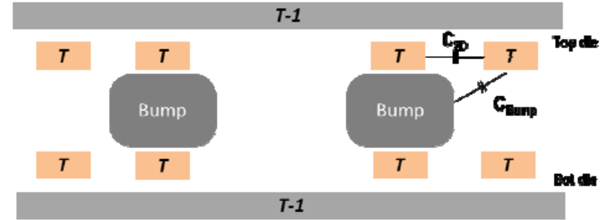

Figure 11. Test structure with bumps in F2F Bonding

B. F2F Bump Impact to Top-Metal Capacitance

Figure 12 shows how *Bump Cap. Ratio* changes in TK (a) and in TN (b). First, we see from both TK and TN that as the top metal spacing increases, *Bump Cap. Ratio* increases. Notice that as the spacing increases, C_{Bump} becomes significantly higher than C_{2D}. As in previous sections, IC designs that have less density in top metal will suffer more from bump capacitance. Second, as the bump height decreases due to the technology scaling, the impact of bump on capacitance reduces. Since the size reduction of bump translates to smaller coupling area, the impact of bump capacitance will reduce as well. Third, TN shows more *Bump cap. ratio* than TK in the same metal spacing. This is because a stronger C_{2D} forms between the TK than TN. Since the metal dimensions of TK is bigger than TN, *Bump Cap. Ratio* shows a bigger value in TN.

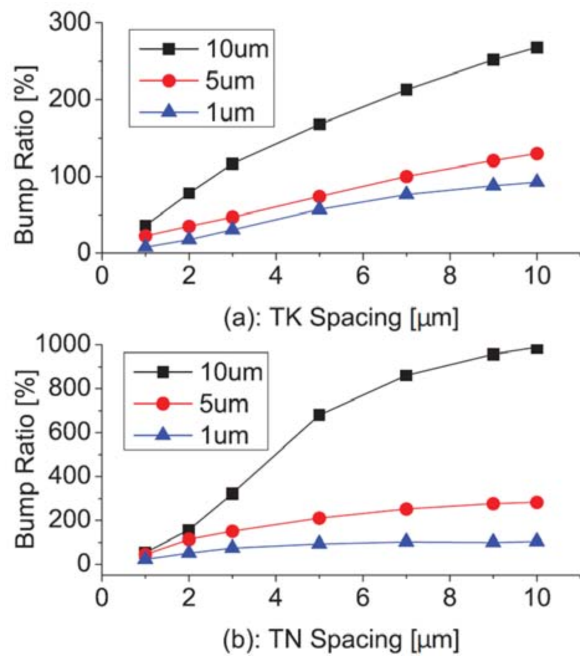

Figure 12. *Bump Cap. Ratio* change due to various parameter changes: (a) TK spacing, (b) TN spacing. Squares, circles, and triangles denote 10, 5, and 1 µm of bump size, respectively.

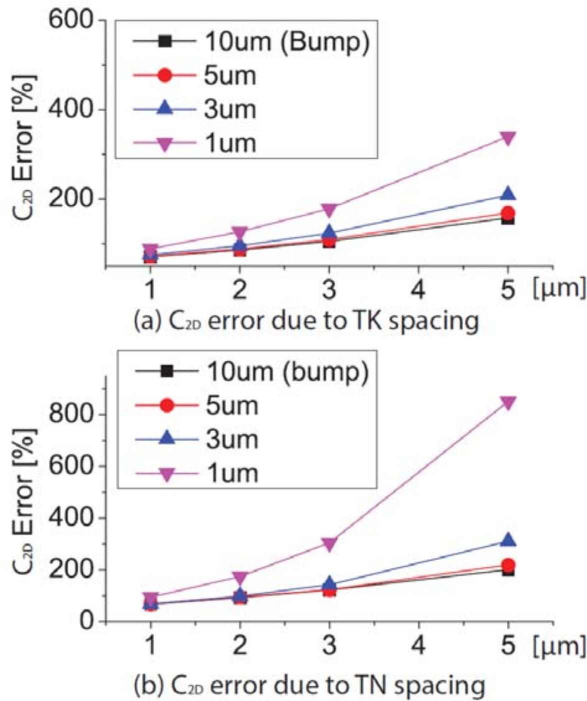

Figure 13. Capacitance C_{2D} error variation. (a): TK spacing, (b): TN spacing. Squares, circles, up-triangles, and down–triangles denote 10, 5, 3, and 1 µm of bump size, respectively.

C. Capacitance Error Due to F2F Bump

In this subsection, we study how much C_{2D} error occurs when the top-metal spacing and bump height changes. Our baseline is Holistic Extraction, and from this baseline, we see how inaccurate it can be when F2F bumps between dies are not considered. Figure 13 (a) and (b) show C_{2D} errors in TK and TN, respectively. First, more C_{2D} error occurs as the spacing between metal increases. When the distance between top-metals become farther, the E-field from F2F bump that impacts the victim becomes stronger. Therefore, C_{2D} miscalculation occurs more as the spacing increases. Note that more than 60% error occurs even with 1µm metal spacing. Second, C_{2D} error occurs more as the bump size becomes smaller. Notice that when the bump size scales, we also assumed that the top-layer passivation thickness scales as well. Since top-metals will be affected more from bumps that are closer, we will see more error as the bump shrinks. Third, TN shows more error than TK. For example, C_{2D} error in TN (94.5%) is more than in TK (88.6%) in 1µm bump/spacing. Since the physical dimensions of TN are smaller than TK, TN is more sensitive to E-field change by objects. Therefore, TN shows more error than TK even with the same external conditions.

Conclusions

In this paper, we studied the inter-die capacitance trends for various physical and process parameters when a 3D IC is implemented using a F2F bonding style. Based on the results, there are several general conclusions:

1) For the thick top metal layers in each die, the impact of inter-die capacitive interactions is significant when the distance between the two dies is smaller than 10 microns.
2) For the thinner metal layer below the top metal layer, the impact of inter-die capacitive interactions only becomes significant once the bump distance is smaller than 3 microns.
3) In the aforementioned process configurations, significant capacitance errors can occur when inter-die interactions are not considered in conventional parasitic extraction methods. This includes both the coupling capacitance between top metal wires in the same die (C_{2D} - overestimated due to missing inter-die shielding effects) and the coupling capacitance between top metal wires in different dies (C_{3D} - ignored).
4) Orthogonal RDL routing in facing dies can reduce inter-die coupling capacitance between individual wires. However, total capacitance and the intra-die coupling capacitance are similar to the scenario where the RDL wires are routed in parallel to the facing dies.
5) The F2F bumps greatly impact the parasitics of F2F bonded structures regardless of the distance between the two dies. This includes both the bump-to-metal capacitance (C_{Bump}) and the metal-to-metal capacitance (C_{2D}).

These conclusions have important implications for both the interconnect extraction and design of F2F bonded 3D ICs with high density micro bumps. Extraction tools will need to adaptively detect the distance between the two dies in a given process where inter-die capacitive interactions become significant in order to effectively balance accuracy and

computational overhead. Designers and design tools may also need to consider the routing orientation of RDL layers as well as the impact of inter-die parasitics on timing, noise, and reliability in order to fully realize the potential of F2F bonded 3D ICs.

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References

1. Y.-J. Lee and S. K. Lim, "On GPU bus power reduction with 3D IC technologies," in Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014, March 2014, pp. 1–6.
2. Samsung Starts Mass Producing Industry's First 3D TSV Technology Based DDR4 Modules for Enterprise Servers, http://www.samsung.com/.
3. M. Jung et al., "On enhancing power benefits in 3D ICs: Block folding and bonding styles perspective," in Design Automation Conference (DAC), 2014 51st ACM/EDAC/IEEE, June 2014, pp. 1–6.
4. Y. Ohara et al., "10 um fine pitch Cu/Sn micro-bumps for 3-D super-chip stack," in 3D System Integration, 2009. 3DIC 2009. IEEE International Conference on, Sept 2009, pp. 1–6.
5. M. Motoyoshi and M. Koyanagi, "3D-LSI technology for image sensor," Journal of Instrumentation, vol. 4, no. 03, p. P03009, 2009. [Online]. Available: http://stacks.iop.org/1748-0221/4/i=03/a=P03009
6. M. Murugesan et al., "High density 3D LSI technology using W/Cu hybrid TSVs," in Electron Devices Meeting (IEDM), 2011 IEEE International, Dec 2011, pp. 6.6.1–6.6.4.
7. K. Lee et al., "3D integration technology and reliability challenges," in Electrical Design of Advanced Packaging and Systems Symposium (EDAPS), 2011 IEEE, Dec 2011, pp. 1–4.
8. M. Motoyoshi et al., "Stacked SOI pixel detector using versatile fine pitch u-bump technology," in 3D Systems Integration Conference (3DIC), 2011 IEEE International, Jan 2012, pp. 1–4.
9. L. Peng et al., "High-Density 3-D Interconnect of Cu-Cu Contacts With Enhanced Contact Resistance by Self-Assembled Monolayer (SAM) Passivation," Electron Devices, IEEE Transactions on, vol. 58, no. 8, pp. 2500–2506, Aug 2011.
10. C.-K. Lee et al., "Wafer bumping, assembly, and reliability assessment of ubumps with 5 um pads on 10 um pitch for 3D IC integration," in Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd, May 2012, pp. 636–640.
11. K. Karklin, J. Broz, and B. Mann, "Bond Pad Damage Tutorial," in IEEE Semiconductor Wafer Test Workshop, 2010.
12. Synopsys QuickCap NX, http://www.synopsys.com/ .