Multi-TSV and E-Field Sharing Aware Full-chip Extraction and Mitigation of TSV-to-Wire Coupling

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***Abstract*—The through-silicon-via (TSV) introduces new parasitic components into 3-D ICs. This paper presents a novel method of extracting the parasitic capacitance between TSVs and their surrounding wires. For the first time, we examine electrical field (E-field) sharing effects from multiple TSVs and neighboring wires and their impact on timing, power, and noise with full-chip sign-off analyses. For fast and accurate full-chip extraction, we propose a pattern-matching algorithm that accounts for the physical dimensions of multiple TSVs and neighboring wires and captures all E-field interactions. Compared with the average error of a field solver, that of our extraction method, which requires only 2.4 s runtime and negligible memory for a full-chip 64-point fast Fourier transform (FFT64) design with 330 TSVs, is 0.063fF. Upon extraction of TSV-related parasitics, we observe that TSV-to-wire capacitance significantly increase average TSV net noise and the longest path delay. To reduce TSV-to-wire coupling, we implement two full-chip optimization methods and show that increasing the minimum distance between TSVs and neighboring wires reduces both coupling noise and the aggressor count. Thanks to E-field sharing from grounded wire guard rings, victim TSVs are more effectively shielded from aggressor noise. A full-chip analysis shows that these methods are highly effective in reducing noise with only slight impact on timing and area.**

***Index Terms*—3-D IC, full-chip, noise optimization, parasitic extraction, signal integrity, through-silicon-via (TSV)-to-wire.**

I. Introduction

ONE promising solution to extend the Moore's law is 3-D ICs. The through-silicon-via (TSV) is used for vertical interconnection in 3-D ICs and provides wide connections between the top and bottom dies. TSVs allow 3-D ICs to have ultrahigh density and bandwidths but much lower power consumption for data transmission. Fig. 1 shows a 3-D IC structure in which two dies are bonded from face-to-back with via-first technology [1]. Because of increased wire and TSV density, parasitic components between TSVs and wires become important contributors to signal coupling in 3-D ICs. One way to avoid heavy TSV-to-wire coupling is to leave a large keep-out zone (KOZ) around the TSV or provide additional shielding around critical signals. However, these techniques are not cost efficient because the area and wirelength increase dramatically. A smarter choice is to carefully extract coupling elements from TSVs based on their physical sizes as well as silicon substrate effects and perform signal integrity analysis to ensure that timing and noise are under control. This process is particularly critical for advanced technologies and mobile applications, in which the supply voltage is low and the signal swing is reduced for low power operation, to obtain a good signal-to-noise ratio (SNR) and a low bit error rate.

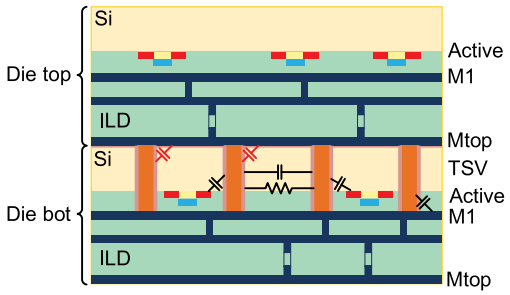

Fig. 1. TSV-related coupling capacitance in a two-die 3-D IC structure.

Many previous studies have analyzed TSV-related parasitic components and their impact on noise and timing. Since TSVs are much larger than regular vias, and they are buried inside the silicon substrate, which has a large relative permittivity (11.9), TSVs have significantly larger capacitance than regular vias. Also, since the substrate body contains no other conductors, an unblocked electrical field (E-field) of the TSV results in few but large capacitors inside the substrate. A major portion of TSV capacitance comes from TSV MOS capacitance, which can be modeled with a series connection of an oxide capacitor and a depletion region capacitor [2]. TSV MOS capacitance can be calculated by analytical equations, though it is hard to predict residue charges inside the oxide liner. Depending on the TSV dimension, the oxide thickness, and substrate doping, MOS capacitance can reach more than 50fF, and most coupling paths around TSVs are formed through this capacitor.

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Previous studies on TSV-to-TSV [3]–[7] and TSV-to-active [7]–[10] coupling focus on a single die. Since TSVs penetrate the silicon substrate when multiple dies are stacked in 3-D ICs, noise not only comes from the same die that the TSV is located on but also from a neighboring die through substrate coupling. Particularly in the full-chip level, TSV farms in the bottom die may overlap with congested routing regions in the top die. For interdie coupling, a parasitic element often ignored in current analyses is TSV-to-wire capacitance. Since TSVs are significantly larger and longer than regular vias, their E-fields cannot be captured with the traditional metal via handling. Because of the geometric complexity of a cylindrical TSV shape, the TSV extraction is more challenging than square vias. If a tapered TSV is used, their unevenly-distributed E-fields are even harder to extract. Moreover, unlike devices, TSVs penetrate the substrate, and their E-fields interact with many surrounding wires and components. Even for industry-standard extraction tools such as Calibre, only TSV-to-TSV coupling, not TSV-to-wire coupling, is extracted. Since active regions are connected to the power or ground supply, they form an E-field shield in the ac domain. Thus, only weak coupling exists between TSV-to-M1 in the same die. However, the other side of the substrate has no substrate connection shielding TSV E-fields, resulting in large coupling capacitance between TSVs and the top metal layer of the neighboring die. Therefore, TSV-to-wire coupling needs to be accurately extracted for timing, power, and noise analyses.

Although interdie coupling is becoming more dominant with advanced technologies in which a thinner substrate is used to reduce the TSV dimension, few studies have addressed coupling issues from the standpoint of interdie impact. Coupling issues affect the signal gain and resonance frequency in components such as TSV-based inductors [11] as well as performance and signal integrity in full-chip designs. Measurement results from [12] show that when the signal frequency is higher than 1 GHz, intertier coupling is greater than intratier coupling. Liu *et al.* [13] found that TSV-to-metal coupling impacts analog devices and showed that TSV-to-metal coupling has a non-negligible effect on the SNR. However, extraction is limited to coupling between wires and TSV landing pads. TSV-to-wire parasitic extraction using a field solver is discussed, and Salah [14] concluded that TSV-to-wire capacitance is not negligible for TSVs with a low aspect ratio. Assuming square-shaped TSVs, Kim *et al.* [15] derived an analytical solution and extended the empirical wire coupling model to handle TSV structures. Since this model is based on closed-form formulas, calculations consume only negligible runtime. However, the model is not scalable because empirical equations handle certain fabrication technology, and curve fitting with various interconnect dimensions needs to be applied. As TSVs are fabricated in cylindrical shapes, the square-TSV assumption also introduces extra errors from geometric approximations.

Another general solution for capacitance extraction is based on a random-walk algorithm [16]. Commercial interconnect extraction engines such as Raphael NXT also use this algorithm for extraction from general structures. Random-walk-based extraction consumes shorter runtime than field solver-based extraction. However, achieving comparable accuracy requires many random walks and hops to capture the E-field distribution, especially with many conductors. As a result, a long extraction time is still needed on the full-chip level. Therefore, random-walk-based extraction is suitable for small designs for the purpose of sign-off verifications, but cannot be applied to fast parasitic extraction during placement and routing stages for timing and noise optimization purposes. Yu *et al.* [17] proposed a random-walk-based TSV-to-wire extraction method with precalculated look-up tables that closely matched a field solver. However, the performed extraction is based on randomly-generated layouts, so the full-chip impact from TSV-to-wire remained unknown.

To alleviate TSV coupling noise, several studies have proposed noise reduction methods. Several shielding techniques such as ground TSVs [18], [19] and ground plugs [20] are used to protect TSVs from TSV-to-TSV coupling noise. Because ground TSVs also similarly impact TSV-to-wire coupling, they can also be used as a TSV-to-wire coupling reduction technique. Measurement results from [21] show that H-shaped TSVs provide better shielding than guard rings. However, these techniques either consume large silicon areas and reduce placement utilization or require special fabrication technology and increase the chip cost.

In this paper, Section II studies impact of E-field sharing from multiple neighboring wires. Section III presents our pattern-matching algorithm with verification against a field solver. Section IV studies multi-TSV impact on TSV-to-wire coupling with verification. Section V applies our pattern-matching method to a 3-D IC layout and studies impact of TSV-to-wire coupling on the full-chip level. Section VI studies two full-chip optimization techniques that alleviate TSV-to-wire coupling, and Section VII concludes this paper.

II. E-Field Sharing Impact

A. TSV Influence Region

Since capacitance is geometry dependent, the interconnect dimension significantly affects coupling capacitance. A large TSV results in stronger coupling as its E-field affects more neighbor conductors. We define a TSV influence region for TSV-to-wire extraction, and only wires within the influence region have their coupling capacitance extracted. We build a special structure, in which a TSV is surround by a wire ring, to study the TSV influence region. The TSV radius is 2.5 μm and height is 15 μm. The ring has the same width (0.14 μm) and thickness (0.28 μm) as wires in M4–M6 layers of a 45 nm technology. Low-K materials are used in the interlayer dielectric layer with a relative permittivity of 2.2. This symmetrical structure is used so that TSV-to-wire distances are the same for all parts of a wire ring.

Single-ring-extraction results are shown in Fig. 2(a) with various TSV dimensions. A short TSV does not heavily affect faraway wires, and most of its E-field is restricted within a 10 μm range. However, a tall TSV affects wires as far as 20 μm. We use bump-less 3-D IC technology [22] and

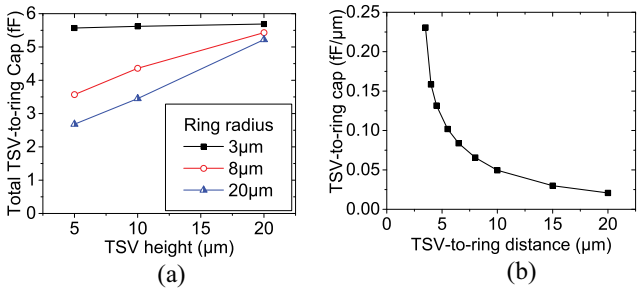

Fig. 2. TSV influence region results. (a) TSV height impact. (b) TSV-to-wire distance impact.

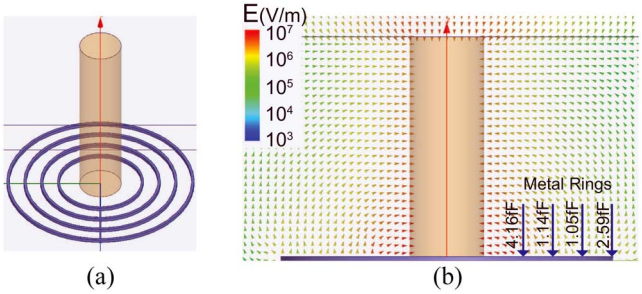

Fig. 3. Multiwire impact. (a) HFSS structure with a TSV and four rings. (b) Cross section E-field around the TSV.

directly bond the TSV pads on the bottom die to the top metal layer landing pads on the top die [23], because this technology provides much higher TSV density. Fig. 2(b) shows the coupling strength measured by the unit length capacitance, which is calculated by dividing total ring capacitance by the ring circumference. TSV-to-wire coupling is majorly within a 10 μm influence region, and wires located farther than 20 μm from the TSV show negligible coupling capacitance.

B. Multiwire Impact

The traditional empirical TSV-to-wire model considers a TSV and wire pair at one time [15] and ignores E-field sharing from other interconnect components. Though careful curve fitting can accurately model simple structures, extraction errors on a complicated structure can be large. This is because multiple wires share the E-field around the TSV. We build a structure with four metal rings in HFSS shown in Fig. 3(a), and extract their E-field interactions with the TSV. Fig. 3(b) shows the cross section E-field distribution map simulated with TSV-to-ring coupling capacitance extracted. As results shown, the strongest coupling E-field forms between the TSV and the nearest wire, and their coupling capacitance is the largest. The outer-most wire also shows large capacitance because no outside neighbor conductor shares the coupling E-field. However, for middle rings having neighbor conductors on both inner and outer sides, only small coupling capacitance is formed as a result from strong E-field sharing. As results shown, without considering E-field sharing, using a formula based on a TSV and wire pair to extract all wire capacitance results in large overestimation. It is also difficult to come up with a compact model for various complicated geometries.

TABLE I
RAPHAEL EXTRACTION RESULTS OF MULTIRING STRUCTURES

Ring count	Ring radius (μm)	Total Ring Capacitance (fF)		
		Nearest ring	Middle rings	Furthest ring
3	5~9	4.21	1.29	3.21
4	5~11	4.16	1.05~1.41	2.59
5	5~13	4.14	0.86~1.05	2.11
5	6~7.12	3.50	2.08~2.09	3.16
9	6~8.24	3.12	1.99~2.02	3.12

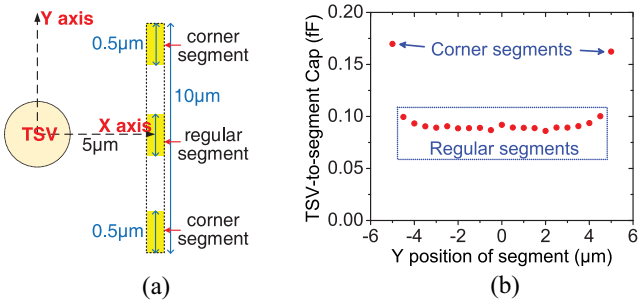

Fig. 4. Corner segment impact. (a) Simulation structure with wire segments of 0.5 μm in length. (b) Extraction results for each segment.

Another observation from the multiring structure is that if the ring pitch is small, coupling capacitance of all middle rings is close because of a similar E-field distribution in this region. When more rings are simulated (e.g., from five rings to nine rings), coupling capacitance differences are less than 5% for middle rings. Table I shows total capacitance results based on various multiring structures. Therefore, if the ring pitch is small enough, we can use fewer rings to estimate the cases with more rings and significantly reduce the library generation time. This condition is often satisfied: if many wires locate inside a TSV influence region, the wire pitch decreases which results in a similar coupling E-field for all wires. In this paper, we use up to five wires for TSV-to-wire library generation. A larger library with more wires improves accuracy at the cost of a longer library generation time.

C. Corner Segment Impact

The E-field sharing impact is observed even for a single wire. If the wire is divided into several segments, coupling E-fields are not the same for all segments. A regular segment has neighbors on both sides, while a corner segment has only one neighbor. We build a single wire structure divided into 0.5 μm segments and extract capacitance for each segment using Raphael. Fig. 4 shows an unbalanced coupling distribution between regular and corner segments. All regular ones have similar coupling capacitance, but corner segments show 80% larger capacitance to the TSV, even though they are located farther from the TSV since sidewalls of corner segments also contribute to fringe capacitance, and no outside neighbor shares the coupling E-field. Therefore, for accurate extraction, corner segments need to be handled separately. Treating corner segments as regular segments underestimates the TSV-to-wire capacitance, especially for short wires. For designs with mostly long wires, the corner segment impact is small.

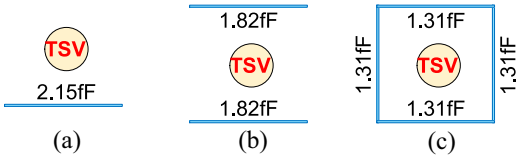

Fig. 5. Impact of wire coverage around the TSV on coupling capacitance. Raphael simulation structure of one TSV and (a) single wire. (b) Two wires. (c) Four wires.

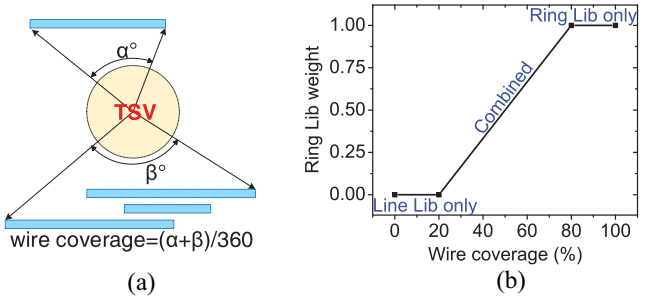

Fig. 6. Our combined method. Calculation of (a) wire coverage and (b) weighted average.

D. Wire Coverage Impact

If multiple wires surround a TSV, another E-field sharing impact is observed. As shown in Fig. 5(a), if the TSV is only facing wires on one side with little E-field sharing, total coupling capacitance for a single wire is 2.15fF. However, if the TSV is facing to wires in more directions as shown in Fig. 5(b) and (c), the single wire capacitance decreases to 1.31fF. This is because TSV-to-wire coupling is evenly distributed to all four neighbors. We use a wire coverage factor to represent how much a TSV is surrounded by wires. A wire coverage calculation example is shown in Fig. 6(a) and wire coverage factors for structures in Fig. 5(a)–(c) are 25%, 50%, and 100%, respectively. Larger wire coverage results in stronger E-field sharing and smaller capacitance per unit length. However, since more conductors are around the TSV total, TSV-to-wire capacitance increases. Therefore, for accurate TSV-to-wire capacitance extraction, the wire coverage effect needs to be considered carefully, especially when routing is congested in the full-chip design.

III. TSV-to-Wire Extraction Technique

A. Pattern Matching Technique

To handle 3-D full-chip TSV-to-wire extraction, we propose a pattern-matching technique. This technique is similar to traditional 2-D full-chip extraction tools which correlate closely with silicon measurements. But our technique accounts for every special TSV-related impact which traditional tools cannot handle. The first stage of a pattern-matching extraction is using a general extraction engine such as a field solver, to perform extraction on various predefined structures. Results are saved into a database called library. Then during extraction stage, full-chip interconnects are compared to the library and extraction results of precalculated structures closest to the layout are used for the capacitance calculation. Modern extraction engines such as Calibre xRC are able to generate a series of extraction rules based on library results. Curve-fitted equations and interpolation methods are used during structure matching to provide a more accurate estimate.

Though generating the library and extraction rules takes a long time as thousands of layout geometries need to be simulated, a common library or a set of rules can be used for certain technology on various designs. Therefore, these extraction files are provided in the process design kit by the foundry. Since only library look-up and math calculations are performed during extraction, pattern-matching extraction can extract parasitics of a large-scale circuit within minutes, and they are suitable for extraction of next generation 3-D ICs with billions of transistors and thousands of TSVs. Also, the pattern-matching method is also a promising solution for parasitic extraction of next generation monolithic 3-D ICs [24].

However, traditional pattern-matching engines can only handle 2-D designs, where interconnect coupling is limited to several neighboring wires. Vias in 2-D ICs does not have large parasitics as their sizes are small and the via coupling capacitance is often ignored by the extraction engine by default. Unlike metal vias, TSVs are hundreds of times larger and they interact with many surrounding neighbors as a result of their large influence regions. E-field sharing from multiple conductors also introduces new challenges which must be accounted for during extraction. Therefore, we focus on the special impact from TSVs and propose a first-of-its-kind 3-D extraction method. Since it is compatible with the pattern-matching-based 2-D extraction tools, our method can be easily integrated into current computer-aided design (CAD) flow and provide a smooth transition to the next generation of 3-D IC designs. Also, it can be easily parallelized and has a great potential for runtime improvement on a multicore system.

To handle all aforementioned effects, we build three special libraries for TSV-to-wire coupling extraction. Two libraries (i.e., a line library and a ring library) are used for regular segments, while a third corner library is used specifically for corner segments. These libraries enable detailed consideration of E-field sharing among wires. In our libraries, the TSV radius, TSV height, wire thickness, and wire width are used as library indexes. This enable extraction of TSVs and wires with various dimensions. To handle relative location between a TSV and a wire, the nearest TSV-to-wire distance, wire pitch, and wire location angle are included as indexes as well. To handle multiple wires, we build libraries containing various numbers of wire, and include the wire count as another library index. During extraction, wires are divided into segments and their capacitance is calculated for each segment. The geometry information of the segment and its context is used to match patterns in the library, and a linear interpolation of closest structures is used when no pattern exactly matches the segment. Our libraries contain thousands of structures covering a wide range of possible scenarios based on 45 nm technology. TSV has a height of 15 μm and a radius of 2.5 μm with a minimum placement KOZ of 0.5 μm. Wire dimensions are based on technology files.

Since Raphael does not handle the frequency-dependent silicon substrate, we use a dielectric material with a relative permittivity of 11.9 in our TSV-to-wire extraction. The silicon conductivity is ignored because the top metal layer is

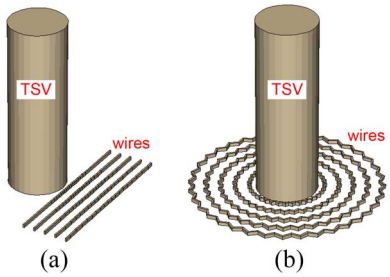

Fig. 7. Test structures for library generation. (a) Line library structure. (b) Ring library structure.

not directly connected to the substrate of the neighboring die and we assume a lightly-doped substrate on the backside. If a highly-doped substrate is used, the substrate resistance can be calculated based on the RC relationship of homogeneous materials [3]. Moreover, as shown in Fig. 1, the active regions are located near the M1 layer of the bottom die. Thus, their E-field sharing only affects the coupling capacitance between a TSV and its neighboring top metal wires on the top die. If a silicon effect-aware field solver is used to handle these properties around TSVs, it can provide more accurate extraction results. However, the semiconducting electrical properties of the silicon substrate and the E-field sharing from active layers affect TSV-to-TSV coupling capacitance. These are major E-fields inside the substrate. Therefore, the substrate resistive path and the E-field sharing in the active layers cannot be ignored in TSV-to-TSV coupling extraction [25]. Thus, in our TSV-to-TSV coupling extraction, we model the silicon depletion regions, substrate resistance, and E-field sharing from active regions to improve the accuracy.

B. Line Library

We build the line library for TSVs with low wire coverage. As shown in Fig. 7(a), the line library is built by placing straight wires on only one side of the TSV. All wires are segmented and a single structure is able to produce results for many segments with various locations. This increases extraction parallelism and reduces the library generation time. The length of each wire segment depends on its relative location to the TSV. Each segment always has a facing angle of 5° to the TSV and wire segments far from the TSV are longer. This is because that wires far from the TSV has weaker coupling and smaller capacitance per unit length. A finer grid provides more accurate results at the cost of longer runtime. Our segmenting method takes advantage of cylindrical shapes of TSVs so that capacitance of each wire segment is in a similar range to prevent accumulations of small errors. Similar to the finite element analysis, finer segmenting is used on areas where the E-field is strongest and rapidly changing while coarser segmenting is used on less critical areas. This enables a best tradeoff between the simulation time and accuracy.

The line library assumes that only one side of a TSV is surrounded by metal wires and only weak E-field sharing exists around the TSV, thus unit length capacitance of a wire is high. Therefore, this library is suitable for layouts where TSVs are covered by a few wires around. For a general case where the TSV is surrounded by wires on multiple sides, the line library gives overestimated capacitance since the line library always assumes a weak E-field sharing. In terms of the library generation time, since the line library consists of less complicated geometry structures such as straight wires, it is faster to simulate.

TABLE II
LIBRARY COMPARISON

Library	Ring	Line	Corner
Target segment	regular	regular	corner
E-field sharing	strong	weak	weak
Unit length capacitance	small	medium	large
Geometry complexity	high	low	low
Generation time	long	short	short

C. Ring Library

To handle layouts where TSVs are surround by many wires on all sides, another ring library is built. As shown in Fig. 7(b), we duplicate wire segments with various locations to form a ring around the TSV. In this structure, as the E-field of the TSV is evenly distributed in all directions, we extract the total capacitance of the ring and divide it by the total number of ring segments. We place various numbers of rings around the TSV to simulate multiple wires. As wire coverage for a ring structure is 100%, E-field sharing around the TSV is high while unit length capacitance in the ring library is small. Unlike the line library, the ring library always assumes strong E-field sharing around TSVs, thus they are suitable for designs with congested routing wires. For a general case where the TSV is surrounded by few wires, and wire coverage is low, the ring library underestimates TSV-to-wire capacitance. Thus, the ring library is complementary to the line library to provide accurate extraction for general cases. However, as the ring structure is built with many segments, the complicated geometry needs a longer extraction time for field solving.

D. Corner Library

As in previous discussions, wire segments with a single neighbor have larger coupling capacitance due to sidewall capacitance and less E-field sharing from neighbors. Therefore, based on the line library, a special corner library is built to extract corner segment capacitance at various locations. The corner library structure is similar to that of the line library. However, only capacitance of the corner segment is extracted and saved. Compared to line and ring libraries, the unit length capacitance of surrounding wires is the highest and geometry complexity for the corner library is low. However, since there are not many corner segments in the full-chip level, especially for top metal layers, its impact on system performance and noise metrics is small. However, for short wires, the extraction error is significantly reduced with corner segment effects resolved. Comparisons of all three libraries are listed in Table II.

E. Pattern Matching Algorithm

Once all libraries are built, we divide surrounding wires into segments and choose closest library structures to obtain

Algorithm 1: Pattern-Matching Extraction Algorithm

```
Input  : Ring, Line, and Corner libraries; Routed layout
Output: TSV-to-wire capacitance
foreach TSV i do
    foreach Wire j within the influence region of TSV i do
        Divide j into segments;
        foreach Segment k within the influence region of TSV i do
            d←sector index;
            Append k to list S[d];
    foreach Sector d do
        foreach Segment k inside d do
            t← nearest wire distance;
            p← average wire pitch in S[d];
            if k is a regular segment then
                LookUp(d, k, S[d], t, p) in the line library;
                LookUp(d, k, S[d], t, p) in the ring library;
                Calculate the combined value based on wire
                coverage;
            else
                LookUp(d, k, S[d], t, p) in the corner library;
Export capacitance in SPEF format;
```

TSV-to-wire coupling capacitance. We develop an algorithm shown in Algorithm 1 for pattern-matching-based TSV-to-wire coupling capacitance extraction. Extraction is performed on each TSV. Areas around the TSV is divided into 72 circular sectors, each with 5° in central angle and the same radius as the TSV influence region. These sectors are numbered clockwise. In this case, wires closer to the victim TSV have finer segments and only segments within the TSV influence region are handled. Similar to the line library structure, wires are segmented at the sector boundary and all wire segments in the same sector are gathered into a list. The wire dimension and location, number of wires, and average pitch of wires are used as indexes to search through the library. The lookup procedure takes place on each list and compares the layout structure to the pregenerated libraries. Linear interpolation is used when the library structure does not exactly match the extraction structure.

For corner segments, results from the corner library is used. For regular segments, we combine both line library and ring library based on wire coverage around the TSV. As shown in Fig. 6(b), if wire coverage is above 80%, we only use the ring library because coupling capacitance per unit length is small. On the other hand, if coverage is below 20%, we only use the line library assuming weak E-field sharing. Otherwise, results from both libraries are combined and a weighted average is calculated depending on wire coverage. This enables wire coverage consideration during full-chip extraction. After all lists are parsed, TSV-to-wire parasitics are exported into a standard parasitic exchange format (SPEF) file which can be integrated into the standard full-chip CAD flow for further timing and noise analyses.

F. Single-TSV Validation

For library comparison and verification, we perform extraction on sample layouts with two TSVs and four wires shown in Fig. 8. Table III compares our extraction results based on single-TSV libraries with Raphael results. Using the line

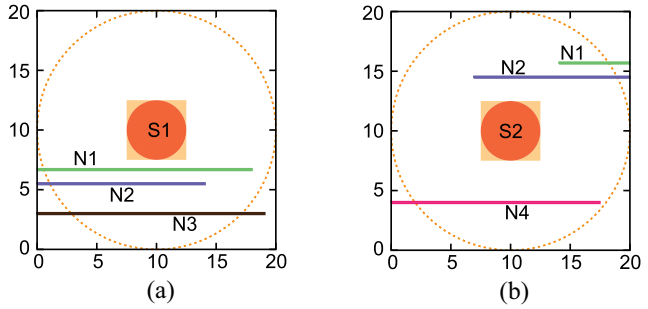

Fig. 8. Sample extraction layouts with a TSV and their surrounding wires. (a) and (b) Areas around TSV S1 and S2, respectively. Lengths are in μm.

TABLE III
SAMPLE LAYOUT EXTRACTION RESULTS BASED ON THE SINGLE-TSV LIBRARIES. CAPACITANCE IS REPORTED IN fF

TSV	Wire	Raphael	Our method		
		Single-TSV	Ring Lib	Line Lib	Combined
S1	N1	1.76	1.49 (-15%)	2.07 (+17%)	1.93 (+9.3%)
S1	N2	0.76	0.68 (-10%)	0.78 (+2.5%)	0.76 (-0.7%)
S1	N3	0.81	0.86 (+6.2%)	0.79 (-2.8%)	0.81 (-0.6%)
S2	N1	0.31	0.29 (-7.9%)	0.34 (+6.9%)	0.31 (-0.3%)
S2	N2	1.38	1.28 (-6.6%)	1.37 (-0.7%)	1.33 (-3.6%)
S2	N4	1.62	1.49 (-7.8%)	1.57 (-2.9%)	1.53 (-5.3%)

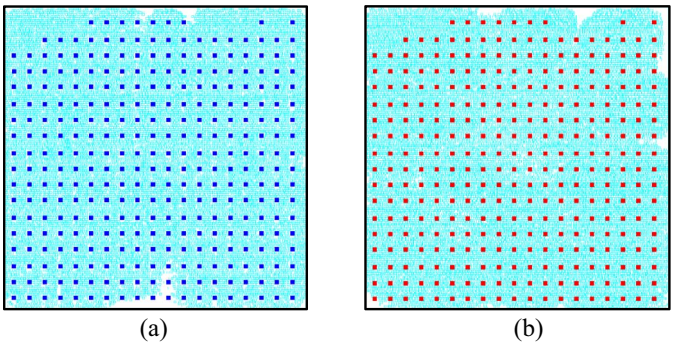

Fig. 9. Gate and TSV placement results of FFT64 design with a footprint size of 380 × 380 μm. (a) Bottom die. (b) Top die.

library is accurate when wire coverage is low, while using the ring library is accurate when wire coverage is high. But a combined method accounted for wire coverage and E-field sharing, always extracts capacitance more accurately. With single-TSV libraries, the maximum error is 0.17fF and the average error is 0.05fF.

To validate our extraction method in the full-chip level, we implement a two-die 64-point fast Fourier transform (FFT64) design and apply our method to all TSVs. The placement result of this design is shown in Fig. 9. After reading the routing results, for each TSV, we build a Raphael structure exactly as the layout around it. We set the TSV influence region as 10 μm to save Raphael simulation time and capture most coupling around the TSV. Extraction results from the field solver and our pattern-matching algorithm are compared in Fig. 10(a), where each dot represents a coupling capacitor between a TSV and a neighboring wire. The error histogram is shown in Fig. 10(b) for all extracted capacitors compared with Raphael.

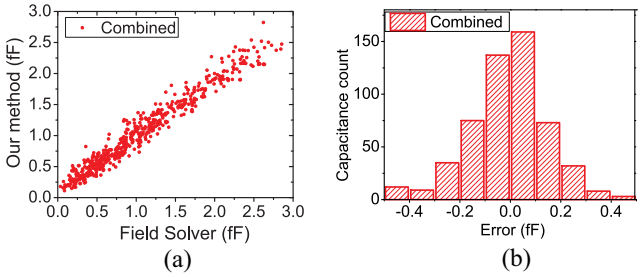

Fig. 10. Full-chip verification using combined method. (a) Extraction result comparison. (b) Error distribution.

TABLE IV
SINGLE-TSV EXTRACTION COMPARISON WITH DIFFERENT LIBRARIES, WHERE THE TOTAL CAPACITANCE FROM RAPHAEL SIMULATION IS 568fF

	Ring Lib	Line Lib	Combined
Total Cap (fF)	538	618	579
Total Cap error	-8.3%	+5.3%	-1.9%
Correlation coefficient	0.971	0.966	0.981
Average error (fF)	0.171	0.163	0.112

TABLE V
FULL-CHIP SIMULATION RUNTIME AND MEMORY SPACE COMPARISON

Extraction method	Raphael	Pattern-matching	Improvement
Runtime	7.5h	2.4s	11250x
Memory space	615MB	21MB	29.29x

Results show that our pattern-matching extraction is highly accurate in the full-chip level.

Table IV compares extraction results using different libraries. Without resolving wire coverage impact, using a single ring library gives 8.3% underestimated total capacitance, while using a single line library gives 5.3% overestimated total capacitance. However, if results from both libraries are combined, the total capacitance error is only 1.9% and the average error decreases to only 0.112fF. Compared with Raphael, which needs significant runtime and memory, our pattern-matching method achieves 11 250 times speedup and 29.29 times smaller memory space as shown in Table V. This enables it as a practical solution even for a large-scale 3-D IC with many TSVs. Therefore, we conclude that our pattern-matching method, which handles E-field sharing impact with ring, line and corner libraries, is highly fast and accurate for full-chip TSV-to-wire extraction.

IV. EXTRACTION WITH MULTI-TSV

A. E-Field Sharing With Multi-TSV

Previous studies [15], [26] are based on TSV-to-wire extraction with a single TSV. Because of fabrication yield and cost issues, TSVs are usually placed regularly where a TSV can only locate at a predefined grid point. However, modern TSV fabrication technology allows much denser TSV placement, where multiple TSVs are placed close to each other and their E-fields interact with each other. A full-chip level study has shown that ignoring multi-TSV impact results in an overestimation on TSV-to-TSV coupling [27]. Therefore, we need

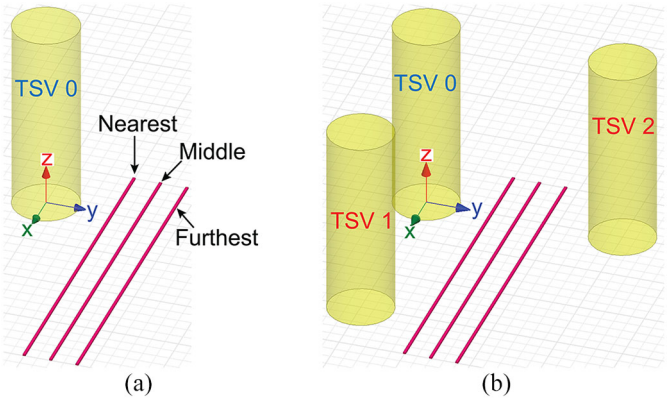

Fig. 11. HFSS structures. (a) Single-TSV. (b) Multi-TSV.

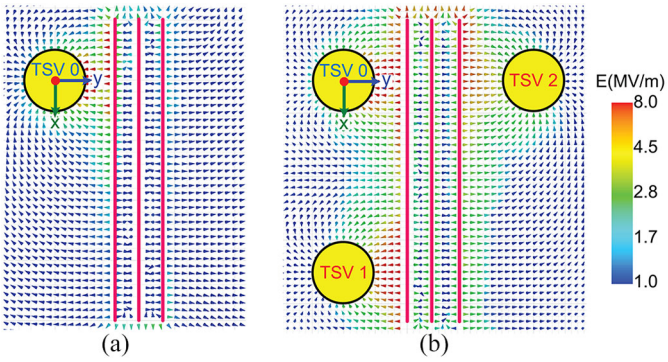

Fig. 12. *XY*-plane E-field distribution comparison. (a) Single-TSV. (b) Multi-TSV.

to handle the E-field interaction with multi-TSV for accurate TSV-to-wire extraction.

Unlike TSV-to-wire coupling, TSVs even far away from each other have non-negligible E-field interaction. As a result, even though a TSV is located beyond the TSV-to-wire influence region of another TSV, it still affects extraction results. We build a sample structure in HFSS to illustrate multi-TSV impact. The single-TSV structure is shown in Fig. 11(a), where three wires are placed around a victim TSV. The multi-TSV structure is shown in Fig. 11(b) with two nearest neighboring TSVs placed around the victim TSV. All TSVs and wires have the same dimensions as those in Section II-A with a TSV pitch of 18 μm. Since our extraction is performed on each victim TSV, the victim TSV is numbered at 0 while two neighboring TSVs are numbered at 1 and 2. The origin of the coordinate system is located at the center of TSV 0. The *XY*-plane E-field distribution comparison between single-TSV and multi-TSV, shown in Fig. 12, is based on HFSS simulations.

With the single-TSV structure, only areas where the victim TSV is close to wires have a strong coupling E-field. This results in large capacitance between the TSV and the nearest wire. Also, as there is no other neighbor conductors, all coupling fields of the furthest wire go to the victim TSV as well. With multi-TSV structure, while the E-field distribution around the victim TSV remains the same to single-TSV case, the coupling E-field changes significantly around the neighboring TSVs. The neighboring TSV not only increases the total

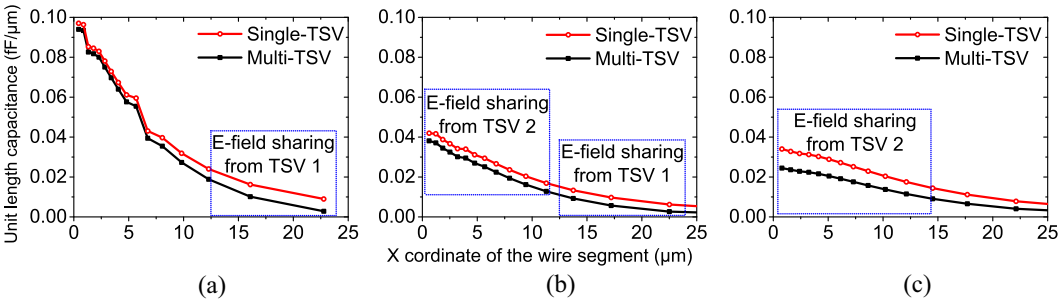

Fig. 13. Coupling capacitance extraction result of Fig. 11. (a) Nearest wire. (b) Middle wire. (c) Furthest wire.

TABLE VI
COUPLING CAPACITANCE BETWEEN VICTIM TSV TO WIRES

Target wire	Coupling capacitance (fF)		
	Single-TSV	Multi-TSV	Δ
Nearest wire	0.765	0.652	-0.113 (-14.8%)
Middle wire	0.448	0.339	-0.103 (-24.3%)
Furthest wire	0.476	0.309	-0.167 (-35.1%)

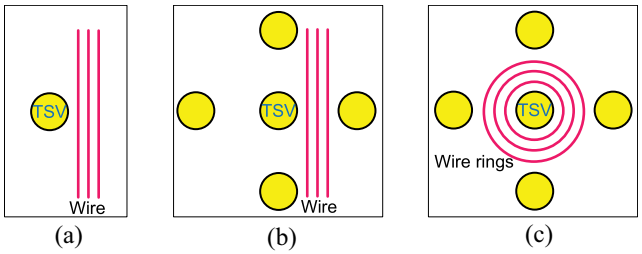

Fig. 14. Library structure comparison. (a) Single-TSV line library. Multi-TSV (b) line library and (c) ring library.

E-field strength but also alters the E-field direction around wires. E-fields from wires are heavily shared by neighboring TSVs thus the coupling between wires and the victim TSV is reduced. For the furthest wire to the victim TSV 0, where most of its coupling goes to the right neighboring TSV 2, its coupling to the victim TSV is reduced significantly. For the nearest wire, E-field sharing from the TSV 1 mostly affects areas that are beyond the influence region of the victim TSV, and the major portion of its coupling to the victim TSV remains the same. For the middle wire, its coupling to the victim TSV is also smaller compared to single-TSV model because of E-field sharing from both TSVs 1 and 2.

To study of the multi-TSV impact on parasitic components, we divide neighboring wires into small segments and perform extraction with Raphael. Fig. 13 shows the coupling distribution comparison between single-TSV and multi-TSV models and Table VI summaries extraction results. For all wires, the coupling capacitance to the victim TSV is reduced due to E-field sharing. For the nearest wire which has the largest coupling capacitance to the victim TSV, its total coupling capacitance to the victim TSV is reduced by 14.8% compared with the single-TSV model since most E-field sharing affects areas where the coupling to the victim TSV is weak. E-field sharing from both TSVs results in a 24.3% reduction for the middle wire, and a 35.1% reduction for the furthest wire. In addition, with the single-TSV model, total coupling capacitance of the furthest wire is larger than the middle wire. However, it becomes the smallest with the multi-TSV model. From victim TSV perspective, total TSV-to-wire capacitance is 1.68fF with the single-TSV model but it is only 1.30fF with the multi-TSV model. From results we conclude that, for layouts where multiple neighboring TSVs are located around, ignoring the E-field sharing from multi-TSV results in an overestimation of TSV-to-wire coupling capacitance. Therefore, for accurate TSV-to-wire coupling extraction, E-field sharing from multi-TSV needs to handled carefully.

B. Multi-TSV Libraries

To handle multi-TSV impact, we extend our patter-matching algorithm with multi-TSV structures. To avoid a long library generation time, four nearest neighboring TSVs are added into multi-TSV library structures because they have largest impact around the victim TSV and shield E-fields from further TSVs. An illustrative comparison of different library structures is shown in Fig. 14. With additional TSVs, the library construction time is increased with more conductors, but E-field interactions among TSVs are captured. All three libraries are constructed with neighboring TSVs and are used in the full-chip extraction. Compared with single-TSV libraries, coupling capacitance is smaller, especially for wire segments which are far from the victim TSV. However, since multi-TSV libraries can only handle layouts with the same TSV pitch, we build our multi-TSV libraries with a TSV pitch of 18 μm which is the same in our design layouts. This limitation is usually not a concern because most TSV technologies such as the one used in [28] require a regular TSV placement. For other technologies which allow irregular TSV placement, multi-TSV libraries with various TSV pitches are needed to provide more accurate extraction. Also, if there is only a few TSVs which are placed far away from each other, single-TSV extraction can still provide accurate results in the full-chip level.

C. Multi-TSV Validation

To verify our multi-TSV extraction algorithm, we first applied this method to sample layouts in Fig. 8. Instead of comparing our extraction results with those extracted from Raphael structures with a single TSV, we expanded the simulation window to cover influence regions of four nearest neighboring TSVs as well. Thus, the Raphael simulation captures E-field interactions from all five TSVs. Extraction results

TABLE VII
SAMPLE LAYOUT EXTRACTION RESULTS BASED ON THE MULTI-TSV LIBRARIES. CAPACITANCE IS REPORTED IN fF

TSV	Wire	Raphael Multi-TSV	Our method Ring Lib	Our method Line Lib	Our method Combined
S1	N1	1.41	1.23 (-13%)	1.61 (+14%)	1.50 (+6.1%)
S1	N2	0.57	0.50 (-12%)	0.58 (+2.3%)	0.56 (-1.9%)
S1	N3	0.49	0.48 (-1.6%)	0.49 (+1.6%)	0.49 (-0.6%)
S2	N1	0.17	0.16 (-3.0%)	0.19 (+13%)	0.18 (+4.8%)
S2	N2	1.00	0.94 (-5.5%)	1.04 (+4.6%)	0.98 (-1.2%)
S2	N4	1.03	0.97 (-6.3%)	1.08 (+4.9%)	1.01 (-1.9%)

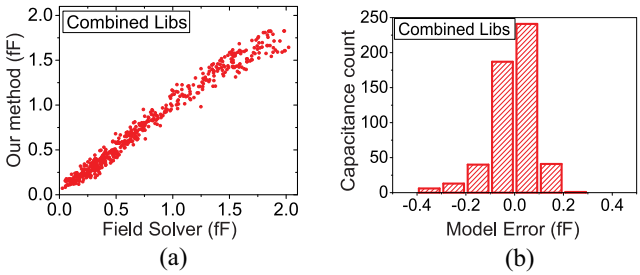

Fig. 15. Multi-TSV extraction verification. (a) Correlation comparison between our pattern-matching algorithm and Raphael simulations. (b) Error histograms of different libraries.

TABLE VIII
MULTI-TSV EXTRACTION COMPARISON WITH DIFFERENT LIBRARIES, WHERE THE TOTAL CAPACITANCE FROM RAPHAEL SIMULATION IS 423fF

	Ring Lib	Line Lib	Combined
Total Cap (fF)	386	459	419
Total Cap error	-8.7%	+8.5%	-0.9%
Correlation coefficient	0.986	0.988	0.989
Average error (fF)	0.100	0.087	0.063

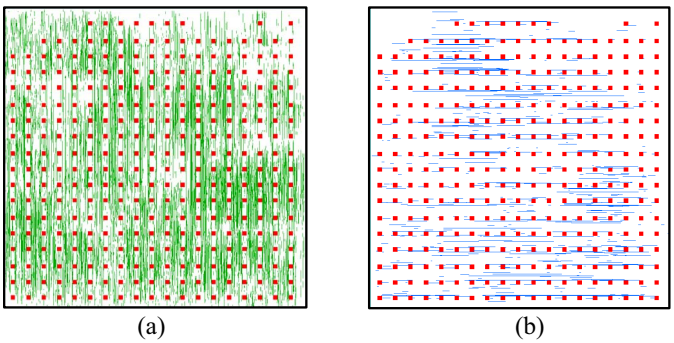

Fig. 16. Top metal routing comparison. Only top dies are shown. Design up to (a) M4 and (b) M5.

are shown in Table VII. With all E-field interactions from neighboring TSVs captured in our multi-TSV libraries, the extraction accuracy improves. The maximum error is only 0.09fF with an average error of 0.023fF. We observe that, with single-TSV extraction, coupling capacitance between TSV S1 and wire N3 is larger than that between TSV S1 and wire N2. This is because wire N3 is the furthest wire around the TSV and E-field sharing from its outside neighboring TSV is not captured. With our multi-TSV libraries, this inaccuracy is corrected and extraction results match well with Raphael simulations. Compared with single-TSV extraction, total capacitance decreases by 29.2% from 6.67fF to 4.72fF.

For full-chip verification, the same flow described in Section III-F is used. For each TSV, Raphael structures with four neighboring TSVs are used for comparison. Extraction results with multi-TSV libraries are compared with field solver extraction in Fig. 15(a), and the error histogram is shown in Fig. 15(b). Table VIII compares extraction results using different libraries. The line library still overestimates coupling capacitance, and the ring library underestimates it, but a combined method gives the most accurate results. The total capacitance error is only -0.9% and the average error is only 0.063fF. Both numbers are significantly improved compared with results using single-TSV libraries. Except for input library changes, the pattern-matching algorithm remains the same, thus the performance speedup and memory reduction are still valid for multi-TSV extraction.

V. FULL-CHIP TSV-TO-WIRE IMPACT

A. Design Specification and Analysis Flow

As a case study of TSV-to-wire coupling impact in the full-chip level, we use our FFT64 design. There are 47K gates in this design, which is partitioned into two dies. TSVs are 15 μm in height and 2.5 μm in radius with a landing pad size of 5 μm. There are 330 signal TSVs in total which connect the M1 of the bottom die with back end of line (BEOL) of the top die. TSVs are placed regularly with a pitch of 18 μm. To provide a fair comparison, we use the same 18 μm as the TSV influence region for extraction with both single-TSV and multi-TSV libraries. The supply voltage is 1.1V as in our 45 nm technology. In this paper, we focus on extraction between TSVs and the top metal layer. This is because E-fields of other metal layers are usually blocked by PDNs, and signal routings on the top metal layer.

In our technology, metal dimensions are the same from M4 to M6. Therefore, the same library can be used to handle designs with top metal layer from M4 to M6. To provide wide coverage for this paper, we implement two design variants. One uses up to M4 and the other uses up to M5, but both of them shares the same placement of gates and TSVs. The latter design has more routing resources than the other one. Thus, the router can better choose routing tracks on multiple metal layers to avoid heavy coupling between routed wires. As a result, the routing congestion on the top metal layer and the longest path delay (LPD) of the design up to M5 decrease, compared with the other design. Fig. 16 compares top metal layer routing between these designs.

We apply our pattern matching method to FFT designs for TSV-to-wire extraction. For TSV-to-TSV coupling extraction, a silicon-effect-aware multi-TSV coupling model [25] is used, and 2-D parasitics are extracted using Encounter. The same full-chip analysis flow is used where the full-chip static timing and power analysis is performed with Primetime, and the worst case noise analysis is performed with Hspice to measure TSV noise with an accurate multi-TSV model.

B. Full-Chip TSV-to-Wire Impact

Since the target of our design partition is to minimize the TSV count, and system performance is not taken

TABLE IX
FULL-CHIP IMPACT OF TSV-TO-WIRE COUPLING ON TIMING, POWER, AND NOISE. BOTH DESIGNS HAVE 4.47pF TOTAL TSV MOS CAPACITANCE AND 0.74pF TOTAL TSV-TO-TSV COUPLING CAPACITANCE

Design	FFT64 design up to M4			FFT64 design up to M5		
TSV-to-wire extraction method	none	single-TSV	multi-TSV	none	single-TSV	multi-TSV
Total TSV-to-wire capacitance (pF)	0	2.01	1.32	0	0.579	0.419
Longest path delay (ns)	4.48	5.08 (+13.4%)	4.83 (+7.81%)	4.43	4.58 (+3.39%)	4.50 (+1.58%)
Total TSV net power (mW)	0.303	0.356 (+17.6%)	0.335 (+10.6%)	0.302	0.316 (+4.64%)	0.310 (+2.65%)
Total net power (mW)	2.42	2.50 (+3.31%)	2.46 (+1.65%)	2.42	2.44 (+0.83%)	2.43 (+0.42%)
Total power (mW)	22.9	23.0 (+0.44%)	23.0 (+0.44%)	22.9	22.9 (+0%)	22.9 (+0%)
Average TSV noise (mV)	98.5	237 (+104%)	185 (+88.3%)	90.3	130 (+44.0%)	112 (+24.5%)

into consideration, critical paths of both designs are a same 3-D path. It starts from a register in the top die, goes through the bottom die by TSV89 and TSV274, and ends on another register of the top die. As a result, both TSV-related parasitics and top-metal parasitics affect full-chip timing results. We apply the pattern matching technique to both designs with both single-TSV and multi-TSV libraries. Table IX summarizes full-chip TSV-to-wire impact on timing, power, and noise. Note that the LPD change only comes from TSV nets since we assume the clock network is ideal. If a real-clock tree network is included, then the LPD is further affected since the clock signal needs to be delivered to the top die using TSVs as well, and TSV-to-wire parasitics affects the clock skew. Therefore, it also calls for fast and accurate TSV-to-wire coupling extraction for high quality clock tree synthesis.

For the design up to M4, if TSV-to-wire coupling capacitance is ignored, timing and noise analyses are inaccurate. From the result, the LPD is only 4.48 ns without TSV-to-wire coupling. This is underestimated since interconnect capacitance is not fully captured. After TSV-to-wire capacitance is annotated from the SPEF file, the LPD increases to 4.83 ns because of increased capacitance mostly on TSV89 and TSV274. Many other 3-D nets are affected by TSV-to-wire coupling as well. Even if the critical path of the original design is not a 3-D path, with TSV-to-wire coupling extracted, the critical path may change and timing impact is noticeable. Note that since 2-D routers and timing optimization engines are not aware of the TSV-to-wire capacitance, not enough buffers are inserted to TSVs and wires on the top metal layer. This results in a large delay increase after TSV-to-wire extraction is applied. Pattern-matching-based extraction is preferred in the full-chip level because it can support fast and incremental estimation for timing and routing optimization. With correct TSV-to-wire parasitic information, timing paths with large interconnect capacitance can be effectively buffered so that timing violations can be addressed.

Also, ignoring the TSV-to-wire coupling results in a significant underestimation in TSV net noise. This is because traditional 2-D extraction only extract parasitics from TSV landing pads, thus TSV coupling capacitance is heavily underestimated. Moreover, the influence region of a TSV landing pad is significantly smaller than that of a TSV. As a result, many aggressors are ignored with 2-D extraction simply because wires are too far away. Even though TSV-to-TSV coupling contributes to TSV noise significantly, its impact is large if the TSV is tall and TSVs are placed closely. Without extracting TSV-to-wire coupling, average TSV noise is underestimated. From full-chip analyses, it increases to 185 mV with multi-TSV extraction. In terms of power, though there is a large increase in TSV net power, we only observe a negligible increase in total power resulting from TSV-to-wire coupling. This is because the major portion of total power is consumed by transistors, and 3-D nets are only a small portion of all nets. Note that the FFT64 design is a small circuit, if a design has larger footprint with more TSVs and longer wirelength, the TSV-to-wire impact on the power will increase.

With shorter wirelength on the top metal layer, the FFT64 design up to M5 shows much smaller impact from TSV-to-wire coupling. Unlike the other design where the TSV-to-wire coupling capacitance is larger than TSV-to-TSV coupling capacitance, total TSV-to-wire coupling capacitance is reduced to 0.419pF with multi-TSV libraries. However, TSV-to-wire still has noticeable impact on timing as well as average TSV noise results. With less routing congestion, the design up to M5 has better performance than the other design. This provides an example of design and cost tradeoff by changing number of metal layers. With more metal layers and a higher cost, wires are less congested, parasitic components are reduced, and timing-aware routers can easily find better tracks to allocate signal wires.

As discussed in Section IV, ignoring E-field sharing among multiple TSVs and using single-TSV library overestimate TSV-to-wire coupling. By using the single-TSV library, total TSV-to-wire capacitance is 2.01pF, but it is reduced to 1.32pF using our multi-TSV libraries. This 34.3% reduction in coupling capacitance results in smaller TSV-to-wire impact on full-chip timing, power, and noise. For the design up to M5, TSV-to-wire coupling capacitance decreases by 36.0% with multi-TSV libraries as well. Therefore, for accurate TSV-to-wire coupling analyses, multi-TSV libraries are needed for full-chip analyses. If only a few TSVs are placed far away, single-TSV library can still provide accurate results.

VI. COUPLING MINIMIZATION

To alleviate TSV-to-wire coupling impact on timing and noise in the full-chip level, we propose two physical design approaches, i.e., increasing KOZ and guard ring protection. In this paper, all TSV-to-wire coupling results are based on multi-TSV extraction which accounts for four nearest neighboring TSVs.

A. Increasing Keep-Out-Zone

Since TSV-to-wire coupling is majorally between TSVs and the nearest metal layer. Therefore, a simple technique for

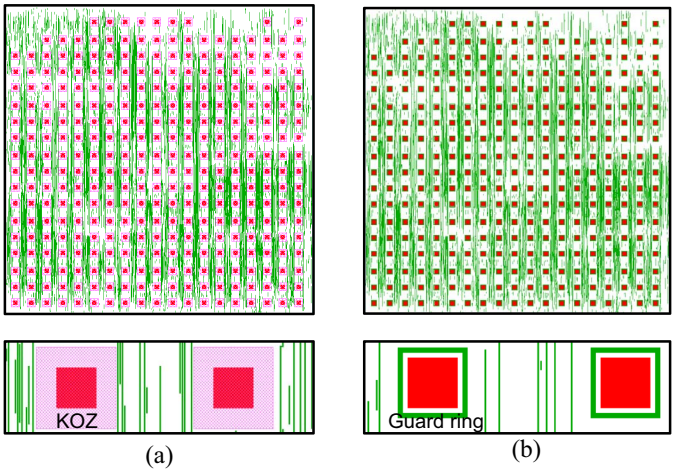

Fig. 17. Top die layout and zoom-in shots of FFT64 designs up to M4. (a) With 2.5 μm KOZ. (b) With 0.5 μm guard ring.

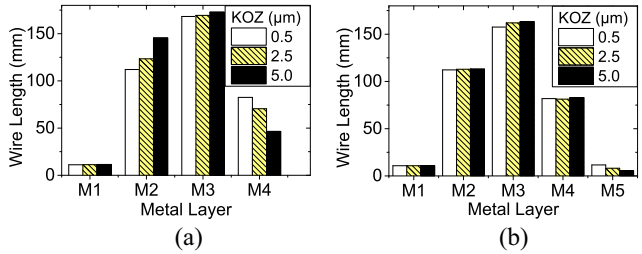

Fig. 18. KOZ impact on wire length usage. Design up to (a) M4 and (b) M5.

TSV-to-wire coupling reduction is increasing the minimum distance between the TSV and its nearest routing wire. To implement this method, we place a routing blockage on top metal layer around each TSV. This blockage region is the routing KOZ. To study impact of various KOZ sizes, we implement two designs with KOZ sizes of 2.5 and 5 μm, respectively. Fig. 17(a) shows design layouts with KOZs. The original design has KOZs of 0.5 μm. With a larger KOZ, capacitance between a TSV and its nearest wire further decreases because of a weaker coupling E-field. In addition, a larger KOZ reduces routing resources available on the top metal layer. This results in a reduction in the top metal layer wirelength and the number of aggressors around the TSV. Note that increasing the routing KOZ does not have any silicon area overhead. Therefore, the placement is the same as the original design placement, and only incremental routing is performed to correct any routing violations. Thus, layouts have minimum changes, and it is a fair comparison among all designs.

However, one drawback for increasing the KOZ is that we observe heavier routing congestion on other layer as a result of the reduced number of routing tracks on the top metal layer. Potentially, this may result in a degradation of design quality and a increase in coupling noise between 2-D wires. Fig. 18 compares wirelength distribution with different KOZ sizes. For the FFT64 design up to M4, since top metal wires are reduced by 43.7% with 5 μm KOZs, wire congestion on other metal layers is more severe. Wirelength on M2 increases by 29.9% and total wirelength increases from 373.9 to 376.3 mm.

TABLE X
KOZ IMPACT ON FFT64 DESIGN UP TO M4

KOZ size (μm)	0.5	2.5	5
M4 wirelength (mm)	82.5	70.5 (-14.5%)	46.5 (-43.6%)
Total wirelength (mm)	374	375 (+0.19%)	376 (+0.64%)
Longest path delay (ns)	4.83	4.77 (-1.2%)	4.64 (-3.9%)
Total TSV net power (mW)	0.335	0.326 (-2.7%)	0.316 (-5.7%)
Total net power (mW)	2.46	2.45 (-0.4%)	2.43 (-1.2%)
Average TSV noise (mV)	185	165 (-11.1%)	139 (-25.0%)

On the contrary, since the design up to M5 has enough routing resources and its top metal wirelength is small, increasing the KOZ only has slight impact. Therefore, for some designs which have limited routing resources, increasing the KOZ size may not be beneficial because of increased routing congestion.

We perform the full-chip analysis on designs with routing KOZs, and results are summarized in Table X. Since the placement is the same, TSV-to-TSV coupling elements are unchanged. With larger KOZs, top metal layer wirelength is reduced, and their coupling capacitance is reduced. Therefore, TSV-to-wire coupling also shows smaller impact on full-chip timing and noise. Compared with the original design, the LPD decreases by 1.2% and 3.9% for 2.5 and 5 μm KOZs, respectively. In terms of signal integrity, a larger KOZ also lowers the TSV net noise by reducing the aggressor count and TSV-to-wire coupling capacitance. The average worst-case noise on TSV nets can be reduced by 11.1% and 25.1% for 2.5 and 5 μm KOZs, respectively. On the other hand, KOZ impact on the full-chip power result is much smaller since TSV-to-wire capacitance decreases but wire-to-wire capacitance increases on other layers. Overall, we conclude that increase top metal layer KOZ is effective in reducing TSV-to-wire coupling at the cost of higher routing congestion.

B. Guard Ring Protection

Another way to protect the victim TSV is to provide E-field shielding using grounded conductors around TSVs. Similar technologies are widely used to increase the SNR in communication applications. In this paper, we propose a physical design optimization technique specifically designed to reduce TSV-to-wire coupling. Unlike the previous work where grounded guard rings in active layer are added around TSV [5], [25], grounded wire guard rings on the top metal layer are inserted around TSV. Therefore, there is no overhead on silicon areas and standard fabrication technology is used. However, the guard ring consumes some routing tracks on the top metal layer and needs additional routing to connect the ring to the ground. The grounded guard ring shields some E-fields around TSV, and introduces a ground capacitor to the TSV net. As a result, there are small delay and power overheads on TSV nets, but it reduces TSV coupling noise. Moreover, the guard ring now becomes the nearest wire around the TSV, thus all other wires have neighbors on both sides. Therefore, coupling capacitance between the victim TSV and signal wires is reduced and the TSV is better shielded with coupling noise.

To model guard ring impact, we build a guard ring model shown in Fig. 19(a), where C_{TW}, C_{TG}, and C_{WG} represent TSV-to-wire, TSV-to-ring, and wire-to-ring capacitance,

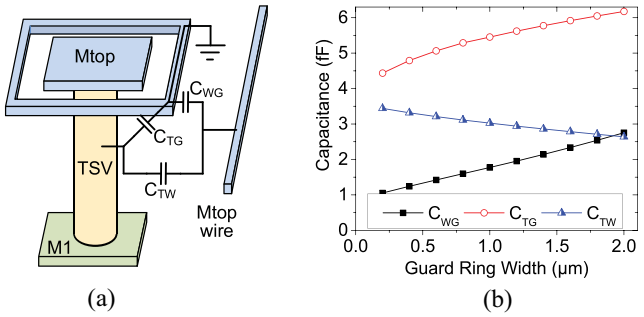

Fig. 19. Guard ring capacitance model. (a) Simulated structure. (b) Raphael extraction result.

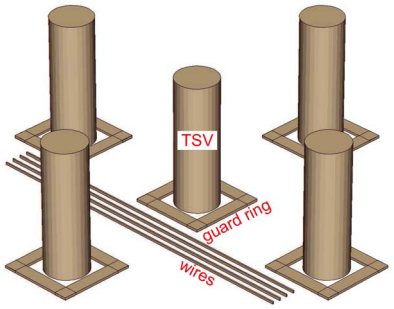

Fig. 20. Sample multi-TSV line library structure with 1.5 μm guard ring.

respectively. The ring is assumed to connect with ground ideally, and a 10 μm long wire on M4 is located 8 μm far from the center of the TSV. We perform Raphael simulations on guard ring structures with various guard ring widths, and results are shown in Fig. 19(b). With a wider guard ring, the TSV is better shielded from TSV-to-wire coupling, thus TSV-to-wire coupling capacitance is smaller. However, a wider guard ring increases ground capacitance on both TSV and wire, which leads to small delay and power increases. Therefore, it is better to protect TSVs which are not located on the critical path so that additional ground capacitance has no impact on design performance. In this paper, we insert wire guard rings to every TSV so that we can observe performance impact from guard rings.

To study full-chip impact of wire guard rings, we build three libraries with multishielded TSVs, i.e., line library, ring library, and corner library, in which TSVs are surrounded by grounded guard rings. To study the guard ring width impact, libraries are built with both 0.5 and 1.5 μm guard rings. Fig. 20 shows a sample structure from the line library, where each TSV is surrounded by a 1.5 μm guard ring. In addition, we implement FFT64 designs with 0.5 and 1.5 μm guard rings on the top metal layer. Fig. 17(b) shows die layouts with guard rings. These two designs are based on our previous FFT64 design with 2.5 μm KOZs. We insert the guard ring into the KOZ so that placement and signal routing are kept the same. Similarly to KOZ insertion, guard rings also consume routing resources on the top metal layer. However, they provide better protections to TSVs.

We perform TSV-to-wire extraction using these libraries with multishielded TSVs and full-chip analysis results are summarized in Table XI for the design up to M4. Compared with the original design, the LPD increases

TABLE XI
GUARD RING IMPACT ON FULL-CHIP DESIGNS

Guard ring width (μm)	0	0.5	1.5
KOZ size (μm)	0.5	2.5	2.5
Longest path delay (ns)	4.83	4.84 (+0.21%)	4.90 (+1.45%)
Total TSV net power (mW)	0.335	0.340 (+1.49%)	0.349 (+4.18%)
Total net power (mW)	2.46	2.46 (+0%)	2.47 (+0.41%)
Average TSV noise (V)	185	146 (-21.4%)	138 (-25.6%)

by 0.21% and 1.45% for designs with 0.5 and 1.5 μm guard rings, respectively. This impact comes from two aspects. Ground capacitance on TSV nets increases but TSV-to-wire capacitance decreases. If they are compared with the design with 2.5 μm KOZs, delay overheads from larger ground capacitance are shown clearly. The LPD increases 1.4% and 2.7% for designs with 0.5 and 1.5 μm guard rings, respectively. Total capacitance on TSV nets always increases with wider guard rings since E-fields around TSVs are stronger, and we observe a slight timing overhead from increased capacitance. Guard ring impact on power is negligible, since TSV MOS capacitance is the major load on TSV nets and it is not changed. From results, we find that the ground guard ring is very effective in TSV net noise reduction. Compared with the design with 2.5 μm KOZs, the average TSV net noise decreases by 11.6% and 16.4% with 0.5 and 1.5 μm guard ring, respectively. Compared to the original design, the average TSV net noise decreases by 21.4% and 25.6% with 0.5 and 1.5 μm guard ring, respectively. Meanwhile, for the design up to M5, we only observe a noticeable noise reduction and there is a negligible timing and power overhead, since TSV-to-wire coupling is much weaker on this design. Overall, we conclude from our full-chip results that both increasing KOZ and inserting guard rings are very effective for TSV-to-wire coupling noise reduction with minimum overheads on design qualities.

VII. CONCLUSION

In this paper, we studied various factors affecting the TSV influence region and TSV-to-wire coupling capacitance. For fast and accurate full-chip TSV-to-wire capacitance extraction, we built three libraries based on multi-TSV structures. We proposed a pattern-matching algorithm which accounted for various E-field sharing impact, i.e., multiple wire impact, corner segment impact, wire coverage impact, and multi-TSV impact. We verified our method using a two-die 3-D FFT64 design against field solver simulations in the full-chip level. We also studied multi-TSV impact on TSV-to-wire coupling. Results showed that ignoring E-field sharing and using a single-TSV model on multiple TSVs lead to an overestimation on coupling capacitance. Applying our pattern-matching algorithm, we studied full-chip TSV-to-wire impact on timing, power, and noise. Increasing metal layer usage reduced impact of both top metal layer signal routing and TSV-to-wire coupling. Analysis results showed that TSV-to-wire coupling was none-negligible and had large impact on full-chip delay and TSV net noise. To alleviate TSV-to-wire coupling, we proposed two physical design solutions, i.e., increasing the KOZ around TSV in top routing layer and adding a ground guard ring. We showed that both methods were very effective in TSV net noise reduction with small overheads on design qualities.

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