Physical Design and CAD Tools for 3-D Integrated Circuits: Challenges and Opportunities

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Editor's notes:
Three-dimensional integration is a breakthrough technology that provides numerous benefits such as better performance, lower power consumption, and wide bandwidth by vertical interconnects and 3-D stacking. This paper presents an overview regarding the physical design and CAD tools suitable for 3-D integrated circuits.
—Partha Pratim Pande, Washington State University

■ **NOT ONLY CONTINUING** Moore's law but also ever-increasing needs for high-performance and low-power integrated circuits (ICs) and systems have been leading researchers to explore various technological options such as multigate transistors, vertical transistors, carbon nanotube field-effect transistors, optical interconnects, on-chip wireless interconnects, and extreme ultraviolet lithography. One of the promising breakthrough technologies is 3-D integration, which is expected to provide numerous benefits in almost all aspects such as chip area, wirelength, performance, power consumption, intermodule bandwidth, device density, and heterogeneous integration [1]–[5]. Three-dimensional integration (including 2.5-D integration) is placing and packaging in a single chip multiple device layers that should otherwise be packaged in

each chip, mounted on a printed circuit board (PCB), and routed through PCB traces. As shown in Figure 1, the concept of 3-D integration is simple and 3-D integration is expected to provide numerous benefits as mentioned above, so 3-D integration has been actively researched in academia and industry for more than ten years.

As of the beginning of 2015, however, commercial products using 3-D integration are very few [6], [7]. A potentially representative application exploiting the benefits that 3-D integration provides is the so-called 3-D-stacked DRAM such as wide input/output (I/O), wide I/O 2, hybrid memory cube, and high bandwidth memory [8], [9]. These memory technologies achieve high integration density by stacking multiple memory layers in a single package and high memory bandwidth by vertical interconnects much smaller than the PCB trace. Another application is the 3-D-stacked CMOS image sensor in which pixel arrays are placed in a die, logic is placed in another die, and the two dies are stacked vertically [2], [10]. Three-dimensional-stacked CMOS image sensors have smaller form factor than 2-D CMOS image sensors and could be cheaper due to heterogeneous integration because one of the dies can be fabricated using a cheap technology if it does not require any expensive technology. Two-and-a-half-dimensional field-programmable gate array (FPGA) is also a good application as is shown in a commercial chip [7]. Although various applications

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have been suggested in academia and industry, these are the only representative applications realizable in the very near future.

The delay of adoption of 3-D integration in the mainstream semiconductor market might be due to various reasons such as the lack of applications, limitations that 3-D integration inherently has (such as higher heat density), and the lack of standards and computer-aided design (CAD) tools supporting 3-D integrated circuits and systems. In this paper, we review four different 3-D integration technologies: 2.5-D integration, through silicon via (TSV) based, inductive coupling based, and monolithic 3-D integration. Then, we discuss challenges to overcome for adoption of 3-D integration in the mainstream semiconductor market. We also present uncharted design and optimization problems to solve for the design of 3-D ICs.

Three-dimensional integration technology

In this section, we review and discuss four 3-D integration technologies (2.5-D, TSV-based 3-D,
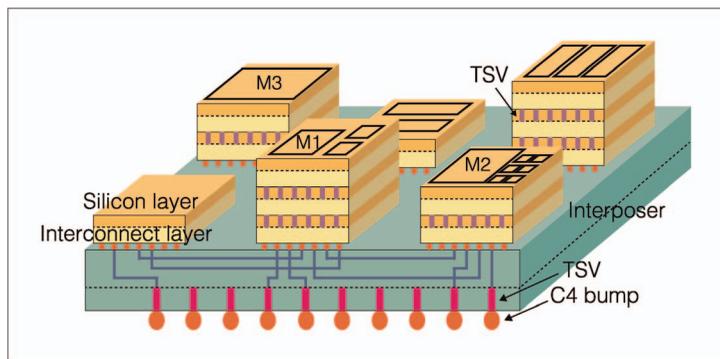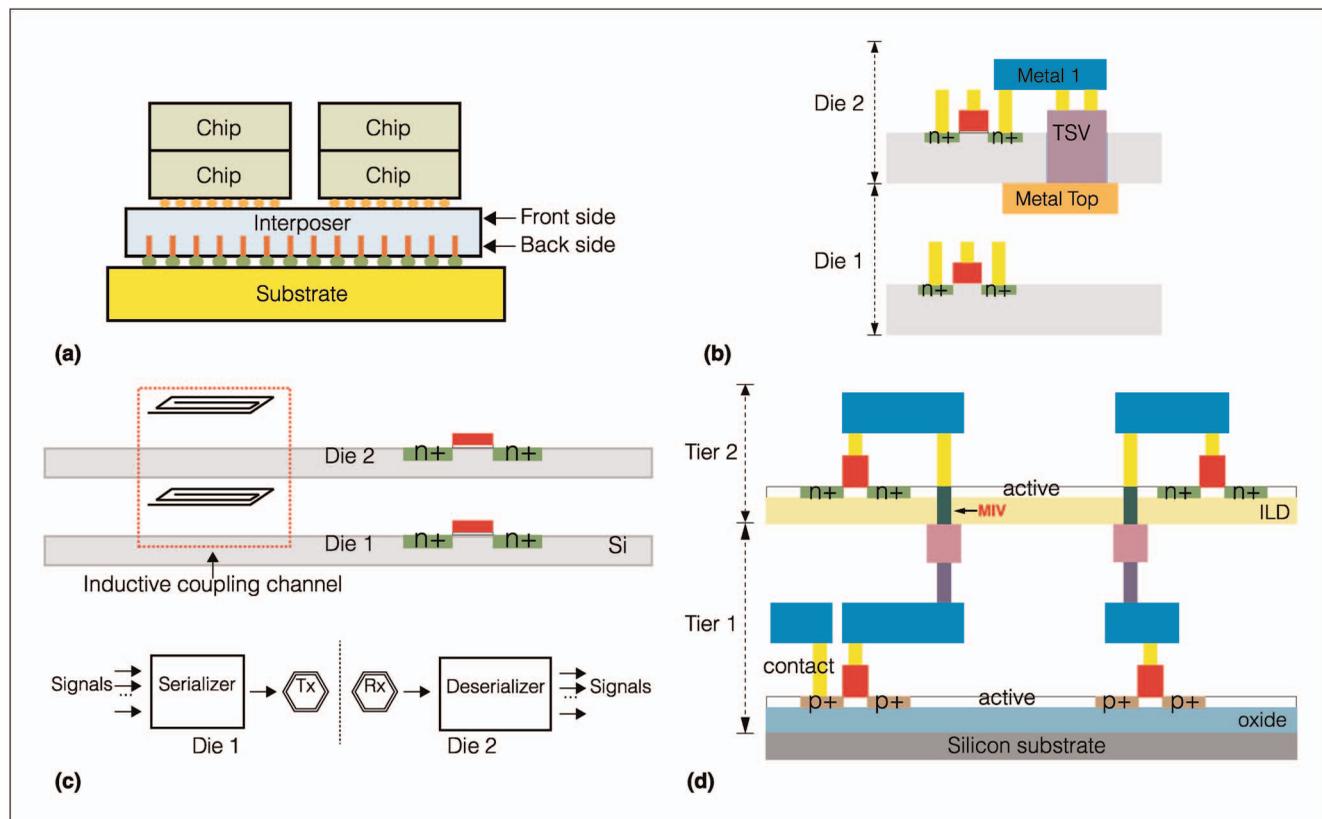

Figure 1. Two-and-a-half-dimensional integration.

inductive-coupling-based 3-D, and monolithic 3-D) shown in Figure 2.

Two-and-a-half-dimensional integration

In silicon interposer-based 3-D integration (namely 2.5-D integration), multiple chips are mounted on a silicon interposer and communicate through interposer routing as shown in Figures 1 and 2a. Through silicon vias (TSVs) are fabricated inside the silicon

Figure 2. Four representative 3-D integration technologies: (a) 2.5-D; (b) TSV-based 3-D; (c) inductive coupling-based 3-D; and (d) monolithic 3-D.

interposer to connect the interposer routing in the front side and C4 bumps in the backside of the interposer [11], [12]. Two-and-a-half-dimensional integration achieves smaller form factor than 2-D ICs by mounting multiple dies on a silicon interposer and packaging them instead of packaging each of them and mounting them on a PCB. Since interposer routing is smaller than PCB routing, 2.5-D integration enables shorter interchip communication distance leading to shorter delay and lower power consumption than connecting 2-D ICs on a PCB. Xilinx Virtex-7 2000T is a commercial product integrating four FPGA chips in a single package using 2.5-D integration technology [7]. In addition, 2.5-D integration has an advantage in yield because it is possible in 2.5-D integration to build many small dies and connect them in the interposer.

Although the initial concept of 2.5-D integration was mounting 2-D ICs on an interposer, mounting 3-D ICs is also possible, as shown in Figure 1. An advantage of mounting 3-D ICs on an interposer instead of stacking them in a single 3-D IC is in the better heat dissipation capacity of the 2.5-D integration. As seen in Figure 2, 2.5-D integration has larger surface area than other types of 3-D ICs, so it has larger contact area to a heat sink at the cost of larger form factor (or footprint area). In addition, each chip can be tested before it is mounted on the silicon interposer, so only good dies can be mounted and the total yield can go up.

TSV-based 3-D integration

TSVs are conductors fabricated in the silicon layer, as shown in Figure 2b. TSVs are used to connect the metal layers above and below the TSVs so that the transistors in the stacked dies can communicate through them. TSV fabrication processes are compatible with modern CMOS processes as presented in many papers. Especially, TSVs can be fabricated before front-end-of-line (FEOL), between FEOL and back-end-of-line (BEOL), or after BEOL depending on the manufacturing process. Conductor such as copper, tungsten, and polysilicon is used for TSVs and barrier and liner layers surrounding the TSVs are also created. A side of a TSV is connected to the metal 1 layer (or a higher metal layer depending on the technology) in the same die and the other side is connected to a microbump and/or a backside metal layer for 3-D connections, as shown in Figure 2b.

As of 2015, typical size (width or diameter) of a TSV is 1–5 μm [4], [13]. Therefore, using TSVs for interdie communication enables very high bandwidth between dies, which is actively exploited in some applications such as wide I/O memory. In addition, TSV-based 3-D integration provides higher volume density than 2.5-D integration, thereby enabling potentially better performance and/or lower power consumption. Due to its structural simplicity, CMOS process compatibility, and the numerous benefits predicted or shown in various works, TSV-based 3-D integration has been actively researched and various TSV manufacturing processes, analysis results, and design and optimization algorithms have been proposed for TSV-based 3-D ICs.

A constraint imposed on TSV locations in the design of 3-D ICs is that a TSV has keep-out zone (KOZ) within which transistors or other TSVs cannot be placed. When TSVs are fabricated, different thermal expansion coefficients of the TSV material and silicon induce tensile stress around the TSVs, which could lead to crack or damage. The mechanical stress also leads to carrier mobility variation in the transistors placed around TSVs. KOZ protects TSVs and surrounding silicon from crack and damage due to tensile stress, and transistors around TSVs from mobility variation [14]–[18].

Inductive coupling

Wireless (or contactless) 3-D integration uses capacitive or inductive coupling for interdie communication, as shown in Figure 2c [19], [20]. Inductive coupling shows many advantages over capacitive coupling because the communication distance of capacitive coupling is limited to a very short range whereas that of inductive coupling is much longer [21]. The inductors in inductive coupling channels are implemented in the metal layers of each die, so fabrication of the inductors for inductive coupling channels does not require any special or additional processes. In addition, increasing the transmission power or upsizing the inductors can increase the transmission gain, which easily enables longer communication distance. In addition, data rate of a single inductive coupling channel is much higher than that of a single TSV channel (e.g., 32 versus 1 Gb/s), so each inductive coupling channel can utilize serializers in its transmitter and deserializers in its receiver to transmit a set of signals [21], [22].

Three-dimensional integration based on inductive coupling provides a few advantages over TSV-based or monolithic 3-D integration. Above all, inductive coupling naturally enables heterogeneous 3-D integration. In detail, the inductive coupling channels do not require any additional circuits for interdie communication, so multiple dies operating under different supply voltage values can naturally communicate with each other through the channels. However, interdie communication in TSV-based 3-D ICs requires level shifters in the same situation, which restricts the applicability of TSV-based 3-D ICs to heterogeneous 3-D integration. Since inductive coupling channels are free from voltage level conversion, they provide much higher flexibility in the design of heterogeneous 3-D ICs and systems.

Inductive coupling channels also naturally coexist with microfluidic channels, which are considered a very promising cooling solution for 3-D ICs, because inductors and microfluidic channels are implemented in metal layers and silicon layers, respectively. Therefore, microfluidic channels in the inductive-coupling-based 3-D ICs are much easier to design and can effectively spread heat. On the other hand, TSVs and microfluidic channels interfere with each other because both of them are fabricated in the same silicon layer. Thus, design of 3-D ICs with microfluidic channels and TSVs requires sophisticated CAD algorithms to find optimal locations of TSVs and microfluidic channels without sacrificing performance and power consumption.

Monolithic 3-D integration

Monolithic 3-D integration stacks multiple, very thin silicon layers, so it is expected to provide the most fine-grained 3-D integration, as shown in Figure 2d. Monolithic 3-D ICs can be built by various methods. A way of stacking multiple thin layers is to fabricate a bottom layer and deposit a new silicon layer on top of the bottom layer. For example, Shen et al., [23] use amorphous silicon (a-Si) deposition, green nanosecond laser spike annealing (GN–LSA) crystallization, and low-temperature thinning to form a new silicon layer (so, this method is actually not stacking the layers but fabricating the layers sequentially). On the other hand, two separate layers can be fabricated separately and stacked and one of them can be thinned. For instance, monolithic 3-D RCAT flow by monolithic IC3D [24] stacks the second layer onto the first (base) layer and cuts the thick body of the second layer out

by ion-cut cleave, which is followed by gate formation and metallization. In any case, the additional layers are very thin (100–200 nm), so the vertical height of interlayer vias is very short. Therefore, the parasitic resistance and capacitance of an interlayer via are almost negligible. The negligible parasitic resistance and capacitance (RC) and the very tiny size of the monolithic interlayer vias (MIVs) enable the most fine-grained 3-D integration, potentially the largest amount of performance improvement and power reduction, and the smallest form factor.

Challenges and opportunities

Although a huge amount of research effort has been put on design and test methodologies, optimization algorithms, modeling, and analysis for 3-D ICs, there are still fundamental challenges and new issues to resolve for adoption of 3-D ICs in the mainstream semiconductor market. In this section, we discuss challenges and issues in 3-D integration.

Applications

Three-dimensional integration has disadvantages such as higher heat density, more difficult testability, and more expensive manufacturing cost, so the amount of benefits that each application obtains from 3-D integration should be sufficiently large. As of 2015, however, applications that can fully exploit the benefits that 3-D integration provides are very limited, so finding more killer applications for 3-D integration is one of the most important and challenging works for successful commercialization of the 3-D integration technologies.

Bandwidth. The 3-D-stacked memory benefits from very wide memory bandwidth are enabled by very small interlayer vias [4], [25]–[27]. For instance, the numbers of signal interlayer vias in [25], [26], and [4] are 821, 32 768, and 7424, respectively. In the same way, integrating multiple chips into a single 3-D IC can replace PCB traces connecting the chips by interlayer vias, thereby achieving very high die-to-die (chip-to-chip) bandwidth. However, "What applications require the very high bandwidth?" is still an open question. The wide I/O is a good example, but just one application is not enough for commercialization. A potential application in this area is integrating many cores (e.g., network-on-chip) in a single 3-D IC [4], [28], otherwise a subset of the cores should be packaged in each chip and the chips should be

connected on a PCB, which would have much lower performance than the 3-D IC. In addition, if too many intercore connections are required, the system may not be physically realizable. Thus, 3-D integration would be the only realizable technology for those applications.

Power consumption. To achieve significant power consumption by 3-D integration, several open questions should be answered, such as the following.

1) What chips should be stacked to benefit from I/O power reduction?
2) What chips should be redesigned in 3-D to reduce power by wirelength reduction and shortened clock tree?
3) How can we develop CAD algorithms to reduce wirelength?

Driving PCB traces consumes a huge amount of power for their large capacitance, but stacking multiple chips in a 3-D IC and communicating through low-parasitic interlayer vias can significantly reduce the I/O power consumption. The 3-D-stacked memory is a good example. In [4], the whole chip composed of cores and memories consumes approximately 3.8 W. However, if the core and memory dies are packaged separately and connected through PCB traces, the power consumption only for I/O would be approximately 4.0 W, assuming all the signal I/O pads (in total, 7424 interdie signals) in both the core and memory chips switch every clock cycle, and the total power would be approximately 8 W, which is twice the power consumption of the 3-D chip. Therefore, the 3-D-stacked memory significantly reduces power consumption by replacing PCB traces and I/O cells by interlayer vias. Similarly, Xilinx showed that integrating four FPGA chips in a single package reduced power consumption from 112 to 19 W [7].

Another way to reduce power consumption is to redesign a 2-D IC in 3-D. Redesigning a chip in 3-D can shorten the logic and clock wires and remove some buffers, thereby reducing dynamic power consumption [29], [30]. However, the amount of power reduction shown in the papers is not sufficiently large for commercialization. For instance, the interconnect power of modern VLSI chips occupies 20%–30% of the total power consumption [30], [31]. Assuming the interconnect power is 30% of the total

power consumption and the interconnect power is proportional to the interconnect length for simple approximation, shortening the total interconnect length by 30% and 50% reduces the total power consumption by 9% and 15%, respectively. In reality, Thorolfsson et al., [29] reduced the total wire length by 56.9%, but the total power reduced only by 4.4% by 3-D integration using 180-nm technology and 2.5-μm-diameter TSVs. Panth et al., [30] reduced the total interconnect length by 20% and achieved 15.57% total power reduction by monolithic 3-D integration at 28 nm. In the latter, all the cell power, net power, and leakage power reduced and contributed to the total power reduction.

Stacking more dies in a single 3-D IC is another way to shorten signal and clock wires, thereby reducing dynamic power consumption. In [32], for example, the wirelength of a specific benchmark is minimized when it is designed in five dies. Therefore, more noticeable power reduction could be achieved by stacking more dies [3]. However, stacking more dies generally requires insertion of more interlayer vias. Thus, if the parasitic RC of interlayer vias are not negligible or inserting more interlayer vias causes serious area overhead (e.g., inductors for inductive coupling), stacking more dies might not reduce dynamic power consumption sufficiently.

Form factor. The 3-D-stacked CMOS image sensor places image sensors on a die and processing logic on another die and stacks them in 3-D, thereby achieving smaller form factor than the traditional 2-D CMOS image sensor [33], [34]. For instance, Suntharalingam et al., [33] stack seven layers consisting of two 3-D image layers and five supporting layers, and Lee et al., [34] stack three layers consisting of an image sensor layer and two supporting layers, thereby reducing the form factor significantly. A common feature found in these works is that the stacked layers are highly independently modularized. The two main supporting layers in [33] are the master and slave analog–digital converter (ADC)/ control layers. Similarly, the two layers under the image sensor layer in [34] are the correlated double sampling and ADC layers. Since the systems are easily partitionable and the number of interlayer connections is not many (in total, 336 in [33]), the 3-D-stacked CMOS image sensor is a good example for achieving smaller form factor by 3-D integration. However, just an application is not enough for

successful commercialization of 3-D integration and "What applications are easily partitionable into balanced area?" is still an open question.

A potential application in this area is splitting a multicore chip into multiple core and memory layers and stacking them as shown in [4] and [35] as long as the number of connections among them is not many. This application is easily partitionable because the cores and the memory blocks are independently modularized. The simple connectivity plays an important role in the physical design step because it enables manual physical design (partitioning and placement of the partitioned modules and interlayer vias). If the connectivity is complex, however, CAD tools would be required to automatically place the submodules and interlayer vias.

Performance. Performance benefits can be obtained in several ways. For instance, the wide I/O improves performance by loading a large memory block in a short period using the wide memory bandwidth. In this case, the direct benefit of 3-D integration is achieving the wide bandwidth between dies, but the ultimate benefit is the performance improvement [26]. On the other hand, Saito et al., [25] achieve 43% latency reduction by reorganizing memory elements, which leads to performance improvement of the system. Performance improvement can also be obtained by redesigning 2-D ICs in 3-D. Thorolfsson et al., [29] achieved 19.7% critical path delay reduction, and Kim et al., [32] also achieved 20%–50% critical path delay reduction by redesigning in two layers. Lee et al., [36] showed that monolithic 3-D ICs achieved even better timing than TSV-based 3-D ICs. Redesigning 2-D ICs in 3-D reduces the footprint area, so the total wirelength goes down and the critical path delay is improved. Thus, it achieves both smaller form factor and performance improvement.

However, "What chips can be redesigned in 3-D to maximize performance?" and "How can we improve performance?" are still open questions. Performance could be improved by: 1) increased operation frequency achieved by reducing critical path delay; 2) increased throughput achieved by increasing communication bandwidth and integrating more processing elements; and 3) improved architectures enabled by 3-D integration [37]. Unfortunately, improving performance by 3-D integration in many cases requires very effective and efficient CAD algorithms, which are not mature yet. We will discuss CAD tools for 3-D integration in the CAD tools section.

Thermal issues

Three-dimensional ICs have higher device density than 2-D ICs, so heat dissipation per unit volume is higher than that of 2-D ICs. In addition, dies seating in the middle of a 3-D IC have longer heat path to the top and bottom heat sinks and higher heat coupling with neighboring dies than the dies on the boundary close to the heat sinks. This heat dissipation and thermal coupling problem is translated into the increase of the maximum and average temperature, so 3-D ICs are more vulnerable to thermal problems than 2-D ICs, which is a major bottleneck for adoption of 3-D ICs.

Two-and-a-half-dimensional integration of 2-D ICs has the lowest heat coupling compared to the other 3-D integration methodologies because heat dissipation per unit surface area does not increase. However, lateral heat coupling exists among the integrated 2-D dies in 2.5-D integration. Temperature in 2.5-D integration highly depends on the interposer material, as shown in [38], but the other 3-D integration technologies have more serious thermal issues than 2.5-D integration. Heat coupling in TSV- and inductive-coupling-based 3-D integration significantly increases the temperature. In addition, monolithic 3-D integration has the highest device density per volume among all the 3-D integration technologies. Assuming all the transistors in different tiers have the same characteristics [39], heat coupling in two-tier and three-tier monolithic 3-D ICs have approximately 10 °C and 25 °C higher maximum temperature than 2-D ICs, respectively [40].

To reduce the temperature and distribute heat effectively, various cooling and optimization methodologies have been proposed. One of the most effective cooling techniques is the microfluidic cooling (MFC). MFC inserts microfluidic channels carrying cooling fluid into the silicon bulk so that the silicon substrate is cooled down by the cooling fluid. However, microfluidic channels are inserted into the silicon bulk, so they overlap with TSVs. Due to this, the design of TSV-based 3-D ICs with MFC requires sophisticated design and optimization algorithms [41], [42]. On the other hand, inductive links and silicon bulk do not overlap in inductive-coupling-based 3-D ICs.

Various design-level optimization algorithms have also been proposed to resolve the heat problem.

Via planning such as thermal via insertion and TSV alignment spreads heat more effectively just by increasing the heat conductivity of the whole 3-D chip [43]–[45]. Optimization of cell locations during placement can also reduce temperature [46], [47].

CAD tools

Physical design of 3-D ICs requires new tools for design, analysis, and optimization. In this section, we discuss uncharted problems to solve for successful commercialization of each 3-D integration technology.

Two-and-a-half-dimensional integration

Enabling 2.5-D integration requires floorplanning on a silicon interposer and routing through the interposer. Although the dies are located on top of the interposer and the routing layers are inside the interposer, routing of the 2.5-D ICs is similar to that of 2-D ICs because flipping the 2.5-D ICs leads to the same routing structure, i.e., the routing layers exist on top of the pins. On the other hand, floorplanning for 2.5-D integration is a bit different from that for 2-D ICs. If 2.5-D integration places 2-D dies on a silicon interposer, floorplanning of the 2-D dies is almost the same as the 2-D floorplanning problem that places 2-D modules on a die.

However, floorplanning of 2-D and 3-D dies across the chips placed on a silicon interposer has not been investigated. As Figure 1 shows, real 3-D floorplanning for 2.5-D integration requires determining the number of 2-D and 3-D dies to mount on a silicon interposer, the locations of the dies, and the locations of the modules in each die. In the figure: 1) six dies are to be placed and two of them are 2-D ICs, another two of them are two-die 3-D ICs, and the other two are three-die 3-D ICs; 2) the locations of the ICs on the silicon interposer are to be determined; and 3) the locations of all the modules integrated in the 2.5-D IC are to be optimized. Definitely the objective function should include wirelength, routability, performance, and temperature. Especially, the routability includes not only intra-IC routability but also inter-IC routability. For instance, placing two modules having many connections between them in two different chips needs as many microbump pins as the connection count. Therefore, poorly placed modules in 2.5-D ICs will increase the total wirelength and result in unroutable designs. Therefore, 3-D floorplanning for the design of 2.5-D ICs should consider all the metrics

while achieving 100% routability. Thermal-aware 3-D floorplanning algorithms for 2.5-D integration should also be developed for more effective heat dissipation in 2.5-D ICs. The temperature models presented in [48] and [49] or the temperature optimization methodology used in [50] could be applied to temperature analysis and optimization of 2.5-D ICs. However, intrachip and interchip thermal conductivities could be very different, so more accurate thermal analysis and models for 2.5-D ICs and effective thermal-aware 2.5-D floorplanning algorithms need to be developed.

TSV-based 3-D integration

TSV-based 3-D integration has been one of the most promising 3-D integration technologies, so a large amount of efforts has been spent to develop design and analysis methodologies and optimization algorithms for TSV-based 3-D ICs.

Three-dimensional floorplanning. Three-dimensional floorplanning of TSV-based 3-D ICs optimizes the locations of the blocks in a given netlist in 3-D. Each block could be a 2-D or 3-D block, and a hard constraint is that any two blocks should not overlap horizontally and vertically. Three-dimensional outlines (width, height, and vertical length of the target 3-D floorplan) can also be given as a hard constraint. The objective function should include wirelength, the volume of the 3-D floorplan, performance, temperature, and so on. Differently from 2-D floorplanning, however, 3-D floorplanning for TSV-based 3-D ICs should also consider TSV insertion, as shown in [51]–[53]. Unfortunately, TSV insertion is a chicken-and-egg problem because optimizing TSV locations requires the locations of the blocks, but optimization of the block locations should consider TSV locations. If 3-D floorplanning does not consider TSV locations, many 3-D nets may need detours that will lead to wirelength overhead. According to [52], 3-D floorplanning needs to consider block locations, TSV locations, 3-D routing, and whitespace manipulation, all at the same time to optimize the objective function. Since some blocks occupy large area or volume, adjusting the locations of the blocks could significantly affect the total wirelength. In addition, the number of TSVs should also be controlled carefully to minimize the area overhead for TSV insertion. For this purpose, multilayer obstacle-avoiding rectilinear Steiner minimum tree (MLOARSMT)

construction algorithms should be developed. The wirelength reduction reported in [52] is 7%–38% for three-die designs and 9%–34% for four-die designs, but more effective algorithms should be developed for adoption of 3-D integration.

Similarly to 2-D floorplanning, more various 3-D floorplanning problems exist for more flexible and useful 3-D floorplanning. Two representative 3-D floorplanning problems are exploiting soft 3-D blocks and bufferable 3-D blocks as those for 2-D floorplanning [54]–[57]. Soft 3-D blocks have variable dimensions (width, height, and vertical length) with a range of volume instead of fixed dimensions. However, the vertical length is discretized because it is integer multiples of the thickness of a die, assuming all the dies have the same thickness. Bufferable 3-D blocks allow CAD tools to insert buffers and TSVs into the blocks so that CAD tools can avoid long detours during 3-D routing. All of these 3-D floorplanning problems have not been investigated yet.

Three-dimensional placement. Three-dimensional placement optimizes the locations of the standard cells in a given netlist in 3-D. Three-dimensional placement is fundamentally the same as 3-D floorplanning of 2-D blocks because both of them optimize the locations of the placeable objects (cells and blocks) in multiple dies. However, perturbing a small area to insert TSVs in 3-D placement does not degrade the total wirelength significantly, so TSV insertion in 3-D placement can be performed after cells are placed. However, performing 3-D placement and TSV insertion at the same time would generate better layouts. The wirelength reduction achieved by four-die designs in [32] is 1%–25% and that in [46] is less than that in [32]. In addition to the wirelength reduction, critical path delay can also be reduced by 3-D integration. The critical path delay reduction achieved by two-die designs in [58] is approximately 10%.

Since heat dissipation is one of the most important issues to be solved in 3-D integration, thermal-aware 3-D placement algorithms have been developed. Luo et al., [46] and Athikulwongse et al., [47] investigated effective heat distribution by analytically optimizing cell and TSV locations. Unfortunately, thermal optimization during 3-D placement degrades wirelength. Therefore, much more effective 3-D placement algorithms that can simultaneously optimize wirelength and temperature should be developed for adoption of TSV-based 3-D integration.

Three-dimensional routing. Routing of 3-D ICs does not require any new algorithms once TSV locations are found because routing after TSV insertion can be performed in each die separately. However, TSVs can also be inserted during routing after placement. Three-dimensional routing can be performed by two existing routing algorithms, multilayer global routing algorithms, and multilayer obstacle-avoiding rectilinear Steiner tree (MLOARST) algorithms [59]. The former collapses routing resources onto a 2-D plane, performs 2-D global routing, and expands the routing result back to 3-D by layer assignment. To apply this algorithm to 3-D routing, the 2-D global routing and the layer assignment algorithms need to consider the number of TSVs to insert and their locations. On the other hand, the MLOARST algorithms handle placement blockages and 3-D routing, so they are more suitable for 3-D routing. However, the runtime of the MLOARST algorithms is long in general. A more optimal algorithm than the MLOARST algorithms for 3-D routing would be an MLOARSMT algorithm, which has not been investigated in the literature yet.

Three-dimensional clock tree synthesis. A simple 3-D clock tree synthesis (CTS) algorithm constructs a 2-D clock tree in each die and connects the source points through TSVs considering the parasitic RC of the TSVs. This 3-D CTS utilizes the minimum number of TSVs, but its wirelength would not be the shortest. On the other hand, utilizing more TSVs could reduce the wirelength further at the cost of TSVs [60]. Although the wirelength is of primary concern in 3-D CTS, prebond and postbond testability is also an important issue in 3-D CTS for yield improvement [61], [62]. Especially, the prebond- and postbond-testability-aware 3-D CTS should minimize the wirelength of the 2-D clock tree constructed for prebond test in each die, that of the whole 3-D clock tree, skew of both 2-D and 3-D trees, and power consumption (and the TSV count depending on the TSV cost).

One of the existing issues in 3-D CTS is whether a 3-D clock tree constructed for a 3-D IC consumes less power than the 2-D clock tree constructed in its 2-D counterpart IC. Power reduction in 3-D integration can also be obtained if the 3-D clock tree has shorter

wirelength than the 2-D clock tree. However, the wirelength of the 3-D clock trees shown in [63] is longer than that of the 2-D clock trees by 33%–46%. Moreover, the actual power consumption of the 3-D clock tree is dependent on both the wirelength and the TSV capacitance. Therefore, even if the planar wirelength of the 3-D clock tree is shorter than that of the 2-D clock tree, the 3-D clock tree might consume more power than the 2-D clock tree. Therefore, 3-D CTS algorithms should also take the TSV count into account to minimize the power consumption of the 3-D clock trees.

Three-dimensional power network design. Power in TSV-based 3-D ICs can be delivered from the bottommost die (assuming the bottommost die is connected to I/O cells) to other dies through power/ground (P/G) TSVs on the chip boundary and/or P/G TSVs in the core area. In any case, signal TSVs in the core area interfere with P/G lines and stripes, so 3-D P/G network design for TSV-based 3-D ICs needs to handle the discontinuity of P/G lines and stripes around signal TSVs. If the height of a TSV is greater than that of a standard cell row, TSVs should be treated as small IPs, so small P/G rings should be inserted around each TSV to guarantee the continuity of P/G lines and stripes. This task could be simplified by designing a signal TSV cell in which P/G rings are contained. In this case, P/G routing should be performed after placement. If TSV locations are changed during any design step, however, P/G routing should be reperformed in the layout area modified.

IR drop in TSV-based 3-D ICs is expected to be smaller than that in 2-D ICs due to smaller footprint area. However, P/G TSV insertion inside the core area can help reduce the IR drop further, so minimizing the number of P/G TSVs satisfying IR drop constraints has been researched in several works [64]–[66]. Ldi/dt noise can also be optimized [64], [67] by optimization of P/G TSV locations.

Inductive-coupling-based 3-D integration

A fundamental difference between an inductive coupling channel and a TSV is that the inductive coupling channel has much higher data rate than a TSV, so transmitting and receiving digital signals through an inductive coupling channel can use serializers and deserializers to fully utilize the data rate. In this case, serialization and deserialization of

multiple nets require that either the initial netlist should contain serializers and deserializers or the design software can insert them into the netlist considering the cell and block locations. This is a new, unique constraint or task existing in the design of inductive-coupling-based 3-D ICs.

Three-dimensional floorplanning. Three-dimensional floorplanning for inductive-coupling-based 3-D ICs is similar to that for TSV-based 3-D ICs. However, there are fundamental differences between these two 3-D floorplanning problems. In the inductive-coupling-based 3-D ICs, two inductive links that belong to different nets should not overlap vertically so that the links do not interfere with each other. This nonoverlap condition is a unique constraint existing in the 3-D floorplanning of inductive-coupling-based 3-D ICs. Due to this new constraint, each 3-D hard block should have the locations of the inductive links in it as input to the 3-D floorplanning so that 3-D floorplanning can avoid aligning inductors belonging to different nets. In addition, the number of inductive links to insert and their locations should also be considered and/or determined during 3-D floorplanning because the inductive links should be placed in whitespace similarly to TSVs. Moreover, the data rate of an inductive link is higher than that of a TSV, so multiple nets can share a single inductive link by utilizing serializers and deserializers. In this case, multiple signals coming from different blocks can share an inductive link placed in whitespace, so assignment of signals to inductive links also becomes an issue in the 3-D floorplanning for inductive-coupling-based 3-D ICs. However, none of these subjects have been investigated yet.

Three-dimensional placement and 3-D routing. Three-dimensional placement for inductive-coupling-based 3-D ICs needs to place inductive links, which can be handled similarly to the TSVs in the TSV-based 3-D ICs. However, there are also fundamental differences between them. First, an inductive link is much larger than a TSV. For instance, the inductor size ranges between 30 μm $\times$ 30 μm and 150 μm $\times$ 150 μm, depending on the communication distance (die thickness) [21], whereas the TSV size ranges between 1 μm $\times$ 1 μm and 5 μm $\times$ 5 μm, depending on the TSV technology. Therefore, placing cells and inductive links is similar to the 3-D mixed-size placement problem rather than the 3-D

gate-level placement. In addition, if it is allowed to reassign 3-D nets to inductive links, as shown in Figure 3, 3-D placement algorithms should be able to consider the reassignment before/during/after 3-D placement, which is a completely new problem.

Another constraint uniquely existing in the 3-D placement of inductive-coupling-based 3-D ICs is that cells should not be placed between two inductors vertically aligned in multidie (more than two dies) 3-D ICs. For instance, cells cannot be placed at the same x- and y-locations as the two inductors placed in die 1 and die 3 for an inductive link, as shown in Figure 4. Thus, the area between two inductors vertically aligned is wasted. A way to avoid this wasted area is to place another inductor in the middle of them so that the three inductors form a single inductive channel. This multidie inductive link can be used to broadcast a signal from a die to multiple dies and is useful for the 3-D nets connecting cells placed in multiple dies. However, if only a few 3-D nets connect cells in die 1 and die 2 through an inductive link and some other nets connect cells in die 1 and die 3 through the same inductive link, it actually wastes the resources.

Once the locations of cells and inductive links in a 3-D IC are finalized, each die in the 3-D IC can be routed independently. However, if reassignment of the 3-D nets to inductive links is allowed during routing, more sophisticated algorithms for the net-to-link reassignment and the construction of a multilayer rectilinear Steiner minimum tree (MLRSMT) considering the locations of the preplaced inductive links should be developed and used. Several different 3-D routing algorithms such as sequential routing of 3-D nets and concurrent routing of 3-D nets could be developed and actual routing of inductive-coupling-based 3-D ICs will need to consider wirelength, timing, distribution of available inductive links, and reassignment of inductive links, which has not been investigated yet at all.

Three-dimensional clock tree synthesis. Although 3-D CTS for inductive-coupling-based 3-D ICs is similar to that for TSV-based 3-D ICs, the area cost of an inductive link is more expensive than that of a TSV. Therefore, inserting too many inductive links is prohibitive, which leads to the minimization of the number of inductive links used for 3-D CTS. However, minimizing the number of inductive links in a 3-D clock tree will not reduce the planar wire-
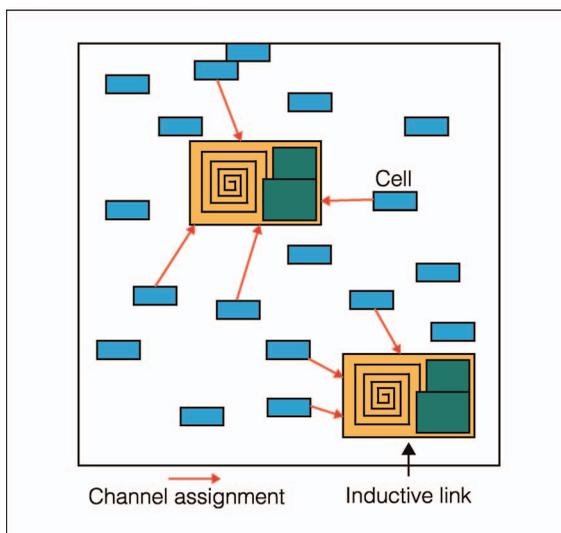
Figure 3. Assignment of 3-D nets to inductive links.

length of the 3-D clock tree. Rather, incorporating the prebond testability with the minimization of the inductive link count will likely increase the planar wirelength of the 3-D clock tree, which will lead to higher power consumption than the clock tree built for 2-D ICs. No work exists on 3-D CTS for inductive-coupling-based 3-D ICs, so more research on this topic should be conducted for adoption of inductive-coupling-based 3-D integration.

Three-dimensional power network design. Power delivery from the bottommost die to other dies in inductive-coupling-based 3-D ICs is more challenging than that in TSV-based 3-D ICs. Depending on in
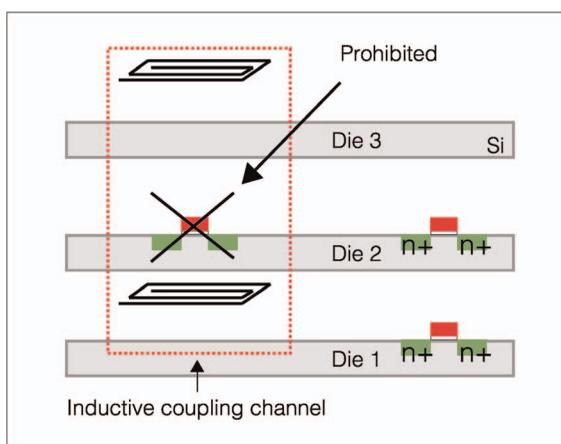
Figure 4. Placing cells between two inductors is prohibited.

which metal layer inductors are created, P/G lines and stripes might need to detour the inductors. In addition, delivering power through P/G inductors is much less efficient than that through wire-bonding or TSVs with respect to the area utilization and power efficiency [68]–[72]. Thus, inserting P/G inductors inside the core area is almost impractical. For power delivery in inductive-coupling-based 3-D ICs, therefore, special-purpose TSVs are used in some applications [22].

Monolithic 3-D integration

Although TSVs and monolithic interlayer vias (MIVs) have very different sizes (1–5 μm versus 0.1 μm), some of the design methodologies for TSV-based could also be used for monolithic 3-D ICs.

Three-dimensional floorplanning. Three-dimensional floorplanning for monolithic 3-D ICs could be performed in two steps: 3-D floorplanning and MIV insertion [73]. Differently from 3-D floorplanning for TSV-based 3-D ICs in which TSV insertion should be considered during 3-D floorplanning not to cause any serious wirelength overhead in the final TSV insertion step, 3-D floorplanning for monolithic 3-D ICs could perform 3-D floorplanning itself without considering the locations of MIVs. This is because MIVs are much smaller than TSVs, so MIV insertion after 3-D floorplanning might not cause serious wirelength overhead. However, 3-D routing should still be considered during 3-D floorplanning for wirelength minimization.

Most of the new 3-D floorplanning problems for TSV-based 3-D ICs such as the two representative 3-D floorplanning problems (soft and bufferable 3-D blocks) discussed in the section on TSV-based 3-D integration also exist in the design of monolithic 3-D ICs. In addition, monolithic 3-D ICs have higher power density than TSV-based 3-D ICs, so 3-D floorplanning for monolithic 3-D ICs should optimize heat removal much more effectively than that for TSV-based 3-D ICs [40].

Three-dimensional placement. Three-dimensional placement algorithms for TSV-based 3-D ICs can also be used for monolithic 3-D ICs. A big difference between them is that TSVs are large, so the TSV count should be carefully controlled in the design of TSV-based 3-D ICs. However, the size of an MIV is similar to that of a local via, so the MIV count may not need to be carefully controlled. For example, when the die size is 1 mm$\times$ 1 mm, utilization is 70%, and the MIV size is 70 nm, the whitespace existing in a layer of the layout can accommodate approximately 15 million MIVs, which is almost infinite. Thus, 3-D placement algorithms for monolithic 3-D ICs can first place cells without considering MIV locations and then insert MIVs for each net during routing. A 3-D placement algorithm for monolithic 3-D ICs is to use an existing 2-D placement tool with uniform downscaling of cell locations and partitioning [30]. This design methodology preserves the relative locations among the cells up to a certain point, but does not guarantee optimality even if the initial 2-D placement result is optimal. However, the methodology is easy to use, so it could be used as a baseline for comparison of 3-D placement algorithms for monolithic 3-D ICs.

Three-dimensional placement for monolithic 3-D ICs should also handle heat dissipation properly. Although various design methodologies and algorithms such as thermal via insertion and alignment for heat dissipation have been developed for TSV-based 3-D ICs [46], [47], there is almost no work on thermal-aware 3-D placement algorithms for monolithic 3-D ICs. For example, redundant MIV insertion for efficient heat transfer and its relationship with routing congestion has not been investigated yet.

Three-dimensional routing and clock tree synthesis. Three-dimensional routing for TSV-based 3-D ICs can also be used for monolithic 3-D ICs. Both of them routes 3-D nets through multiple routing layers. However, 3-D routing for monolithic 3-D ICs might not need to control the MIV count because MIVs are sufficiently small. In this sense, MLOARST or MLOARSMT algorithms that can take the number of MIVs into account should be developed so that 3-D routing for TSV-based 3-D ICs can minimize the TSV count if the TSV size is large and 3-D routing for monolithic 3-D ICs can use sufficiently many MIVs while minimizing the total wirelength.

Three-dimensional CTS algorithms for monolithic 3-D ICs might not need prebond testability unless each tier can be tested during manufacturing. Although a few 3-D CTS algorithms have been used in the literature [30], more general and effective 3-D CTS algorithms that can balance the MIV count and the clock tree wirelength need to be developed to reduce the clock power.

Three-dimensional power network design. Monolithic 3-D ICs have much higher cell density than TSV-based or inductive-coupling-based 3-D ICs. Thus, 3-D P/G network in monolithic 3-D ICs has a larger impact on the quality of the 3-D ICs than that in TSV-based or inductive-coupling-based 3-D ICs [74]. Especially, monolithic 3-D ICs have higher routing congestion than other types of 3-D ICs because of the highest cell density, but MIV insertion has a little impact on the quality of monolithic 3-D ICs. Therefore, P/G network topology generation and optimization algorithms for monolithic 3-D ICs should focus on reducing routing congestion while satisfying IR drop constraints.

AN ENORMOUS AMOUNT of effort has been put on 3-D integration to achieve better performance, lower power consumption, and smaller form factor, but adoption of 3-D integration in the high-performance and/or low-power semiconductor market has been delayed for several years. The delay of the adoption is due to various reasons such as the lack of applications, limitations 3-D integration inherently has, and the lack of standards and CAD tools. To expedite adoption of 3-D integration, more killer applications that can fully exploit the benefits that 3-D integration provides should be developed. In addition, 3-D ICs have more serious heat density problems than 2-D ICs, so more effective heat distribution and removal technologies and algorithms need to be developed. The actual amount of benefits that the papers on the design of 3-D ICs obtained is not satisfactory, so more effective and efficient design methodologies and optimization algorithms for 3-D ICs should also be developed. ∎

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