Evaluating Chip-Level Impact of Cu/Low-κ Performance Degradation on Circuit Performance at Future Technology Nodes

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***Abstract*— Dimensional scaling of interconnects at future technology generations presents major limitations to the improvement of the performances of integrated circuits. In this paper, we investigate the impact of highly scaled Cu/low-κ interconnects on the speed and power dissipation of multiple circuit blocks based on timing-closed full-chip Graphic Database System II (GDSII)-level layouts with detailed routing. First, we build multiple standard cell libraries for 45-, 22-, 11-, and 7-nm technology nodes and model their timing/power characteristics. Next, we pair these standard cell libraries with various interconnect files and build GDSII-level layouts for multiple benchmark circuits to study the sensitivity of the circuit performance and power dissipation to multiple interconnect technology parameters such as resistivity, barrier/liner thickness, and via resistance. We investigate the implications of slowing down interconnect dimensional scaling below 11-nm technology node.**

***Index Terms*— Back-end-of-the-line (BEOL) scaling, Cu/low-κ limitations, GDSII layouts, power/performance analysis.**

I. Introduction

In earlier technology nodes, the resistance–capacitance (RC) delay of electronic chips was dominated by the front-end-of-the-line (FEOL) parameters, such as the resistance of the driver transistor and the receiver load capacitance. With miniaturization of the device and interconnect dimensions for over four decades, the back-end-of-the-line (BEOL) RC delay became a critical factor in determining the performances of modern electronic chips. The resistivity of Cu wires increases rapidly at small dimensions due to increasing electron scattering at the grain boundaries and surfaces. This adverse impact of scaling on the resistance, hence delay of wires, prevents fully exploiting the improvement in the intrinsic device performance. An earlier work that extended to the 65-nm technology node [1] has shown that the interconnect latency problem is not only confined in the global metal levels where interconnects are long, but also extend to the local/intermediate metal levels. As the interconnect dimensions shrink toward the 7-nm technology node, the impact of the resistance increases in metal lines and vias have to be studied carefully to optimize the BEOL architecture.

In [2], we explored the impact of the resistivity increase in local interconnects for future technology nodes based on GDSII-level layouts of a 512-bit fast Fourier transform (FFT) circuit. The main contributions of this paper are as follows.

1) We build multiple predictive cell libraries down to the 7-nm technology node to enable early investigation of the electronic chip performance using commercial electronic design automation tools based on the design and analysis flow that is outlined in [2].
2) We extend the study in [2] to quantify the impacts of intercell and intracell interconnect technology parameters on the speed and power dissipation of multiple circuit blocks with different layouts and wiring demands. We demonstrate that this impact highly depends on the circuit.
3) We investigate the possible issues in slowing down the BEOL scaling below 11-nm technology node to alleviate the resistance increase.

Section II outlines some of the important interconnect and standard cell library properties. Section III summarizes our design results. Section IV focuses on the impact of via resistance. Section V studies an alternative path to BEOL scaling. Section VI concludes this paper.

II. Predictive Libraries

A. Interconnect Definitions

The interconnect structure and the layer dimensions are shown in [2]. All designs in this paper use the minimum number of metal levels that ensures routability. Table I demonstrates the effective resistivity values at these small dimensions calculated [3] considering the impact of size effects and the trench area lost to the barrier material normalized to the bulk Cu resistivity ($1.8\ \mu\Omega \cdot$ cm). The barrier/liner thickness

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TABLE I
NORMALIZED EFFECTIVE Cu RESISTIVITY VALUES

Scenario	Metal Layer	Normalized Resistivity			
		45nm	22nm	11nm	7nm
CASE I	M1	-	5.1	12.98	29.47
$p = 0$, R=0.43,	M2:M3	-	5.05	12.8	28.97
thick barrier	M4:M6	-	2.67	4.73	7.75
CASE II	M1	2.81	4.49	7.75	13.29
$p = 0$, R=0.43,	M2:M3	2.79	4.44	7.67	13.13
ITRS barrier	M4:M6	1.84	2.53	3.85	5.75
CASE III	M1	2.3	3.44	5.63	9.36
$p = 0.2$, R=0.3,	M2:M3	2.29	3.41	5.56	9.24
ITRS barrier	M4:M6	1.62	2.09	2.98	4.26
CASE IV	M1	1.94	2.7	4.13	6.58
$p = 0.25$, R=0.13,	M2:M3	1.93	2.67	4.07	2.35
ITRS barrier	M4:M6	1.46	1.77	2.35	3.2
CASE V	M1	1.68	2.14	3.01	4.52
Single-crystal Cu,	M2:M3	1.67	2.12	2.96	4.44
ITRS barrier	M4:M6	1.35	1.54	1.89	2.41

values are taken from International Technology Roadmap for Semiconductors (ITRS) projections as in [2]. Considering reliability issues at future technology nodes, and challenges in scaling the barrier/liner thickness to ITRS projected values, we also assume thicknesses of 3.5, 3, and 2.5 nm at all metal levels of the 22-, 11-, and 7-nm technology nodes, respectively. These numbers are projected to estimate the resistivity increase through a slower scaling path than the ITRS projections provided that the Cu ratio for the local metal levels are larger than or equal to 50%. Note that comparing the most optimistic (Case V) and most pessimistic (Case II) scenarios of size effects with ITRS projected barrier thickness, the effective Cu resistivity can increase by 2.95× and 2.39× for the local- and intermediate-level wires at the 7-nm technology node. Thicker barrier/liner material can cause these values to go up to 6.52× and 3.22×.

B. Standard Cell Definitions

The predictive standard cell libraries that are used in this paper are obtained using the scaling-based library construction flow [2] to quickly create sufficiently accurate predictive technology libraries to design multiple experimental setups for various interconnect parameters. For this purpose, the parasitics of the gate layouts comprising multigate devices have been scaled from the existing 45-nm library data, which use planar devices. The characterization results for minimum size inverter, NAND2, and D Flip-Flop (DFF) cells are tabulated in Tables II and III. Note that the cell delay highly depends on the interconnect scenario at sub-11-nm technology nodes. Considering a minimum size inverter and comparing Case V and Case I for the interconnect resistivity, the cell delay increases by 18.1% and 44% at the 11- and 7-nm technology nodes, respectively. This moderate change is due to within cell interconnects, which are short.

III. SIMULATION RESULTS

Using our predictive libraries, we run full-chip layout experiments concentrating on three categories of circuits that are represented by an encryption circuit (AES), a low-density parity check circuit (LDPC), and a 256-bit FFT circuit. LDPC represents a group of circuits with a high routing demand. FFT represents circuits with a highly regular layout. Most cells in the FFT circuit that communicate with each other are clustered together. There are a small number of connections between these smaller clusters. The third group of circuits whose regularity lie somewhere between the former two groups are represented by the AES circuit, which is a random logic circuit with a fair amount of routing demand. The placement and routing results for these three circuits considering a pessimistic scenario of interconnects as described in the previous section is shown in Fig. 1.

For each design, we set the maximum target utilization to 85%. This number is adjusted in the case of severe wiring congestions by changing the initial utilization

TABLE II
CELL DELAYS AT A MEDIUM INPUT SLEW/OUTPUT LOAD CASE FOR VARIOUS INTERCONNECT SCENARIOS. INPUT SLEW = 18.75 ps (14.06 ps FOR DFF) AND OUTPUT LOAD = 0.64/0.88/1.76/3.2 fF AT 45/22/11/7-nm TECHNOLOGY NODES, RESPECTIVELY

Scenario	Cell	Delay(ps)			
		45nm	22nm	11nm	7nm
CASE I	INV	-	20.29	12.54	13.04
$p = 0$, R=0.43,	NAND2	-	24.33	14.57	15.55
thick barrier	DFF	-	48.37	23.4	24.34
CASE II	INV	43.55	20.28	11.62	11.6
$p = 0$, R=0.43,	NAND2	49.05	24.32	14.17	13.42
ITRS barrier	DFF	122.9	48.26	22.76	20.17
CASE III	INV	43.56	20.25	10.84	10.79
$p = 0.2$, R=0.3,	NAND2	49.05	24.32	13.74	12.71
ITRS barrier	DFF	122.82	48.08	22.62	19.66
CASE IV	INV	43.62	20.25	10.78	9.78
$p = 0.25$, R=0.13,	NAND2	49.17	24.3	13.6	12.39
ITRS barrier	DFF	122.76	47.94	22.24	18.94
CASE V	INV	43.61	20.24	10.62	9.06
Single-crystal Cu,	NAND2	49.17	24.29	13.53	11.49
ITRS barrier	DFF	122.77	47.55	21.83	18.04

TABLE III
CELL CHARACTERIZATION RESULTS FOR CELL POWER, LEAKAGE, OUTPUT SLEW, AND CAPACITANCE AT A MEDIUM INPUT SLEW/OUTPUT LOAD CASE AS DESCRIBED IN THE CAPTION OF TABLE II

Cell Characteristics		Technology Node			
		45nm	22nm	11nm	7nm
INV	cell power (fJ)	0.445	0.203	0.064	0.074
	input cap. (fF)	0.463	0.346	0.169	0.126
	output slew (ps)	32.29	12.97	8.67	7.6
	leakage (pW)	2843	4311	3055	2438
NAND2	cell power (fJ)	0.669	0.178	0.081	0.063
	input cap. (fF)	0.523	0.233	0.116	0.084
	output slew (ps)	36.75	16.35	9.38	8.32
	leakage (pW)	4962	6019	3698	2907
DFF	cell power (fJ)	3.413	1.859	0.652	0.435
	input cap. (fF)	0.877	0.299	0.145	0.106
	output slew (ps)	35.37	11.17	4.32	3.55
	leakage (pW)	42965	42477	28832	22850

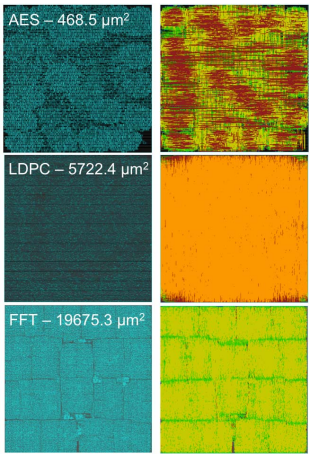

Fig. 1. Placement and routing results for AES, LDPC, and FFT considering a pessimistic scenario for interconnect size effects.

during placement. For instance, due to the high wiring demand of the LDPC, the initial utilization is lowered to 25% to provide enough tracks to route the design by increasing the footprint. FFT, AES, and LPDC are routed with four, five, and six metal levels, respectively. Timing is closed in all of the designs in this paper.

A. Impact of Size Effects on Critical Path Delay

To quantify the impact of the increase in wire resistivity on circuit speed, we gradually reduce the clock period until any further reduction results in a negative worst negative slack value. This is reported as the minimum clock period in Table IV. For all the designs that are reported in this paper, the minimum clock period value decreases if size effects can be mitigated from Case I to Case V in Table I. The impact of interconnect size effects on the circuit speed increases as technology scales. At the 11-nm technology node and beyond, this impact increases drastically. For the AES circuit, the difference in the circuit speed comparing Case I and Case V is as high as 52% and 98% at the 11- and 7-nm technology nodes, respectively. These values are 90% and 143% for LDPC, and 71% and 104% for the FFT circuit. Therefore, irrespective of the circuit size and type, there is a drastic reduction in circuit speed due to interconnect resistivity increase as dimensional scaling continues.

Furthermore, the improvement in the intrinsic device speed at each new technology node translates into smaller and smaller returns in the circuit speed due to the effect of the wires. In fact, in all of the circuits that are studied in this paper, the circuit speed degrades beyond the 11-nm technology node for severe size effect scenarios. Therefore, it is not enough to improve the device intrinsic properties beyond the 11-nm technology node to improve the circuit speed. It is critical to mitigate size effects and find solutions to manufacture thin barrier/liner regions. For instance, the speed of the AES circuit will degrade by 10% from the 11- to the 7-nm technology nodes if the interconnect size effects are as severe as Case II for both technology nodes. By mitigating size effects to Case IV during the shift to the 7-nm technology node, this circuit speed can be improved by 18% instead.

B. Impact of Size Effects on Power Dissipation

For the power dissipation analysis, we run isoperformance simulations for each design at the frequency that each circuit can support for all the experimental setups. As reported in Table IV, this frequency corresponds to the minimum clock period value that is estimated for the simulations in Case I during our analysis for the critical path delay. The power dissipation values are calculated based on a switching activity of 0.2 for primary inputs and 0.1 for sequential cell outputs. The three components of the total power dissipation are as follows.

1) The net switching power, which is the power dissipated in charging the interconnect capacitance and cell pin input capacitances.
2) The cell internal power, which is the power dissipated within each cell including the short-circuit power.
3) The cell leakage power.

The percentage contributions of each of these components to the total power dissipation depend on the circuit. Unlike the critical path delay analysis results, the power dissipation analysis results indicate that the impact of interconnect size effects on total power dissipation highly depends on the circuit. For all of our benchmark circuits, this impact increases with technology scaling.

For the AES circuit, the total power dissipation monotonically increases as the interconnect resistivity is progressively worsened from Case V toward Case I. At each technology node, comparing the results for the most pessimistic and most optimistic interconnect scenarios shows that the power increases significantly at sub-11-nm technology nodes due to the degrading interconnect performance. The percentage increase in total power is 9.51% and 36.73% at the 11- and 7-nm technology nodes, respectively. Most of the change in the power occurs in cell internal power, which is due to both the increase in the number of buffers in the system and the upsizing of some of the gates on the critical paths to meet timing constraints. In this comparison, the increase in the number of buffers is 12.45% and 116.5% at the 11- and 7-nm technology nodes, respectively. The net switching power is also affected by these changes through the insertion of extra input pin capacitance, but the overall impact is not as pronounced as for the cell internal power since the fraction due to the interconnect capacitance changes only slightly. The extra buffers and larger gates directly affect the change in the total cell leakage power as well, but the leakage power is a small component of the total power in our analysis.

The LDPC results are similar to the AES circuit results in terms of the monotonic power dissipation increase with worsening interconnect performance. However, the power dissipation breakdown for the LDPC is very different. The interconnect capacitance has a much more pronounced impact on the total power dissipation of the LDPC compared with the AES circuit. Since this is a wire dominated circuit, the total interconnect capacitance is much larger compared with the total input pin capacitance. Therefore, the largest component of power is the net switching power, which is largely dominated by the interconnect power. As a result,

TABLE IV
PLACEMENT AND ROUTING RESULTS FOR ALL DESIGNS FOR AES, LDPC, AND FFT CIRCUITS AT MULTIPLE TECHNOLOGY GENERATIONS AND CONSIDERING VARIOUS SIZE EFFECT SCENARIOS

Circuit	Tech Node	Design Scenario	Min. Clock Period (ps)	Iso-performance Results							
				Target Period (ps)	Cell Count	Buffer Count	WNS (ps)	Total Power (mW)	Net Switching (mW)	Cell Internal (mW)	Cell Leakage (mW)
AES	45nm	CASE II	714	714	17559	5121	0	18.35	9.9	8.03	0.422
		CASE V	710	714	16907	4818	0	18.05	9.802	7.849	0.403
	22nm	CASE I	236	236	20050	6538	0	20.4	9.703	10.18	0.517
		CASE II	226	236	19818	6379	+2	20.31	9.656	10.14	0.515
		CASE V	216	236	19818	6354	+7	20.15	9.51	10.13	0.511
	11nm	CASE I	164	164	17651	5725	+3	10.29	4.6	5.394	0.291
		CASE II	134	164	17257	5547	+17	9.696	4.507	4.899	0.29
		CASE III	126	164	17695	5518	+34	9.634	4.517	4.832	0.285
		CASE IV	118	164	17381	5219	+36	9.49	4.473	4.737	0.28
		CASE V	108	164	17411	5091	+41	9.396	4.46	4.671	0.265
	7nm	CASE I	202	202	17647	5769	+1	6.094	2.114	3.763	0.217
		CASE II	148	202	15908	4582	+29	5.362	1.875	3.334	0.153
		CASE III	120	202	15604	4537	+24	5.161	1.866	3.145	0.15
		CASE IV	110	202	14425	3855	+44	5.086	2.04	2.902	0.144
		CASE V	102	202	12382	2665	+40	4.457	1.801	2.531	0.125
LDPC	45nm	CASE II	1260	1260	78047	28442	0	178	124.7	51	2.222
		CASE IV	1100	1260	75051	26793	0	167.5	117.7	47.82	2.044
	22nm	CASE I	620	620	60495	22092	0	88.136	57.65	28.85	1.636
		CASE II	590	620	59844	18658	0	86.097	57.25	27.25	1.597
		CASE V	500	620	57129	16601	+2	81.76	53.82	26.54	1.405
	11nm	CASE I	570	570	45583	8711	0	30.28	19.81	9.67	0.798
		CASE II	390	570	43333	6987	+1	28.05	18.59	8.782	0.677
		CASE V	300	570	40975	5007	+1	26.48	17.68	8.227	0.576
	7nm	CASE I	680	680	50735	13744	0	19.19	10.04	8.39	0.752
		CASE II	470	680	45111	8699	0	16.96	9.79	6.597	0.567
		CASE V	280	680	39106	5178	+2	14.45	7.91	6.1	0.438
FFT	11nm	CASE I	480	480	231865	18754	+2	154.847	61.98	88.14	4.727
		CASE II	350	480	230716	17716	+7	153.783	61.32	87.76	4.703
		CASE V	280	480	230608	17502	+21	150.999	59.53	86.8	4.669
	7nm	CASE I	590	590	236174	22881	+2	102.3	33.02	65.41	3.871
		CASE II	370	590	233350	20498	+10	100.19	32.01	64.33	3.849
		CASE V	240	590	231457	18473	+16	98.42	31.5	63.09	3.609

although the interconnect distribution is not a function of the interconnect resistivity as strongly as the number of buffers or the gate sizes, any slight change in this distribution between designs has a larger impact on the net switching power, hence the total power, compared with the AES circuit. In short, due to the change in the weights of the impact of different parameters on the total power dissipation of the circuit, it is not reasonable to expect a larger power dissipation difference between interconnect scenarios for the LDPC than the AES circuit simply based on the critical path delay results. In fact, our results show that the percentage increase in total power when comparing Case I and Case V results for the LDPC is 14.35% and 32.8% at the 11- and 7-nm technology nodes, respectively, which is not too different than the AES circuit results. This is true in spite of the fact that the percentage increase in the number of buffers is 73.97% and 165.4% at the 11- and 7-nm technology nodes, respectively. The significant difference in the impact of interconnects on the percentage change for the critical path delay for AES and LDPC circuits does not reflect to the power dissipation results in the same way due to the difference in the circuit type.

The FFT circuit is a much larger circuit compared with the AES and LDPC circuits. Therefore, the simulation time for the FFT circuit is much longer. To save simulation time, we have focused on the 11-nm technology node and beyond for the FFT circuit because those are the nodes where the more interesting changes occur. Having observed a monotonic change for both the critical path delay and power dissipation analyses in our previous benchmark circuits, we concentrate our efforts on only three cases of interconnect scenarios knowing that the results for the other cases will fall within the range of the results we get if we concentrate on the lower and upper extreme cases. Our results indicate that the significant change in the critical path delay is not translated to the results for the power dissipation in the FFT circuit. Comparing the two extreme cases, the percentage increase in total power is only 2.55% and 3.94% at the 11- and 7-nm technology nodes, respectively. Since most of the cells that communicate with

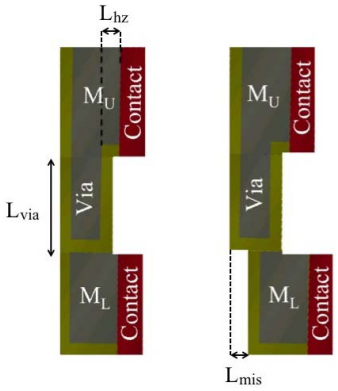

Fig. 2. Simulated structures for well-aligned and misaligned via structures at the 7-nm technology node.

each other are placed closely by the routing tool to minimize the total wire length, which is indicated by the clear clusters of cells in Fig. 1, and there are a small number of connections between these clusters, the cells on the critical path are a very small portion of this large circuit. Therefore, even at the 7-nm technology node, the percentage increase in the number of buffers is only 23.9%.

IV. Impact of via Resistance on Performance

In our analysis, we have focused on the line resistance and have assumed optimistic values for the via resistances to isolate the impact of the line resistance on the overall system performance/power. Recently, it was shown [4] that via resistance has a significant impact on the circuit speed at the 7-nm technology node and needs to be considered in optimizing the BEOL architecture. This paper is based on a circuit model considering an inverter driving a similar inverter through a variable-length horizontal interconnect at the third metal level. In this section, we consider the resistance increase of the via structure due to both dimensional scaling and possible misalignment issues to the underlying metal layer and study the impact of via resistance on circuit performance.

We used Synopsys Raphael [5] to estimate the via resistance at the 7-nm technology node for both the ideal and misaligned via structures. The simulation structure is shown in Fig. 2. The barrier material resistivity is assumed to be 500 $\mu\Omega \cdot$ cm [6]. The Cu resistivity is calculated according to interconnect scenario Case I as defined before. The horizontal run length, L_z, for the top, M_U, and bottom, M_L, metal levels are assumed to be very small to avoid any impact on the final estimated via resistance value. The misalignment length, L_{mis}, is calculated as a percentage of the ideal via width and is varied from 0% to 50% of the width value. The vertical length of the via, L_{via}, is based on the layer definitions as determined during library construction [2]. V1–V3 resistance values for well aligned, 10%, 20%, 30%, 40%, and 50% misaligned cases are 311.4, 313.9, 333.21, 360.6, 397.9, and 456.2 Ω, respectively, at the 7-nm technology node. Via dimensions and resistance values for all via layers are tabulated in Table V for three different cases considering optimistic resistance values that we used so far, a realistic scenario for well-aligned vias and a 50% misaligned via scenario. We quantify the impact of via resistance on the circuit performance/power at the 7-nm technology node based on the design results for the AES circuit from the previous section under interconnect scenario Case I. If the same netlist is used to recalculate the critical path delay of the circuit, we observe a 18.57% increase between Case A and Case B results. This method of comparison is similar to the discussion in [4] as the design is not reoptimized considering the new set of via resistance values. For a fair comparison, however, the correct set of via resistance values have to be considered during the design process, so the timing-driven placement and routing can be performed more accurately for each scenario. The simulation results are tabulated in Table VI. The results for Case C are a worst case corner analysis for via misalignment.

Note that the isolated impact of the via resistance on circuit speed in this scenario is only 3.96% between Case A and Case B. Therefore, the timing-driven placement and routing tools can compensate for the increasing via resistance if the correct values are provided during the design process. For instance, as the via resistance is increased from Case A toward Case C, the number of vias per standard cell in the design reduces and the total wire length increases. This means that the placement and routing tools work to use a smaller number of vias even though the number of standard cells in the design increases, mainly due to a larger number of buffers, while running longer wires to connect them. Therefore, it can be concluded that the tradeoff between using shorter wires to connect two points by changing the metal layer through a via and using a slightly longer wire for the same connection avoiding a via connection shifts toward the latter option as via resistance is increased. In short, the overall impact of via resistance comparing Case A and Case C results for the AES circuit design is to reduce the maximum circuit speed by 13.86% and to increase the total power dissipation by 13.69%.

TABLE V
Via Dimensions and Resistance Values

	Width (nm)	L_{via} (nm)	Resistance (Ω)		
			Optimistic CASE A	Ideal CASE B	50% Misaligned CASE C
V1-V3	10.8	18.7	24.08	311.4	456.2
V4-V6	21.8	45.1	14.25	30.46	67.18
V7-V8	62.2	127.6	0.68	2.97	4.1
V9	124.4	311.2	0.41	0.98	1.28

TABLE VI
Placement and Routing Results for the AES Circuit Under Multiple via Resistance Scenarios

CASE	Min. Clock Period (ps)	Iso-performance Results					
		Target Period (ps)	Cell Count	Via Count	Buffer Count	WL (mm)	Total Power (mW)
A	202	230	17457	124681	5744	24.39	5.246
B	210	230	17736	121695	5801	25.35	5.805
C	230	230	18011	121641	6177	26.73	5.964

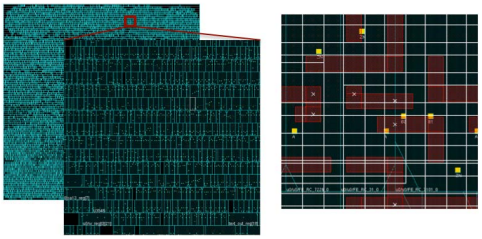

Fig. 3. Placement density for the AES circuit assuming 7-nm FEOL + 11-nm BEOL structure and the routing congestions at $M2$.

V. Alternative Path for BEOL Scaling

In this section, we investigate the implications of using the 11-nm technology node BEOL design with the 7-nm technology node FEOL. In other words, we assume that during the shift from the 11- to the 7-nm technology node, the device dimensions can be shrinked and the intrinsic device performance is improved, but to avoid the significant performance degradation at both the cell and system level due to interconnects, the BEOL dimensions are not scaled. $M1$ is the only metal level that is scaled to the 7-nm technology dimensions in this analysis. This paper is performed for an optimistic interconnect resistivity scenario (Case V).

The results indicate that the major problem with this approach is the routing congestions due to the small dimensions of the cells that are being connected by wide wires. Compared with the all-11-nm technology node, there is a 2.67× reduction in the footprint of the circuit with this approach, while the number of pins to connect stays almost unchanged. The high pin density gives rise to the wiring congestion and design rule violations, as shown in Fig. 3. To overcome the congestion problem, multiple solutions can be tried. The design can be slowed down to reduce the optimization steps including the insertion of buffers, breaking down of complex cells, and upsizing of gates, all of which increase either the total pin density or the silicon area utilization. Extra metal levels can be added or chip area can be increased to satisfy the routing demand. Increasing the chip area is not a preferred solution due to cost reasons. The implications of using an 11-nm BEOL architecture with a 7-nm FEOL without changing the area of the chip or the number of metal levels compared with the all-7-nm technology node are tabulated in Table VII.

Note that if the 11-nm BEOL technology is used with the 7-nm FEOL in the AES design (row 2) without changing the area and the number of metal levels compared with the all-7-nm technology (row 1), the minimum clock period of the circuit needs to be increased by 96.1% to avoid routing congestions and design rule violations. This way, the number of buffers in this design is much smaller, which reduces the pin density. On the other hand, if the original all-7-nm technology was operated at this slow frequency (row3), it would dissipate 5.3% less power, as shown in Table VII. Therefore, slowing down the BEOL scaling to slow down resistivity increase associated with the wires degrades both circuit performance and power dissipation due to congestion problems.

TABLE VII
Design Results for the AES Circuit Using the 7-nm Technology Node FEOL With 7- and 11-nm BEOL Options With Five Metal Levels

BEOL Technology	Min. Clock Period (ps)	Buffer Count	Total Power (mW)
7nm (max. speed)	102	5527	13.41
11nm (max. speed)	200	1467	4.706
7nm (slower)	200	2665	4.457

TABLE VIII
Design Results for the AES Circuit Using the 7-nm Technology Node FEOL With 7- and 11-nm BEOL Options With Extra Metal Levels

BEOL Tech.	T_{min} (ps)	Cell Count	Buffer Count	Footprint (μm^2)	Utilization (%)
Original	102	17851	5527	469.11	86.8
CASE 1	150	17490	5398	468.47	85.6
CASE 2	180	10135	1499	467.19	65.7

Another solution to overcome congestion issues is to increase the routing capacity by adding extra metal levels. Additional metal layers will add to the cost of the chip, but may improve the performance. We compare two cases: 1) add an extra local metal level at the 7-nm technology node local metal dimensions and 2) add an extra intermediate metal level at the 11-nm technology node metal dimensions. As a result, the former scenario (Case 1) has scaled $M1$ and $M2$ whereas $M3$–$M5$ are adopted from the 11-nm technology node BEOL structure and the latter scenario (Case 2) has scaled $M1$ whereas $M2$–$M6$ are adopted from the 11-nm technology node BEOL structure. The results are tabulated in Table VIII.

Case 1 is clearly the better option as it can provide enough routing capacity to increase the silicon area utilization such that a large number of buffers can be inserted to increase circuit speed. However, the minimum clock period is still 50% larger than the original all-7-nm technology node results. Case 2 does introduce some extra routing capacity, but it is not effective enough as indicated by the lower utilization and small buffer count, which result in a slow circuit speed. Therefore, slowing down the BEOL architecture dimensional scaling to compensate for the significant resistivity increase of the wires and the performance degradation that it brings is not a trivial question. During the shift from the 11- to the 7-nm technology node, the wire pitches of the metal levels need to be carefully optimized to maintain routability while trying to avoid performance degradation due to interconnects.

VI. Conclusion

We quantified the implications of the line and via resistance increase at future technology nodes due to size effects based on GDSII-level layouts. We showed that the line resistance increase can hinder circuit performance improvement during the shift from the 11- to the 7-nm technology node. We also showed that via resistance becomes a significant contributor to

circuit delay at the 7-nm technology node, but the placement and routing tools can in part compensate for its impact if the correct via values are considered during design. We underlined that simply slowing down the BEOL scaling to compensate for the resistance increase associated with interconnects is not a trivial problem as it introduces congestion issues, which degrade the performance.

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