Electromigration Study for Multiscale Power/Ground Vias in TSV-Based 3-D ICs

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***Abstract*—Electromigration (EM) in power distribution networks (PDNs) is a major reliability issue in 3-D ICs. While the EM issues of local vias and through-silicon-vias (TSV) have been studied separately, the interplay of TSVs and conventional local vias in 3-D ICs has not been well investigated. This co-design is necessary when the die-to-die vertical power delivery is done using both TSVs and local interconnects. In this paper, we model EM for PDNs of 3-D ICs with a focus on multiscale via (MSV) structure, i.e., TSVs and local vias used together for vertical power delivery. We study the impact of structure, material, and preexisting void conditions on the EM-related lifetime of our MSV structures. We also investigate the transient IR-voltage change of full-chip level 3-D PDNs with MSVs with our model. The experimental results demonstrate that our EM modeling can effectively capture the EM reliability of the full-chip level 3-D PDNs with MSVs, which can be hard to achieve by the traditional EM analysis based on the individual local via or the TSV.**

***Index Terms*—3-D ICs, electromigration (EM), IR voltage, multiscale-vias (MSVs), power distribution network (PDN), reliability, through-silicon-vias (TSVs).**

I. Introduction

ELECTROMIGRATION (EM) is one of the major reliability concerns in advanced IC technology [2]. It refers to the transfer of metal atoms due to the electron current, and is becoming more challenging as feature size shrinks. For EM, local vias in between metal layers of IC have been regarded as EM-prone structures, and have been actively studied [2]–[4]. Meanwhile, EM for through-silicon-vias (TSVs) in 3-D IC technology has drawn lots of attention as well, both for modeling [5]–[10] and measurement [7], [11], [12]. Fig. 1 shows examples of EM-induced voids in a local via and a TSV.

In 3-D power distribution networks (PDNs), local vias often bridge power and ground TSVs, particularly with a via-first/middle approach. Jung and Lim [13] showed that an array of stacked local vias can exist on top of the TSV landing pad for a 3-D PDN as appears in Fig. 2. Because this multiscale via (MSV) including a TSV and array of local vias is essential to a 3-D PDN system, EM issues of MSV needs to be fully studied for reliable 3-D ICs. Nonetheless, there has been little effort to study the EM issue of the MSV structure in a 3-D PDN. Frank *et al.* [11] showed measured data of EM failure in via-first/middle TSV samples, but they used extended M_1 wires to connect the local vias with the landing pad rather than directly placing the local vias on top of the TSV landing pad, which can cause a higher IR-drop for PDNs. Choi *et al.* [12] showed that EM can occur at the MSV structure, but did not analyze EM failure time as a combined effect of EM of local via and TSV. To the best of our knowledge, there has been no work to model EM of MSV considering both EM in local vias and that in TSV.

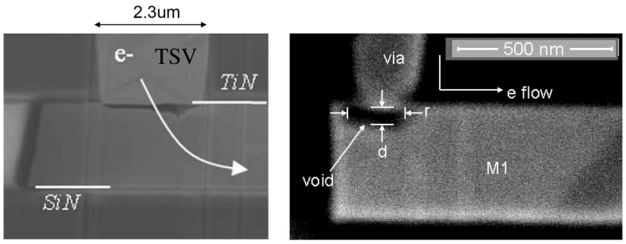

Fig. 1. Void from downstream EM by focus ion beam-scanning electron microscopy (FIB-SEM). Void under (a) TSV [11] and (b) local via (V_1) [14].

In this paper, we study EM robustness of 3-D PDNs with the MSV structure that includes via-first/middle TSV and stacked local vias. Some preliminary results of this paper are published [1]. Overall, our contributions are summarized as follows.

1) We propose an efficient EM modeling flow for MSVs in 3-D PDNs.
2) We investigate the impact of material property, number and size of local vias, and initial void condition on EM-induced failure time of the MSV structure.
3) We study the interplay between the EM of local vias and EM of TSV, and analyze its impact on the EM of the MSV structure.
4) We suggest a full-chip level EM simulation flow of 3-D PDNs with MSVs, and investigate the impact of initial void condition, temperature, and current density on the IR-drop of full-chip level 3-D PDNs.

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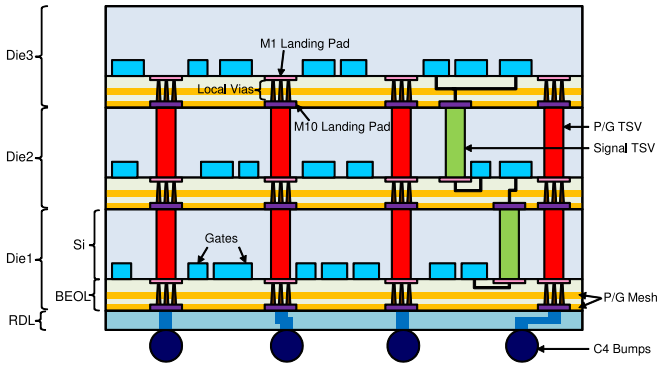

Fig. 2. PDN of 3-D ICs with via-first/middle TSVs [13]. Three dies are stacked with face-down, and power/ground TSVs are vertically connected with stacked local via arrays [13].

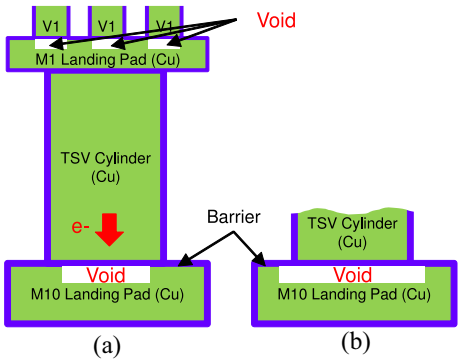

Fig. 3. MSV structure and voids from downstream EM. EM-induced voids are located under the bottom barrier of each TSV and local via. (a) TSV void smaller than a TSV cylinder. (b) Larger TSV void.

The rest of this paper is organized as follows. After introducing the background of this paper in Section II, we show our suggested EM modeling methods for MSV in Section III. We then investigate the impact of various factors on failure time of the MSV structure in Section IV. Finally, we study the EM of full-chip level 3-D PDNs, and show the IR-drop according to the initial void condition, temperature, and current density in Section V.

II. Preliminaries

A. 3-D PDN Structure

Fig. 2 presents the PDN of 3-D ICs with via-first/middle TSVs [13]. Unlike via-last TSVs which go through all the metal layers, via-first/middle TSVs do not penetrate metal layers. Therefore, a TSV can have one landing pad on the global metal layer (M_{10}) and the other landing pad on the local metal layer (M_1) as shown in the Fig. 2. Since the power/ground meshes can be located in the global (M_7–M_{10}) and intermediate metal layers (M_4–M_6), the M1 landing pads need stacked local vias to reach power meshes on the upper metal layers. To reduce the IR-drop and improve EM reliability, stacked local vias can be as many as possible. On the other hand, stacked local vias can be routing blockages, thus it is necessary to determine the proper number of local vias on each landing pad.

We define a MSV, as a structure composed of multiple local vias and a TSV. In an MSV, local vias are connected to a TSV landing pad in one of the BEOL layers, as shown in Fig. 3. On M_1 landing pad of a via-first/middle TSV, an array of local vias (V_1) is directly connected. MSV structures frequently appear in 3-D PDN because local vias directly bridging power mesh and TSVs can achieve minimal IR-drop, especially with via-first and via-middle TSVs. With via-last TSVs, on the contrary, MSVs are unnecessary because TSV landing pads abut power mesh on the top metal. In this paper, we limit our scope to 3-D PDN with MSV structures.

B. Basics of Electromigration

EM is a wear-out failure mechanism for metal interconnects [4]. EM failures are often caused by the interconnect voiding from metal atomic diffusion. This diffusion is driven by the strong flow of electrons, and the strength of electron flow, denoted as current density, is intensified as feature size shrinks, thereby aggravating the EM problem [4]. The vacancy flux due to EM can be expressed with multiple driving forces such as current density, stress gradient, and vacancy concentration, as shown by [15]

$$\vec{J}_v = -D_v \left(\nabla C_v - C_v \frac{eZ^*}{kT} \rho \vec{j} + C_v \frac{f\Omega}{kT} \nabla \sigma \right). \tag{1}$$

Here, J_v is vacancy flux, D_v is effective vacancy diffusivity, C_v is vacancy concentration, ρ is electrical resistivity of the material, $\vec{j}$ is current density, e is electron charge, f is vacancy relaxation ratio, Ω is atomic volume, σ is hydrostatic stress, k and T are Boltzmann constant and absolute temperature, respectively. The effective vacancy diffusivity D_v is expressed by Arrhenius equation [15]

$$D_v = D_o \cdot exp\left(\frac{-Ea}{kT}\right) \tag{2}$$

where Ea is activation energy and D_o is initial diffusivity.

On the right side of (1), the second term is the dominant one that is affected by the current density $\vec{j}$, while the other two factors are of secondary importance. Usually, the first term can be assumed to be negligible [5]. Moreover, if current density and wire length jL is larger than critical Blech product [16] $(jL)_c$ (which is usually true in PDN mesh), we can safely neglect the third stress effect term. Based on our assumption, vacancy flux can be simplified as

$$\vec{J}_v = D_v C_v \frac{eZ^*}{kT} \rho \vec{j}. \tag{3}$$

Equation (3) will be used for our EM model to simulate void growth in Section III. Although some previous works suggested mechanical stress dominance in EM of 3-D ICs [6], [8], others investigated the dominant influence of TSV-induced stress is in the void nucleation phase only [9], [17]. Thus, for the void growth phase, this paper assumes the current effect as the most dominant factor of the void growth by using (3).

Within dual-damascene copper interconnects, wire-via interface is the most EM-critical spot [4]. Depending on the current direction, there are two distinctive categories of EM failure [3]: 1) downstream EM (i.e., line depletion) and 2) upstream EM (i.e., via depletion). With downstream EM, electrons flow from

via top to bottom (current flows from bottom to top), and voids are generated beneath the barrier, at the interface of via trench and the lower metal wire [2], [3]. An example of voids from downstream EM is shown in Fig. 3. On the other hand, with upstream EM, electrons and migrated atoms flow from the bottom to the top of a via, and voids appear inside the via trench [2], [3].

Previous studies showed that the via-wire interface indeed is a site where EM-induced voids appear frequently [11], [14], as shown in Fig. 1. With downstream EM, both local vias and TSV can have voids under the via structure, right under the barrier structure. Fig. 3 illustrates the downstream EM of the MSV structure, with voids under the local vias as well as the TSV. Although our algorithm can be utilized to analyze both upstream and downstream EM, in this paper, we focus on downstream EM for the MSV structure.

For the failure criterion, we use a 10% resistance increase from the initial resistance value of the MSV structure. Previous EM work used either percentage resistance increase (e.g., 10%) [5], [7] or a fixed amount resistance increase (e.g., 10Ω) as their failure criteria [18]. We use percentage resistance increase because it provides a more comparable failure time for vias with different initial resistance. Although a 10% increase of resistance of structure may not lead to a shutdown of the entire power/ground network, it means that the EM problem has already been initiated and EM-induced problem of the PDN, such as an IR-drop increase, can be expected at this point.

EM is generally explained as a two-phase process, void nucleation followed by void growth. However, for deep submicrometer copper interconnects, it is reasonable to assume a very short void nucleation time because it is nearly impossible to have void-free adhesion between copper and barrier/liner material [2]. Especially in 3-D ICs, this assumption can be more valid since the intrinsic stress from TSV manufacturing can shorten the nucleation time further [9], [17]. Thus, this paper assume that the entire failure time can be largely dominated by void growth rather than void nucleation.

III. Modeling of EM for MSV in 3-D PDNs

This section discusses our modeling algorithm for the EM-related lifetime of MSVs in 3-D PDNs. We present our EM modeling algorithm summarized in Fig. 4. This algorithm uses discrete time with small time step, and calculates the degree of void growth under a via using a function named calculate void growth (Section III-A). Once we get the vector of void radius for each TSV and local vias, we calculate the resistance of the entire MSV structure using function calculate resistance (Section III-B). Since the failure criterion is a 10% increase of resistance from the initial resistance, as we explained in Section II, we check the resulting resistance to see whether it exceeds our failure criterion at each time step. Once it is over the failure criterion, our algorithm reports current time step as the failure time. Otherwise, we recalculate current density of each via to reflect the void growth during the current time step, and repeat the cycle.

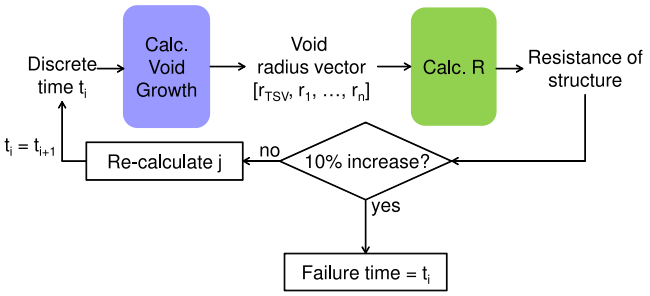

Fig. 4. Flowchart of proposed EM modeling algorithm.

A. Calculating Void Growth

The calculate void growth function accepts its input as current time step, void size, and current density of each via from previous time. The output of this function, void radius vector, contains radius of a cylindrical void under the barrier of the MSV structure as shown in Fig. 3. For example, if an MSV contains four V_1 local vias, void radius vector becomes $[r_{\text{TSV}}, r_1, r_2, r_3, r_4]$, where r_{TSV} and r_i represent void radius of TSV and ith V_1, respectively.

For void growth beneath the TSV barrier, [5], [7] used cylindrical void models. Because slit-like voids under the via tend to grow in a radial direction, we can assume that cylindrical voids have fixed thickness and grow toward a radial direction only, which is similar to [5] and [7].

For void location, we assumed the worst case, the case when the initial void is located at the center of a via, similar to [5] and [7]. This case is the worst in terms of EM reliability because the void blocks the entire via area in the shortest time.

According to[5] and [7], void growth can be expressed by the rate of vacancies captured by a void. Void volume formed by infinitesimal time dt can be expressed as the following:

$$dV = \alpha f \Omega A |J_v| dt \tag{4}$$

where α is the ratio of vacancies captured by the void, A is area under flux effect, and J_v is the vacancy flux [5]. In (3), de Orio *et al.* [5] assumed a constant area, A, no matter how big the void radius is. However, the area under the vacancy flux that contributes to void growth should change as void size grows. Because we assume the cylindrical void grows just in radial direction, only the area around the circumference of a void should be responsible for absorbing vacancies, since that is the front line of void growth. Fig. 5 shows our concept of cylindrical void growth. Unlike [5], we put vacancy absorbing area A in (4) as follows:

$$A = 2\pi r_{\text{void}} \epsilon. \tag{5}$$

Thus, vacancy absorbing area A becomes a function of void radius r_{void}. dV at (4) should be equal to the infinitesimal void volume represented with a dotted line in Fig. 5, then it can be expressed as

$$dV = \alpha f \Omega A |J_v| dt = 2\pi \delta r_{\text{void}} dr \tag{6}$$

and thus

$$dr = \frac{\alpha f \Omega A |J_v| dt}{2\pi \delta r_{\text{void}}} \tag{7}$$

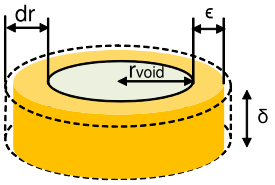

Fig. 5. Cylindrical void under the via. r_{void} is current void radius, dr is infinitesimal void radius growing during time dt, and ϵ is effective radius that governs effective cross area A for absorbing vacancies.

TABLE I
PARAMETER VALUES FOR EM MODELING OF MSVS

Parameter	Description	Value
r_{TSV}	TSV Cu radius	$1.15um$ [7]
l_{TSV}	TSV height	$15.0um$ [7]
$tb_{TSV,side}$	TSV TaN thickness, side	$25.0nm$ [7]
$tb_{TSV,bot}$	TSV TaN thickness, bottom	$45.0nm$ [7]
δ_{TSV}	TSV void thickness	$5.0nm$
LP_{TSV}	TSV landing pad size	$3.6um \times 3.6um$
ϵ_{TSV}	Effective void radius	$\min(0.14um, r_{TSV})$
$t_{LP,M1}$	TSV M_1 landing pad thickness	$0.13um$ [19]
$t_{LP,M10}$	TSV M_{10} landing pad thickness	$2.0um$ [19]
$r_{V1,total}$	V_1 total radius	$32.5nm$ [19]
l_{V1}	V_1 height	$120.0nm$ [19]
$tb_{V1,bot}$	V_1 TaN thickness	$5.0nm$
$r_{V1,Cu}$	V_1 Cu radius	$27.5nm$
ϵ_{V1}	Effective void radius	$\min(3.3nm, r_{V1,Cu})$
δ_{V1}	V_1 void thickness	$1.0nm$
T	Temperature	$453K = 180\ ^\circ C$
ρ_{Cu}	Cu resistivity	$2.73 \times 10^{-8} \Omega m$ at $180\ ^\circ C$
ρ_{TaN}	Barrier (TaN) resistivity	$3.0 \times 10^{-6} \Omega m$ at $180\ ^\circ C$
k	Boltzmann const.	1.38×10^{-23}
α	Ratio of captured vacancies	1.0 [5]
f	Ratio of vacancy volume	0.4 [15]
Ω	Atomic volume	1.182×10^{-29} [15]
D_o	Initial diffusivity	0.0047
Ea	Activation Energy	$0.9eV = 1.44 \times 10^{-19} V$ [7]
Z^*	Effective charge const.	1.0 [5]
e	Electron charge	$1.6 \times 10^{-19} C$
j_o	Initial current density of TSV	$2.5 \times 10^{10} A/m^2$ [7]

where J_v and A are given by (3) and (5), respectively. All the parameters we use are presented in Table I. Unlike [5] and [7], we recalculate current density of each via for each time step to get feedback from the grown voids.

B. Calculating Resistance of MSV

Next step of our EM modeling algorithm is to calculate resistance of the MSV, given the void sizes from the previous step. Here, we suggest an look-up table (LUT)-based resistance network model for the MSV. Our approach contains two steps. First, we build LUTs with a finite element analysis (FEA) tool to derive resistance of TSV and local via with voids, and then we use the resistance network to calculate the total resistance of MSV. We use two different sets of LUTs for TSV and local via, and then utilize them for the resistance network. The advantages of our LUT-based resistance network approach are: 1) easy extension to various conditions such as a different number of vias, because we use accurate FEA results and superpose them for entire resistance and 2) fast and accurate results, because LUTs can enable fast reference and interpolation from simulation results. Use of LUTs provides several orders of magnitude faster access to simulation results than doing simulation with FEA for every input void size. Accuracy loss with LUT is limited because the range of input

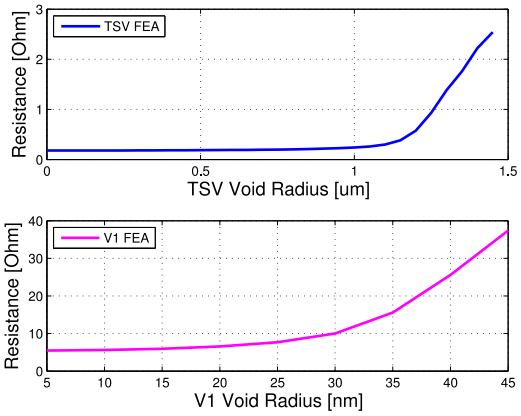

Fig. 6. Relationship between void radius and resistance, for the TSV (top) and for the V_1 (bottom) from FEA simulation. We use TSV radius as 1.15 μm, and V_1 radius as 27.5 nm, thus a void larger than via radius increases the resistance dramatically.

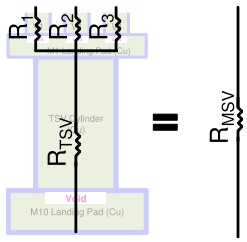

Fig. 7. Resistance network of the TSV and the local via array. Since local vias are connected to the same TSV landing pad, they can be represented as parallel resistance network.

void size is mostly confined to the size of a via and resistance can be assumed to be a continuous function of the void size. To derive resistance of a MSV with certain void size, we use an industrial FEA tool, Comsol multiphysics. Fig. 6 shows an example of void radius and resistance of a TSV and a local via (V_1) from the FEA simulation. All the other parameters are from Table I.

To derive resistance of the whole structure, we construct a simple resistance network as illustrated in Fig. 7. Since local vias are on the same TSV landing pad, they can be represented as a parallel resistance network.

With resistance values of vias retrieved from LUTs, we can now calculate the resistance of the entire MSV structure. For resistance values derived by referring to LUTs (R_i for a local via, and R_{TSV} for TSV), total resistance of the MSV (R_{MSV}) with a single TSV and n local vias is as follows:

$$R_{\text{MSV}} = \frac{1}{\sum_{i=1}^{n} \frac{1}{R_i}} + R_{\text{TSV}} \ , i \in [1, n]. \tag{8}$$

Note that this method can calculate the resistance of the entire structure well regardless of void size distribution among vias. For instance, our algorithm can even be applied to an extreme case where some vias do not have any void at all while others have large voids.

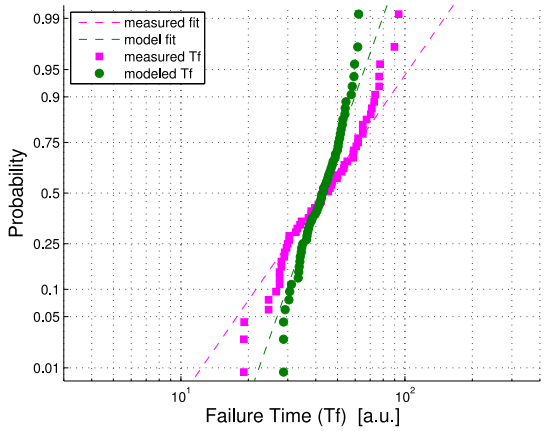

Fig. 8. Comparison of modeled EM-induced failure time against measured data [7] on a log-normal probability plot.

TABLE II
COMPARISON OF MODELED FAILURE TIME AND THE MEDIAN OF MEASURED DATA [18], WHEN $j = 2.50\text{MA}/cm^2$

	Ours	Measured [18]
t_{50} [hr]	89.0	90.5

C. Evaluation of Our Model

We evaluate our modeling method by benchmarking its results against previous measurements of EM-induced failure time for TSV [7] and local via [18]. To the best of our knowledge, no such measurement study has been done for the entire MSV structure that we can compare our result to. However, we can expect that our modeling approach can provide a reasonable estimate of failure time for the entire structure if the modeled failure time of individual components (i.e., TSV and the local via) corresponds with the measured time.

For the comparison of TSV modeling, we apply the parameters used for modeling that are the same as the experimental condition in [7]: temperature as 300 °C, current density as 2.5 MA/cm^2, TSV shape as square of $2.3 \times 2.3\,\mu$m. Since [7] extracts effective barrier resistivity values from their measurement samples, we use their extracted barrier resistivity values to give variation of failure time, similar to [5]. Other parameters are as shown in Table I. Fig. 8 shows EM-induced failure time distributions from measured data and from our modeling. Although our modeling deviates from the measurement results at both extremes, the modeled results around the median corresponds well with the measured data.

Similar to TSV, we compare our modeled failure time of local vias to the measured data [18]. We use the same physical structure as the measurement: we use an additional local via and an M_1 wire, set temperature as 295 °C, set failure criterion as a 10 Ω increase from the initial resistance. We model failure time with the same current density they use, 2.50 MA/cm^2. Other parameters for the EM model remain same as in Table I. Table II shows a comparison of our modeling results against a median failure time t_{50} of measurement [18]. The failure time values closely follow the modeled data.

Together with the TSV comparison result, this result suggests that our model is effective in estimating EM-induced failure time with various types of vias, thus it could provide reasonable estimation with MSV structure. For the rest of this paper, we will use this model to evaluate EM induced failure time, with parameters shown in Table I, unless specified otherwise.

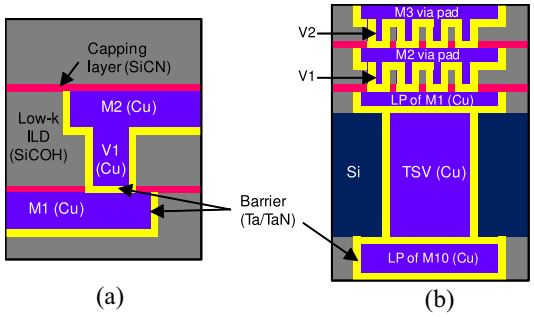

Fig. 9. Schematics of via structures (a) Local via between M_1 and M_2 [20] and (b) MSV including via-first/middle TSV [11] and local vias stacked on top of landing pads. The barrier layer (yellow in this figure) is located at the bottom of both local vias and the TSV.

IV. STUDY ON EM OF MSV WITH VARIOUS FACTORS

This section explores several factors that affect EM-induced failure time. One factor of our interest is the material property, more specifically barrier resistivity. We also discuss other structural factors, such as the number of local vias on a TSV, and the size of a local via that is subject to the via design rule of the technology node. Lastly, we study how initial void size of a TSV can affect the failure time of an entire MSV structure. Throughout this section, we assume 45 nm technology [19].

Our EM modeling algorithm has been implemented with Python programming language, and all the experiments are performed on a machine with 2.93 GHz Intel quad-core Xeon X5670 CPU, 71 GB of memory, Red Hat Enterprise Linux 5.9. Its running time is dependent on the time step size and the detected failure time. In our experiments, we set the step size so that the number of time steps until the failure time is in between a thousand and ten thousand. This provides comparable results across simulation runs and a running time of maximum 30 s for each simulation.

A. Study on Barrier Resistivity

Fig. 9 shows a schematic view of vias in the dual-damascene copper process [11], [20]. For both TSVs and local vias, tantalum (Ta) or tantalum nitride (TaN) can be used as barrier material at the sidewall and the bottom of the via structure. This barrier prevents diffusion of copper to interlayer dielectric, and enhances the adhesion of copper. Although various materials may be used as the barrier material, such as Ta/TaN, TaC, TiN, TiC, WC [2], we limit the scope of this paper to TaN due to its wide use. Because the barrier acts as the physical obstacle to atomic flux (zero atomic flux at the boundary [2]), migrated copper atoms from the via trench cannot cross the barrier, which facilitates void growth under the barrier with downstream EM.

The resistivity of barrier material is difficult to express with a constant. In Table III, we show resistivity variation

TABLE III
RESISTIVITY OF *TaN* ACCORDING TO PARTIAL PRESSURE OF NITRIDE DURING MANUFACTURING [21]

N_2 pressure	0.0%	5.0%	10.0%	20.0%	30.0%
ρ_{TaN} [1e-8Ωm]	95	254	702	2810	14800

TABLE IV
EFFECT OF BARRIER RESISTIVITY ρ_{TaN} ON FAILURE TIME *Tf* OF MSV

ρ_{TaN}[1e-8Ωm]	Tf [a.u.]
200	1300
300	1214
500	1136
1000	1042
2000	992
3000	967
5000	939
10000	917

of barrier material TaN which is usually generated by partial pressure of nitride during manufacturing [21]. We note barrier resistance can vary greatly depending on the partial pressure of nitride. In fact, it is hard to express the barrier resistivity value of a certain barrier structure with a single number because of the variation in the material proportion of compounds as well as in the microstructure such as the grain size and the orientation [2]. Instead of looking at certain values, we observe the impact of a wide range of barrier resistivity values on EM failure time of MSV structures.

Based on our model discussed in Section III, we observe the effect of TaN barrier resistivity on EM failure time of MSVs. For the experiments, we set an initial void radius as 0.1 μm for a TSV, 1 nm for local vias, and assume 676 local vias on top of the TSV landing pad.[1] Other parameters are specified in Table I.

The result, presented in Table IV, shows decreasing failure time, i.e., more vulnerability to EM, as the resistivity of the barrier increases. With the existence of a void under barrier of a via, the current has to detour through the barrier to avoid the void. This detour creates a concentration of the current in a smaller area of the barrier, which magnifies the effect of barrier resistivity, and contributes to the overall resistance increase from void growth. Since our failure criterion involves the relative amount of resistance change, increased resistivity reduces the time to failure.

B. Impact of Void-Free Local Vias

Because a dual-damascene copper interconnect is known to have zero or a small nucleation time, we have assumed that all the local vias and the TSV have nucleated voids that can be grown. However, it is meaningful to see how failure time of MSV changes according to the number of local vias without a void because sets of local vias may exhibit diverse void growth tendency, and a more advanced technology may be able to suppress void nucleation.

Our study with void-free local vias is shown in Table V. Each value represents failure time with a given barrier resistivity and void-free ratio. The results shown in the previous section (Table IV) correspond to the column with 0% void-free ratio. The second column represents an extreme case when all the local vias have growing voids while TSV has no such void, and the last column shows another extreme when only the TSV has growing voids and all the local vias do not have voids at all. The columns in between show failure time of MSV when both local vias and TSV have growing voids due to EM, with varying ratio of void-free local vias.

If all the local vias and the TSV have their own void due to the EM, we get the worst failure time as shown in the column with 0%. In this case, the overall failure time is driven by the local via voids rather than the TSV void. However, with more void-free local vias, the influence of the TSV void gets stronger. Since failure time of the TSV void-only case (last column) is much longer than the failure time of the local via voids-only case (second column), if more and more local vias do not have any void at all, the entire MSV would become much more robust and can achieve EM reliability close to a TSV.

Our findings evince the advantage of our approach. Depending on the void condition of vias, the failure time of MSVs can range from the failure time of the case with local via voids only to that of the TSV void only. Because these diverse void conditions cannot be addressed by other EM models, such as models that only concern local vias or those only for TSVs, our proposed EM modeling for MSV structures is essential to understand the interplay between multiple voids across local vias and the TSV.

C. Study on the Number of Local Vias

The size of a TSV is gigantic (a few μm) in comparison to a local via (a few tens of nm). If we use just a single local via to connect to the TSV landing pad for power delivery, extremely high current crowds to the tiny local via and can have immediate failure from EM even at room temperature. For current load balancing, it is proper to assume multiple local vias on the TSV landing pad for a MSV. In this section, we examine the impact of the number of local vias connected to a TSV. We use 676 vias as the maximum number of local vias in a MSV, observing the design rules [19]. Other than the number of local vias, all the other parameters are still the same as Table I. Here, we assume a Gaussian distribution for current density between testing MSVs.[2]

More local vias on a TSV mean more load balancing of the current, which eventually extends the failure time of a MSV. This tendency is shown in Fig. 10, which is estimated by our EM model (Section III). Increased reliability with more local vias indicates that we can achieve more robust 3-D PDN systems if we have more local vias connected to the TSV landing pads. We note that the failure time is improved by orders of magnitude when we increase the number of local vias from 16 to 676.

[1] 676 is the maximum number of V_1 local vias that can be packed within 3.6×3.6 μm TSV landing pad, assuming 45 nm technology for V_1.

[2] $j = j_o \times (N(100, \sigma^2))/100$ where $\sigma = 4$.

TABLE V
EFFECTIVE OF BARRIER RESISTIVITY ρ_{TaN} ON FAILURE TIME Tf OF MSVS WITH VARYING RATIO OF VOID-FREE LOCAL VIAS

ρ_{TaN}[1e-8Ωm]	Tf by V_1 voids only [a.u]	Tf by both TSV void and V_1 voids [a.u.] (%: V_1s w/o void)						Tf by TSV void only [a.u]
		0%	10%	20%	50%	80%	90%	
200	1311	1300	1594	4806	6658	7189	7269	7328
300	1222	1214	1411	2856	5839	6456	6561	6650
500	1150	1136	1264	1544	4825	5644	5792	5914
1000	1053	1042	1136	1294	3550	4711	4919	5089
2000	1006	992	1058	1167	2533	4075	4286	4444
3000	989	967	1038	1125	2247	3792	4075	4250
5000	967	939	1017	1092	2025	3561	3842	4075
10000	942	917	997	1072	1850	3406	3683	3911
avg. ratio of Tf	1	0.98	1.10	1.73	3.42	4.49	4.68	4.82

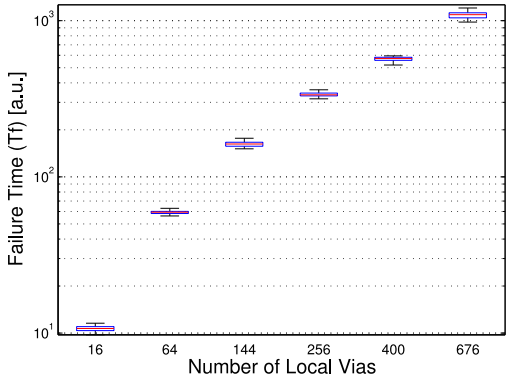

Fig. 10. Impact of the number of local vias on failure time. For each case, 30 samples are used with current density variation. Boxes denote 25 and 75 percentile, while bars are min/max values.

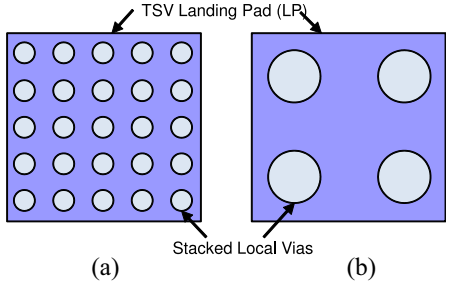

Fig. 11. Example of trade-off between the size and the number of local vias. TSV landing pad with (a) large number of small-sized local vias and (b) small number of large-sized local vias.

D. Trade-Off Between Via Size and Number

We have investigated the impact of the number of vias on failure time in Section IV-C, assuming local vias have the minimum size in V_1 layer. The underlying premise is that a TSV landing pad is located on an M_1 layer if we have a via-first/middle approach for TSV manufacturing. However, via-middle TSV technology makes it possible to build a TSV during the BEOL process, which places the landing pad somewhere between M_1 and M_{10}. With this process, vias connected to a TSV landing pad may become much larger, which may reduce the number of vias, as shown in Fig. 11. In this section, we explore the impact of this trade-off between size of local vias[3] (subject to via layer) and the number of vias connected to a TSV landing pad on the failure time from EM.

In this paper of this trade-off, the diameter of vias d_{via} and the space between vias follows the 45 nm design rule [19]. These parameters from the design rule give us the maximum number of vias within the $3.6 \times 3.6\,\mu$m landing pad. Then the maximum current density of each local via $j_{o,\text{via}}$ is

$$j_{o,\text{via}} = \frac{I_{o,\text{TSV}}}{n \times A_{\text{via}}} = \frac{j_{o,\text{TSV}} \times A_{\text{TSV}}}{n \times A_{\text{via}}} \tag{9}$$

where $I_{o,\text{TSV}}$ and $j_{o,\text{TSV}}$ are total current and current density of TSV, n is the number of local via, and A_{via} is area of local via. We show $j_{o,\text{via}}$ of each layer in the third column of Table VI. Although V_1 is much smaller than V_8, up to 676 V_1 vias can be packed in a landing pad while 16 vias can with V_8, and current density of each local via does not show significant difference.

In Table VI, *Init.* r_{void} and *Crit.* r_{void} represent the radius of an initial and critical void at the local via. We estimate the failure time of the MSV by our model as appears in the seventh column of the table. Area is the area occupied by n local vias at the via layer as follows:

$$\text{Area} = n \times A_{\text{via}} \tag{10}$$

where n is number of local vias. From the Table VI, the failure time (Tf) improves as the TSV landing pad is located in the higher metal layer. This is mainly due to the larger critical void size to reach the failure criterion, and also due to the lower current density in V_4 and V_8.

In case of power/ground MSV structures, total routing blockage can be similar regardless of the metal layer used for the landing pads. For example, if a landing pad is located in the forth metal layer M_4, a TSV cylinder should be fabricated in silicon layer as well as lower metal layers from M_1 to M_3, which makes routing blockage. However, above the M_4, routing blockage also should exist as a form of power/ground local vias pads (or meshes), for the connection to the other die. Therefore, even if we change the landing pad layer from M_1 to M_2/M_4/M_8, the total routing blockage may not change much because it only changes the objects taking the space—whether a TSV or power/ground via pads. Note that this scenario is very different from that of signal TSVs, where we do not use stacked via structures and thus the M_1 landing pad has the smallest routing blockage in general. As a result, our experiment shows less EM with a higher metal layer for the TSV

[3]Here, we use the terminology local via as a via in the BEOL metal layers (V_1–V_9), as a distinct one from the TSV.

TABLE VI
TRADE-OFF BETWEEN THE SIZE OF VIA WITH DIFFERENT VIA LAYERS (V_1–V_8) AND THE NUMBER OF LOCAL VIAS. VIA SIZE IS BASED ON 45 NM TECHNOLOGY [19]

LP Layer	Via Layer	d_{via}/ Space	# via / LP	$j_{o,via}$	Init. r_{void}	Crit. r_{void}	Tf [a.u]	Area	Tf / Area
M_1	V_1	65/75 nm	676	6.47 MA/cm^2	5 nm	36.8 nm	1078	1.61 um^2	670 (1)
M_2	V_2	70/85 nm	529	6.95 MA/cm^2	5 nm	38.0 nm	1044	1.50 um^2	696 (1.03)
M_3	V_4	140/160 nm	144	5.44 MA/cm^2	5 nm	64.8 nm	2411	1.91 um^2	1261 (1.88)
M_4	V_8	400/440 nm	16	5.44 MA/cm^2	5 nm	144 nm	5583	1.91 um^2	2923 (4.36)

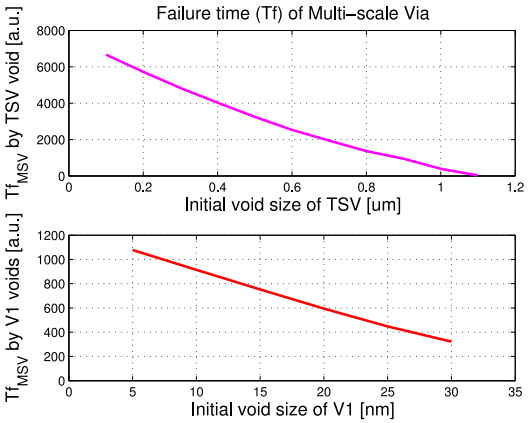

Fig. 12. Impact of initial void size on failure time of MSV. Top: impact of TSV void size, when MSV failure time is driven by the TSV only. Bottom: impact of V_1 void size, when MSV failure time is driven by the V_1s only.

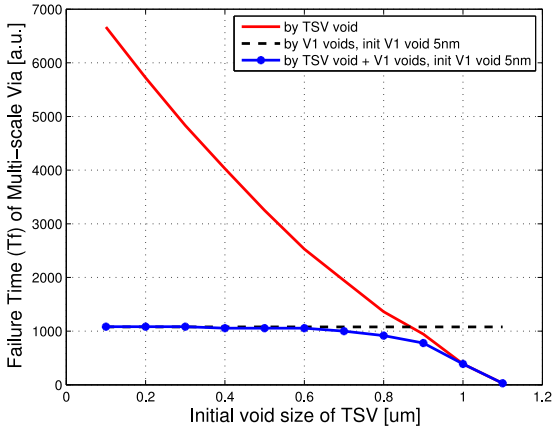

Fig. 13. Impact of a large void (crack) of TSV on failure time of MSV via structure. If a TSV initial void is larger than 0.9 μm and a local via void is 5 nm, and both the TSV void and the local via voids grow due to EM, it follows the TSV void induced failure trends.

landing pads for the MSVs with negligibly increased routing blockage.

E. Analysis of Initial Void Size

In an MSV, both TSV and local vias can have an initial void. First, TSV can have a crack due to the thermo-mechanical stress generated by a coefficient of thermal expansion (CTE) mismatch [22]. For local vias, as the feature size becomes smaller and the aspect ratio of the via trench increases, unsuccessful filling inevitably leaves nano-size voids, which grows with time [2]. Since the initial void size of TSV and local vias can affect the failure time of MSV, we examine how much impact they have through our EM model. First, we reveal the impact of void size of TSV and local via (V_1) on failure time of MSV. The top panel of Fig. 12 shows the impacts of the TSV void size on failure time, when only TSV is responsible to the failure time of MSV. The bottom panel describes impacts of local void size on failure time, when the lifetime of MSV is driven by void growth of local vias only. As the initial void size increases, both cases show degraded robustness by having a shorter lifetime, because it is easier to reach the critical void size with a large initial void.

In general, if only a TSV void governs failure time of MSV (top panel), it is more robust than the opposite case driven by local via voids only (bottom panel). However, we find out that if the TSV has a very large initial void, and V_1 has a smaller initial void, TSV void can dominate the MSV failure time even if both TSV and local vias have growing voids. The relationship between TSV initial void size and failure time of MSV is shown in Fig. 13. In the figure, the red line represents that only the TSV void grows and V_1 does not have any void; in the black dashed line, only the V_1 voids grow with fixed initial void (5 nm); and in the blue line with circles, both TSV and V_1 voids grow, with V_1 initial void as 5 nm. We can see that if the diameter of a TSV initial void is larger than 0.9 μm and that of a local via void is 5 nm, and both TSV void and local via voids grow due to EM, it follows that the TSV void induced failure trends. Although 0.9 μm of the TSV initial void seems to be an extreme case, it implies that a TSV crack can have a visible impact on the EM robustness of a MSV.

V. EM OF FULL-CHIP 3-D PDNS WITH MSVS

There are few papers that have studied full-chip level EM statistically [23], [24], or to have evaluated the impact of EM on performance of the circuits [25]. These works provide meaningful insights of the large-scale reliability evaluation, but their approaches do not focus on getting benefits from the EM modeling of specific interconnecting structures to the full-chip level. References [26] and [27] use statistical EM failure models to analyze reliability and power integrity, but their scopes are focused on the conventional PDNs with wires and local vias, rather than 3-D PDNs. Reference [28] models IR drop of 3-D PDNs with simulation of atomic concentration. It suggests the way to link between the EM modeling of TSVs and the evaluation of full-chip level reliability, but it only considers via-last TSVs, and does not study the interplay between the local vias and via-first TSVs in MSV structures. Moreover, [28] relies on the model with atomic concentration

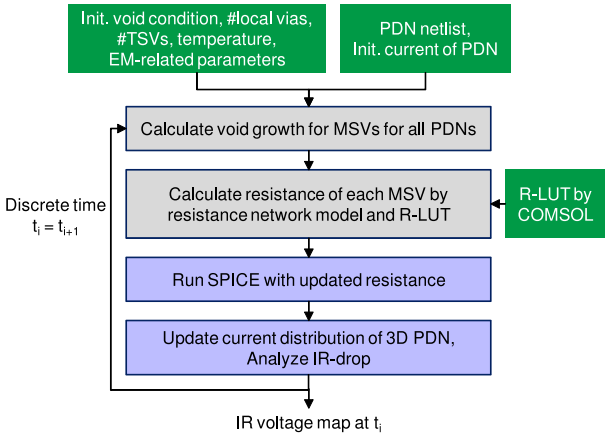

Fig. 14. Flow for EM analysis of full-chip level 3-D PDNs using MSVs.

than the void growth model, it can be hard to analyze the impact of void conditions on full-chip level reliability.

In this section, we extend our EM modeling of a single MSV to the full-chip level 3-D PDNs. First, we describe the overall flow of our transient EM analysis. Based on our full-chip level EM analysis flow, we further investigate the impact of initial void condition, temperature, and current density on IR voltages of 3-D PDNs.

A. Overall Flow of EM Analysis for 3-D PDNs

Fig. 14 shows the overall flow EM analysis for 3-D PDNs. Similar to the single MSV case, we have inputs, such as initial void condition (e.g., void location and initial void size), number of local vias per an MSV, number of TSVs per die, temperature distribution, and EM-related parameters as we shown in Table I. On top of it, we need PDN netlists and initial current distribution of a PDN as inputs for the full-chip analysis. We assume power consumption from gates remains the same as time goes by, meanwhile that from the interconnects can be varied due to the change of resistance of a PDN.

As illustrated in Fig. 14, the first step of full-chip EM analysis is calculating void growth of all MSVs, for a discrete time step. In Section III-A, we described that we can calculate void growth for a single MSV when we assume cylindrical void growth beneath the barrier, under the vias. Here, we extend that methodology to the multiple MSVs. For the multiple MSVs, the basic void growing algorithm is used, but we use different current values for the different MSVs, according to the current distribution information. If we have information on geometric temperature distribution according to time, we can use it in this stage as well. Next, we calculate the resistance of each MSV. Similar to the single MSV case in Section III-B, we use the resistance network model (Fig. 7) and resistance look-up tables (R-LUT) generated by Comsol. And then, we run SPICE simulation with updated resistance of the PDN. After that, we can get the new current distribution for the entire PDN, by reflecting the void growth of each MSV during the time step. We update the current distribution of MSVs accordingly, analyze the IR-drop, and then repeat the process for the next time step.

Algorithm 1: Example of Integration of EM Analysis in a CAD Tool

Require: current density of each node in 3-D PDN
1. Analyze EM: get IR voltage map for the 3-D PDN
while *IR drop* $\geq$ *threshold* **do**
| 2. Improve EM: fix the EM violated nodes
end

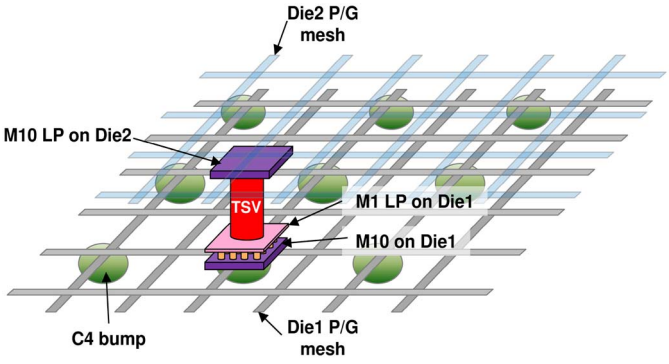

Fig. 15. Illustration of a two-tier 3-D PDN with MSV structures. For simplification, we display only one MSV in this figure.

To integrate this flow into a CAD tool for 3-D ICs, an example is shown in Algorithm 1. Here, the requirement is the current density information of each node in PDN, including MSV structures. The first step is to identify the EM violation, using the suggested EM analysis flow as described in Fig. 14. In this example, the EM failure criteria is based on the IR-drop, and if there is any violated node, the CAD tool calls fixing functions for the node. We refer to the first part as Analyze EM, and the second part as Improve EM. This paper is focused on the first part.

B. EM and IR-Drop Analysis of MSV-Based PDNs

For a single MSV structure, we use a 10% change of resistance as the failure criteria. However, in case of a full-chip PDN, the single-number of failure time can be less meaningful, because we may have a different lifetime for different MSVs, depending on their current distribution and void condition. Thus, we analyze the IR-drop of MSVs according to time, and use it for our reliability metric due to EM.

We measure average IR-drop of the MSVs in the benchmark circuits with our transient simulation, and show the results in Table VII. All the benchmark circuits include two-tier stacked dies with array-time TSVs [28]. Combining the benchmark meshes with our MSV model, we exemplify a two-tier 3-D PDN in Fig. 15. In this figure, two dies are faced down, thus the MSV structure is also upside-down; we can see local via arrays under the TSV cylinder, which is the opposite as we showed in Fig. 3. For Table VII, we assume that the temperature is set to 130 °C, and all the local vias and TSVs have void seeds. In other words, we assume nano-scale initial voids are already nucleated under the local vias and TSVs, and make them grow accordingly as time goes by. We use 676 local vias per MSV structure, which is the maximum number of

TABLE VII
FULL-CHIP EM EVALUATION OF 3-D PDNS USING MSVS. BENCHMARK CIRCUITS ARE THE SAME AS IN [28]

Design	Area [mm^2]	Pwr dens top [W/mm^2]	Pwr dens bot [W/mm^2]	Pwr grid [#×#]	# TSVs	# C4	Avg. IR-drop of MSVs in mV (%increase) t=0s	t=5e7s≈1.6yrs	t=1e8s≈3.2yrs	t=2e8s≈6.3yrs	Avg. runtime per iter. [sec]
PDN1	5x5	0.57	0.57	50x50	144	144	33.96	38.33 (12.9%)	39.93 (17.6%)	41.45 (22.1%)	0.82
PDN2	6x6	0.80	0.75	60x60	225	225	44.82	52.38 (16.8%)	53.11 (18.5%)	57.50 (28.7%)	4.89
PDN3	9x9	0.80	0.80	90x90	484	484	45.60	53.30 (16.9%)	54.08 (18.6%)	59.98 (31.5 %)	7.84
PDN4	11x11	0.71	0.91	110x110	729	729	45.67	53.38 (16.9%)	54.17 (18.6%)	60.60 (32.7%)	13.63
PDN5	15x15	0.47	0.49	150x150	1369	1369	26.66	28.90 (8.4%)	31.40 (17.8%)	39.81 (49.3%)	26.29

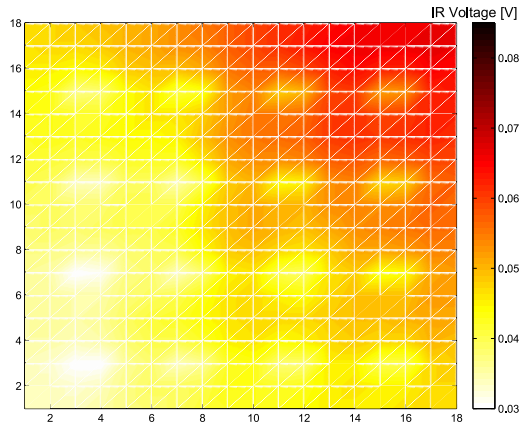

Fig. 16. Initial IR voltage distribution of top die of a small 3-D PDN with MSVs. We use 4×4 TSV arrays for illustration.

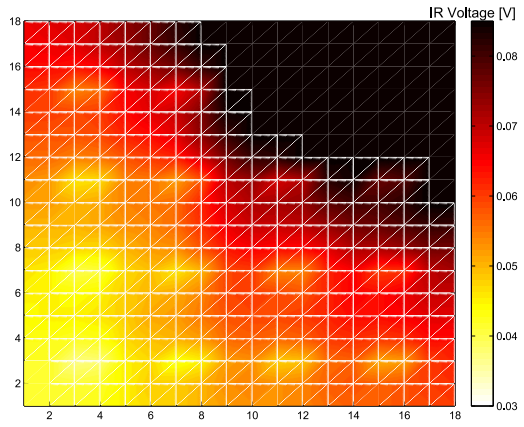

Fig. 17. IR voltage distribution of top die when t = 1.8e8 s. Here, we use temperature as 130 °C, and assume that all the local vias and TSVs have initial voids, to show the worst case scenario. Upper right corner shows significant increase of IR voltages due to EM.

local vias in our setting from 45 nm technology node, as we discussed in Section IV-C.

During our experiments for Table VII, we use the same PDN meshes as [28]. The differences between this paper and [28] are as follows: 1) Zhao *et al*. [28] used via-last TSVs without any local vias while we consider MSVs with local via array and via-first/middle TSVs and 2) we use different modeling of EM, we consider resistance change based on the void growth, whereas [28] is based on the change of atomic concentration without considering void growth. The footprint area, number of TSV and C4 bumps, and power density of benchmark circuits are described in the first seven columns of Table VII. We note that the other EM-related parameters such as temperature may set differently since [28] does not show temperature value, therefore we would like to emphasize that this table is not intended for comparison of reliability between via-last TSVs in [28] and MSV structures in this paper.

From Table VII, we can see that the average IR-drop of MSV structures increase for the long-term simulation. Compared to the initial IR voltages, there is a 31.8% of IR voltage increase after 2e8 s (≈ 6.3 years) passed due to EM. Once EM has occurred, due to the voids developed under the local vias and TSVs, each MSV structure can have a higher resistance than before, and that increases the IR-drop of MSVs and the entire PDNs. In this experiment, we assume that all the C4 bumps are aligned with the TSV locations to minimize IR-drop loss, so a current crowding analysis between TSVs and C4 bumps was not needed, which Zhao *et al*. [28] performed. The average run time is less than 30 s per iteration (i.e., time step) for the largest benchmark, *PDN5*. In our experiments, we use 50 iterations per case for each design.

Figs. 16 and 17 show transient IR-drop change due to EM. For illustration, we use a smaller circuit than the benchmarks in Table VII, it has only 16 MSV arrays. Each MSV has 676 local vias and a single TSV. Comparing between Figs. 16 and 17, we can see that maximum and average IR-voltages increased significantly.

C. Full-Chip EM Analysis on Initial Void Condition of MSVs

With the suggested full-chip EM analysis flow, we investigate the impact of the initial void condition on MSVs. Table VIII shows the average IR-drop of MSVs when t = 2e8 s, under the same condition as Table VII except the initial void condition. For this experiment, we changed the ratio of local vias without initial voids, from 0% to 90%, similarly to the study in Section IV-B. In other words, 0% means that all the local vias have initial voids to grow, and 90% means that 90% of local vias in the MSV structures are void-free. From the table, the average IR voltage increases slower with a higher percentage of void-free local vias. This implies that the importance of perfection in manufacturing; if we have a larger number of imperfect vias with initial defects, we can have a higher IR-drop in a PDN due to EM.

We plot transient IR voltage changes in Fig. 18. According to the time, IR-drop increases, and it rises faster if we have imperfect local vias only (i.e., 0%). Also from the graph, we can see the two-phase of IR-drop increase. The first part is the local via dominant phase. As we discussed in Section IV-E, local vias can contribute more than a TSV to the resistance

TABLE VIII
IMPACT OF INITIAL VOID CONDITION ON AVERAGE IR-DROP VOLTAGES OF FULL-CHIP 3-D PDNS USING MSVS. PERCENTAGE REFERS TO THE RATIO OF VOID-FREE LOCAL VIAS. BENCHMARK CIRCUITS ARE THE SAME AS THE TABLE VII

Design	t = 0	Avg. IR-drop of MSVs in mV at t = 2e8 sec ≈ 6.3 years (%increase)					
		0%	10%	20%	50%	80%	90%
PDN1	33.96	41.45 (22.1%)	39.27 (15.6%)	38.15 (12.3%)	36.72 (8.1%)	36.14 (6.4%)	36.02 (6.1%)
PDN2	44.82	57.70 (28.7%)	54.83 (22.3%)	53.35 (19.0%)	51.46 (14.8%)	50.70 (13.1%)	50.53 (12.7%)
PDN3	45.60	59.98 (31.5%)	57.08 (25.2%)	55.59 (21.9%)	53.67 (17.7%)	52.91 (16.0%)	52.74 (15.7%)
PDN4	45.67	60.60 (32.7%)	57.69 (26.3%)	56.20 (23.1%)	54.28 (18.9%)	53.51 (17.2%)	53.34 (16.8%)
PDN5	26.66	39.81 (49.3%)	38.12 (43.0%)	37.25 (39.7%)	36.13 (35.5%)	35.68 (33.8%)	35.59 (33.5%)

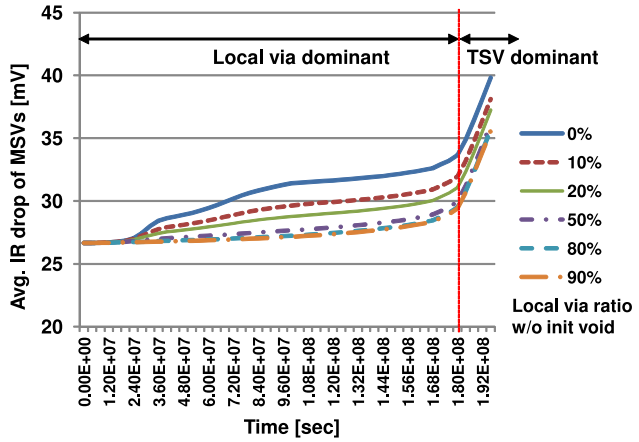

Fig. 18. Effect of initial void condition on average IR-drop of MSVs, from t = 0 to t = 2e8 s. Here, percentage stands for the ratio of void-free local vias; 0% means all the local vias have initial void to grow, 90% means only 10% of local vias have initial voids.

change of an MSV, when the initial void of TSV is not very big. In this phase, we can see that the IR-drop differs largely depending on the ratio of immortal local vias. However, once the local via voids are developed enough, the TSV can dominate the resistance change of an MSV. That appears in the second phase, the TSV dominant phase in this graph. Here, we can see the steep increase of IR voltage on average, because some of the MSVs now have very large resistance, not only due to the local vias voids, but also due to the TSV voids.

D. Temperature and Current Density Impact on EM Reliability of Full-Chip 3-D PDNs

Lastly, the impact of temperature and current density of EM is studied, in terms of IR voltages of MSV-based 3-D PDNs. First, we investigate that the higher temperature can make EM-induced IR-drop worse. Fig. 19 evinces the temperature effect on average IR-drop voltages. For five benchmark circuits, we test IR-drop voltages when t = 2e8 s for two different temperatures, 100 °C and 130 °C. All the other settings are same as Table VII. From the figure, IR voltage increases by 28.2% in the higher temperature (130 °) on average. Because temperature is in the exponent of diffusivity in (2), there can be exponentially worse EM effects with increased temperature. Therefore, it is important to have lower temperature in the operating circuits to reduce EM.

EM is also tightly related with the current density as we discussed in (1). To study current density impact on IR voltages of PDNs, we change input current to 90% and 110%, simulate EM-induced IR-drop voltages of 3-D PDNs. The average

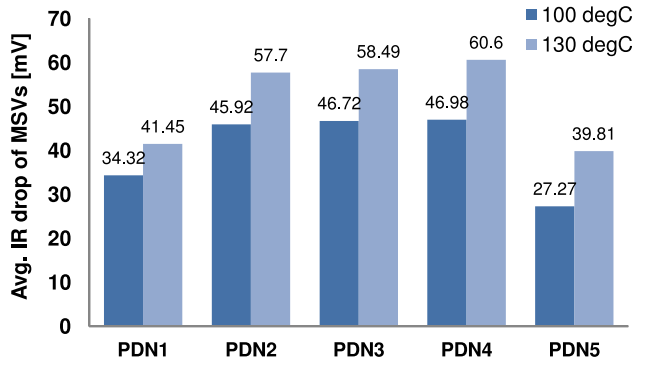

Fig. 19. Graph to show temperature effect on IR-drop of MSVs in 3-D PDN. We changed the temperature from 100 °C, 130 °C, and 160 °C, and get the average IR-drop of MSVs. Here, we assume that all the local vias and TSVs have initial voids, to show the worst case scenario.

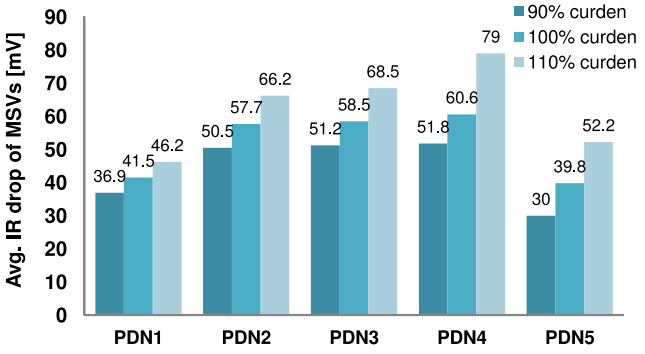

Fig. 20. Impact of current density on average IR-drop of MSVs, when t = 2e8 s. We changed injected current density of each current source, 90%, and 110% from the original values for SPICE simulation. Here, we use temperature as 130 °C, and assume that all the local vias and TSVs have initial voids, to show the worst case scenario.

IR-drop values of MSVs at t = 2e8 s appear in Fig. 20. Comparing to the original current density, 10% decrease of current density shows −14.6% of IR voltages, while 10% increase of current density raises IR voltage by 21% on average.

VI. CONCLUSION

Although the EM of local via and TSVs have been actively studied separately, little effort has been made to analyze EM considering the interplay between local vias and TSV in the MSV for 3-D PDNs.

We summarize the key findings of this paper as below.

1) We propose an efficient EM modeling flow for MSV structure in 3-D PDNs. Our experimental results show

that EM modeling approaches only for TSVs or those for local vias may not be able to estimate the EM reliability of the entire MSV, and that our integrated EM modeling approach is essential for MSV structures in 3-D PDNs.

2) We also investigate the impact of structure, material, and preexisting void condition on EM-critical time of MSV of 3-D PDNs. For the material impact on the EM-induced failure time of MSV, we show that barrier resistivity can have significant effect on the lifetime of the MSV. Also, as many as possible local vias can be necessary to achieve robustness of the MSV structure.
3) Regarding the trade-off between local via size and the number of local vias in the MSV, we find that a small number of large vias can be more preferable to many small vias in terms of EM.
4) We find that barrier resistivity and a preexisting void condition can play a great role in EM lifetime of an MSV structure. Depending on the preexisting void condition, the lifetime of an MSV can be dominated by either TSV or the local via array. In many cases, EM reliability is more likely to be dependent on local vias than TSV. However, if we have local vias without voids, or the preexisting void of the TSV is large enough, the EM of TSV can also dominate the failure time of MSV.
5) We extend our study on EM of an MSV structure to the full-chip level 3-D PDNs. With the suggested EM-evaluation algorithm, we can get the IR-drop of 3-D PDNs with a reasonable run time. Since EM increases resistance of MSVs in a PDN, the IR-drop of a 3-D PDN increases as time goes by, and we study the impact of initial void condition, temperature, and current density on EM of full-chip level 3-D PDNs.

Our experimental results demonstrate that our EM modeling can efficiently estimate the EM reliability of the MSV structures in chip-level 3-D PDNs, and we expect this model to analyze reliability with EM in more complex structures in the future.

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