Through-Silicon-Via Material Property Variation Impact on Full-Chip Reliability and Timing

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***Abstract*—We study the impact of material property variations in through-silicon-via (TSV) and its surrounding structures on the reliability and performance of 3D ICs. We focus on coefficient of thermal expansion (CTE) and Young's modulus variations for TSV, barrier, and liner materials. Our toolset efficiently handles the complexity of modeling and analysis of individual TSVs as well as full-chip 3D IC designs. This tool enables 3D IC designers to accurately assess and evaluate various methods to tolerate mechanical reliability and performance variations.**

I. Introduction

Recently, authors in [1] showed measurement data on the copper (Cu) Young's modulus variation from 65GPa to 165GPa near the top of a Cu TSV as shown in Fig. 1 [1]. This is due to the different sizes and orientations of Cu grains, which are highly process-dependent. They also demonstrated the non-negligible impact of this Cu Young's modulus variation on electron and hole mobility. In addition, it is well known that the CTE of material is temperature and density-dependent. For example, Cu CTE varies from 15.1ppm/K to 24.2ppm/K over the temperature range from 25°C to 250°C [2]. However, there is no full-chip stress analysis tool currently available that considers material property variations and their impact in the full-chip scale.

In this work, we propose a full-chip thermo-mechanical stress and reliability analysis flow under material property variations. We also investigate this variation impact on the full-chip performance. Our comprehensive study encompasses in-depth modeling of individual TSV and device characteristics, efficient method for large-scale full-chip analysis, and design methods for variation tolerance.

II. Single TSV-level Variation Study

We first examine how the variations of CTE and Young's modulus of TSV, barrier, and liner materials affect the thermo-mechanical stress distribution on the *device layer around a TSV* using FEA simulations.

A. Simulation Setup

Our baseline TSV diameter, height, landing pad size, Cu diffusion barrier thickness, and dielectric liner thickness are $5\mu m$, $30\mu m$, $6\mu m$, $50nm$, and $250nm$, respectively. We use Ti and SiO_2 as Cu diffusion barrier and liner materials. The nominal material properties used for our experiments are as follows: Cu = (17/124), tungsten (W) = (4.5/411), Si = (2.3/130), SiO_2 = (0.5/71), and Ti = (8.6/116), where the first and the second values respectively denote CTE (ppm/K) and Young's modulus (GPa).

We use a FEA simulation tool ABAQUS [3]. All materials are assumed to be linear elastic and isotropic [4]. The entire structure undergoes ΔT = -250°C of thermal load (annealing 275°C $\rightarrow$ 25°C) for Cu TSV, and ΔT = -400°C (deposition/annealing 425°C $\rightarrow$ 25°C) for W TSV [5]. In addition, all materials are assumed to be stress free at the annealing temperature.

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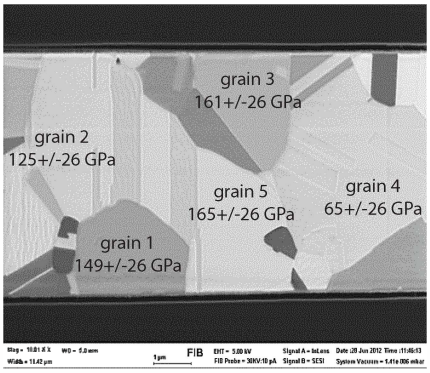

Fig. 1. Significant Cu Young's modulus variation due to the variations on grain size and orientation in Cu TSV (focused ion beam (FIB) image with gray contrast [1]).

B. Variation Impact on Stress

In this section, we examine the impact of each material property on stress and identify the dominant material properties for stress variations. We first vary the CTE and Young's modulus of Cu from -30% to +30% from their nominal values and obtain the σ_{xx} stress distributions on the device layer as shown in Fig. 2. A higher Cu CTE causes a larger CTE mismatch between Cu and Si, hence it elevates the stress level for TSV, barrier, liner, and substrate regions as shown in Fig. 2(a). For the extreme +30% case, the maximum σ_{xx} increases by 42% compared with the $no\ variation$ case.

From Fig. 2(b) we note that Cu Young's modulus variation also affects the stress distribution for all regions, although its impact is lower than Cu CTE. We also performed the same simulations for the TSV barrier and liner materials. We observe that their contributions on the stress distribution are mostly limited within those materials. This is because barrier and liner materials act as a secondary stress contributor in addition to the stress caused by the TSV pillar and substrate.

These simulations clearly show that the material property variation in the TSV materials is the major source for the stress variations. However, we investigate the material property variations in barrier and liner materials to accurately assess the stress inside the barrier and liner as well as the TSV/barrier, barrier/liner, and liner/substrate interfaces.

III. Full Chip-level Variation Study

A. Simulation Settings

In our simulations, we build two-die stack 3D IC designs with Nangate $45nm$ cell library. In addition, we employ two different 3D

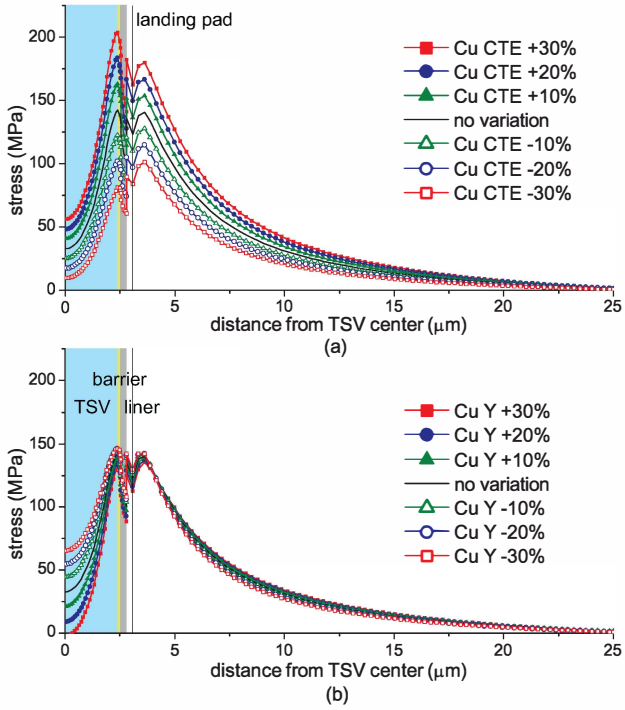

Fig. 2. Cu variation impact on σ_{xx} under various variation ranges (FEA results). (a) Cu CTE variation, (b) Cu Young's modulus variation.

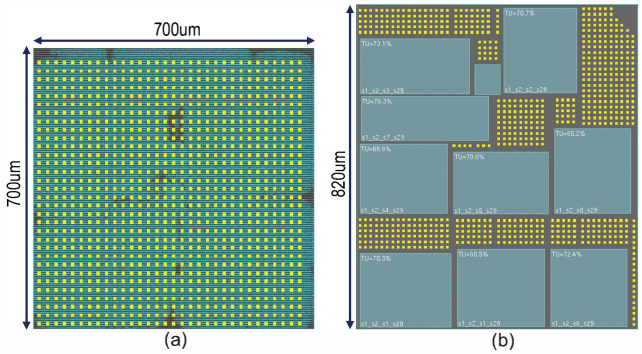

Fig. 3. Layouts of different 3D IC design styles. Yellow rectangles are TSVs. (a) Gate-level design with regular TSV placement (#TSV: 1024). (b) Block-level design (#TSV: 727).

TABLE I
VON MISES STRESS COMPARISON BETWEEN FEA AND OUR METHOD. ERROR = OURS - FEA.

# TSV	FEA		ours		max error (MPa)		
	# node	run time	# grid	run time	inside TSV	TSV edge	outside TSV
1	923K	1h34m	1M	2.5s	5.4	1.2	-1.7
2	1.1M	2h17m	1.2M	4.5s	-6.7	-11.4	-4.3
3	1.5M	2h53m	1.44M	6.2s	-13.2	-13.7	-3.2
5	2.2M	4h23m	2M	10s	-21.1	-18.6	-6.1

IC design styles, i.e., gate-level and block-level designs as shown in Fig. 3. Each 3D design contains 250K cells. The number of TSVs in gate-level and block-level designs are 1024 and 727, respectively. The baseline TSV material, pitch, and keep-out-zone (KOZ) size are copper, $20\mu m$, and $1\mu m$, respectively, unless otherwise specified.

We perform 1000 full-chip Monte Carlo simulations for every test case and set both σ_{CTE} and $\sigma_{Young's\ modulus}$ as 10% of the nominal value of each material. We also assume that material properties follow the normal distribution. We monitor the maximum von Mises stress inside TSV material as a mechanical reliability metric for each simulation. In addition, we check the longest path delay (LPD) and total negative slack (TNS) to examine the material property variation impact on the full-chip performance. The stress-aware 3D static timing analysis flow in [6] is utilized. We normalize the LPD and TNS to the *no variation* case (= [4]).

B. Variation-aware Stress Model

So far, we used an FEA simulator to obtain stress distributions under material property variations. However, in order to conduct *full-chip* stress analysis under variations, we need a parametric stress model that considers variations. We employ the design of experiment (DOE) and response surface method (RSM) to build stress models that consider material property variations in the TSV structure.

To perform DOE and RSM, we first need to define design knobs (= input factors) and metrics (= responses). We use stress tensor as our metric. The stress at a point in a body can be described by a nine-component stress tensor, and only six of them are independent. However, we build models for only four of these elements, i.e., σ_{xx}, σ_{yy}, σ_{zz}, and σ_{xz}. This is because the magnitude of σ_{xy} and σ_{yz} is far much lower than others, and hence their impact on the stress distribution is negligible. In our modeling, we use seven input factors; the variation of CTE and Young's modulus of TSV, barrier, and liner materials (= 6) and the distance from the TSV center (= 1).

We generate 60 design points using Stratified Latin Hypercube from space filling design styles. We set the maximum variation range as $\pm 30\%$ of the nominal value. For each design point, we perform FEA simulation with a single TSV structure and obtain stress data. With these stress tensors, we build the response surface and obtain compact stress models for four stress tensor components.

C. Linear Superposition under Variations

To enable a full-chip stress analysis, we adopt the principle of linear superposition of stress tensors from individual TSVs [4]. The accuracy of linear superposition method compared with FEA simulations is already validated in [4]. Our question is whether this linear superposition method still holds under material property variations among TSVs. In order to answer this question, we assign material properties randomly to each TSV and compare the analysis results with FEA. Table I shows some of our test cases. Results show that large errors occur inside TSV and TSV edge (= TSV/barrier interface). In general, the most critical region for mechanical reliability is at the interface between different materials. Thus, the TSV edge is important in our case. Although the maximum error at the TSV edge is as high as -18.6MPa, the %error is only -4.3%, which is acceptable for a fast full-chip stress analysis.

D. Full-Chip Impact of TSV Pitch

We first examine the impact of TSV pitch on the full-chip mechanical reliability and performance. We use three different TSV pitches for both gate-level and block-level designs; $15\mu m$, $20\mu m$, and $25\mu m$. Table II shows that the mean of von Mises stress is the lowest with the smallest pitch. The von Mises stress is computed considering all stress tensor components. Inside the TSV array, there is destructive stress interference between tensile and compressive stress along the X- and Y-axis, respectively. This destructive stress interference becomes higher with a smaller TSV pitch, and hence reduces von Mises stress level. However, the standard deviation of von Mises stress increases

TABLE II

IMPACT OF TSV PITCH ON FULL-CHIP RELIABILITY AND PERFORMANCE UNDER MATERIAL PROPERTY VARIATIONS. TSV MATERIAL IS CU FOR ALL CASES, AND σ_{CTE} AND σ_Y OF EACH MATERIAL ARE SET AS 10% OF THE NOMINAL VALUES.

TSV pitch (μm)	gate-level design								block-level design							
	von Mises (MPa)		σ_{xx} (MPa)		normalized LPD		normalized TNS		von Mises (MPa)		σ_{xx} (MPa)		normalized LPD		normalized TNS	
	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ	μ	σ
15	585.3	24.8	234.3	8.6	1.000	0.0037	0.996	0.0302	576.5	18.8	230.6	8.7	1.000	0.0007	1.003	0.0164
20	600.0	22.3	230.7	8.3	1.001	0.0036	1.001	0.0296	593.1	18.4	224.6	8.4	1.000	0.0005	0.999	0.0166
25	597.9	22.8	228.3	8.2	1.000	0.0021	1.000	0.0164	588.3	17.9	214.3	8.3	0.999	0.0004	0.993	0.0058

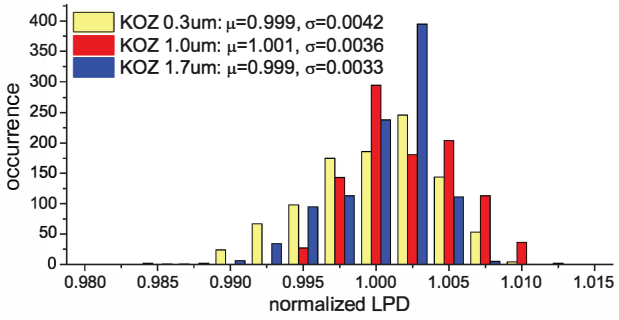

Fig. 4. Impact of KOZ size on full-chip performance under variations. Longest path delay is normalized to *no variation* case (= [4]).

as the TSV pitch decreases. This is because the impact of stress variation in a TSV can easily propagate to nearby TSVs in smaller pitches. On the other hand, the mean and standard deviation of σ_{xx} magnitude increases monotonically with a smaller TSV pitch.

Nonetheless, the impact of TSV pitch on variation tolerance in mechanical reliability metrics is not significant. This is because mechanically instable spots in the TSV structure are TSV/barrier and barrier/liner interface in general, and in this region the TSV under consideration is the dominant stress contributor. Neighboring TSVs act as secondary stress contributors and their impact is limited.

As TSV pitch increases, variations in both LPD and TNS decrease significantly. The standard deviation of LPD and TNS decreases by 43.2% and 45.7%, respectively for gate-level designs and by 42.9% and 64.6%, respectively for block-level designs as the TSV pitch increases from $15\mu m$ to $25\mu m$. Therefore, this TSV pitch is a strong design knob to suppress performance variations under material property variations. However, increasing TSV pitch may lead to larger footprint area, hence a careful design decision needs to be made.

E. Full-Chip Impact of TSV KOZ Size

In this section, we examine the impact of KOZ size on the full-chip performance under material property variations. We employ three different KOZ sizes; $0.3\mu m$, $1.0\mu m$, and $1.7\mu m$. Because we only vary KOZ size with fixed TSV locations, we do not monitor mechanical reliability metrics. In addition, only gate-level designs with $20\mu m$ TSV pitch are examined, since performance variations in block-level designs are much less than gate-level designs.

Fig. 4 shows that the standard deviation of LPD decreases monotonically with a larger TSV KOZ size. Compared with the extreme $0.3\mu m$ KOZ, the standard deviation of LPD decreases by 21.4% with $1.7\mu m$ KOZ. Again, although increasing KOZ size could suppress the full-chip performance variation further, it might incur a larger footprint area and hence slower performance. Thus, the KOZ size needs to be determined carefully.

TABLE III

IMPACT OF TSV MATERIAL ON FULL-CHIP RELIABILITY AND PERFORMANCE UNDER MATERIAL PROPERTY VARIATIONS.

TSV Material	max stress (MPa)		normalized LPD	
	μ	σ	μ	σ
Cu	600.0	22.3	1.001	0.0036
W	396.8	17.6	0.999	0.0025

F. Tungsten vs. Copper TSV on Full-Chip Reliability

The impact of TSV material on full-chip reliability and performance is examined in this section. We employ the gate-level design with a $20\mu m$ TSV pitch. We see that the tungsten TSV shows narrower spread compared with copper TSV for both von Mises stress and LPD as shown in Table III. Moreover, the von Mises stress level is much lower than copper TSV. Since the yielding strength of tungsten is higher than copper, material yielding and interfacial delamination at the TSV/barrier interface for tungsten TSV are less of a concern than copper TSV.

However, the resistivity of tungsten (= $52.8n\Omega \cdot m$) is about 3.1X higher than copper (= $16.78n\Omega \cdot m$). This high resistive tungsten TSV may degrade both performance and 3D IR-drop. Therefore, the choice of TSV material needs to be determined carefully depending on applications.

IV. CONCLUSIONS

We demonstrated how material property variations affect the stress field, mechanical reliability, and performance in 3D ICs. We built stress models that consider CTE and Young's modulus of TSV, barrier, and liner materials using DOE and RSM. We also presented a full-chip thermo-mechanical stress analysis flow under material property variations. We learned that TSV pitch, KOZ size, and TSV material are key design knobs to reduce variations in mechanical reliability and performance under material property variations.

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