# Impact of Size Effects in Local Interconnects for Future Technology Nodes: A Study Based on Full-Chip Layouts

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*Abstract* -- **In this paper, we investigate the impact of local interconnect size effects on the performance of integrated circuits (ICs) based on timing-closed GDSII-level layouts of circuit blocks with detailed routing. For this purpose, we create multiple standard cell and interconnect libraries for 45-, 22-, 11- and 7-nm technology nodes considering scaling trends projected by the International Technology Roadmap for Semiconductors (ITRS) and assuming various sets of size effect parameters. We make comparisons between the performances of circuit designs that are implemented using these libraries.**

## I. Introduction

As the minimum dimensions of both transistors and interconnects scaled for over five decades, gate delays of transistors decreased at each technology generation whereas the resistance-capacitance (RC) limited delays of global level interconnects that ran across the chip increased. Historically, the latency of local/intermediate level wires whose lengths scaled with technology also decreased with dimensional scaling. At ultra-scaled dimensions; however, the effective resistivities, hence delays, of local/intermediate-level Cu wires increase rapidly due to size effects. These size effects include electron scatterings at the wire surfaces and grain boundaries and interconnect process variations. Eventually, the interconnect latency problem became a major performance limitation in both the local/intermediate and global levels [1].

Prior works on the impact of size effects on the overall performance of electronic chips have been based on stochastic wiring distribution models [2] and have treated all wires equally [3]-[4]. However, not all wires on a chip are parts of critical paths and they are not all driven by the same type and size of drivers. In this work, we perform our analysis based on actual netlists and GDSII-level layouts with detailed routing instead of using stochastic models to predict wiring distribution. This methodology is more comprehensive in that it encompasses the diversity of interconnects in terms of length, functionality, and the type and size of drivers and receivers. Since interconnect size effects are more pronounced for local/intermediate-level wires, we concentrate our analysis on block-level circuits instead of a whole processor to reduce simulation time.

## II. Design and Analysis Flow

Our overall design and analysis flow [5] is illustrated in Fig 1. First, we set up interconnect and standard cell libraries for 45-, 22-, 11- and 7-nm technology nodes based on the Nangate 45nm library [6] and considering 4 different sets of size effect parameters spanning a range of Cu resistivity values. These parameters are chosen from experimental results in literature and are referenced in order of increasing severity [7]-[9]. The transistor model used in the Nangate 45nm library is the bulk ASU PTM for 45nm [11]. In generating the 22-, 11- and 7-nm standard cell libraries, we use the ASU PTM for HP multi-gate devices [11]. Next, we use these libraries to synthesize the RTL code for the circuit, perform placement, routing and optimizations, and analyze the results. The placement and routing results for the 7-nm technology generation for two benchmark circuits considering the most pessimistic scenario of size effects is illustrated in Fig 2.

### A. Interconnect Library Preparation

The interconnect dimensions are calculated based on the Nangate 45 nm library and assuming a scaling factor of roughly 0.7× at each new technology node as tabulated in Table I. The Cu resistivity values for these metal layers considering various sets of size effect parameters are shown in Table II. These values are calculated [12] using the appropriate specularity, $p$, and reflectivity, $R$, parameters and a line edge roughness of 40% of the intended wire width [1]. The barrier/liner thickness values are based on the ITRS projections [13] except for one case where the challenges in scaling the barrier/liner thickness are taken into account by assuming thicknesses of 3.5 nm, 3 nm and 2.5 nm at the 22-, 11- and 7-nm technology generations, respectively. The most optimistic scenario is the single-crystal Cu structure, where the grain size is assumed to be infinite to eliminate the impact of grain boundary scatterings on the increase in Cu resistivity [10]. The most pessimistic scenario considers severe size effects and a thick barrier/liner layer.

Using these interconnect layer definitions, we create an interconnect technology file (.ict) and generate a capacitance table file (.captbl) using Cadence Encounter [14], which is used in the initial stages of design. We also create the more detailed .tch file, which is used for more accurate parasitic extraction after detailed routing. The cross-section of the multi-level interconnect structure for the 7-nm node is illustrated in Fig. 3.

### B. Standard Cell Library Preparation

We generate predictive 22-, 11- and 7-nm libraries by scaling the 45-nm library data [15]. The library exchange format (.lef) file for the original 45nm library is modified using the dimensional scaling factors for each new technology. Furthermore, the transistor models in the original RC-extracted SPICE file from the Nangate 45nm library are replaced with the transistor models for the new technology node. The nominal transistor parameters described in [16] are not modified. The cell internal parasitic resistance and capacitance values in this SPICE file are modified with appropriate scaling factors considering that the shape of the cells, hence the length and width of internal interconnects, is changed by the dimensional scaling factor. Assuming that the internal per unit length (p.u.l) capacitances do not change much, the scaling factor for

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parasitic capacitances is chosen the same as the dimensional scaling factor with respect to the 45nm node. For instance, the internal cell capacitances in the 11-nm node become ~0.25× the original values in the 45-nm node. The scaling factors for the p.u.l parasitic resistances in the cells for each technology node are calculated considering the changes in resistivity and cross-sectional dimensions.

The modified RC-extracted SPICE netlist files are used to characterize minimum size INV, NAND2 and DFF cells in the new libraries. Characterization results are compared against the original Nangate 45nm library to calculate scaling factors for multiple cell characteristics for each technology generation and size effects scenario. Some of the characterization results are tabulated in Table III. Final scaling factors are calculated by averaging the scaling factors for the three aforementioned gates. These final scaling factors are applied to the original 45nm library Liberty (.lib) file to generate .lib files for each technology node.

### *C. Design Methodology*

Using our predictive standard cell libraries, we synthesize the RTL code of an interconnect-dominated, ~40K-gate low-density parity check (LDPC) circuit and a 500K-gate FFT circuit in Synopsys Design Compiler [17]. The placement, routing and optimizations are performed using Cadence Encounter. Synopsys PrimeTime [18] is used to analyze the timing/power of the design assuming a switching activity of 0.2 for primary inputs and 0.1 for sequential cell outputs.

## III. Design Results

For each technology generation and size effects scenario, the LDPC and FFT designs are optimized for the maximum clock frequency. The simulations for the FFT design are run for the 7-nm technology node only. The area utilization for the FFT circuit is taken as 65%, but this value is reduced to 33% for the LDPC circuit due to severe wire congestions. All of the designs reported in this work meet the timing constraints. The results for wirelength, standard cell area, and power dissipation of each LDPC design are reported in Table IV.

For the LDPC circuit, as the technology scales from 45nm to 22nm, the total wirelength is scaled by 0.386×, from 22nm to 11nm by 0.57×, and from 11nm to 7nm by 0.6×. The smaller reduction in wirelength for the latter case is because there is only a single generation of advancement whereas there are two generations for the former two cases. The reduction in the total wirelength is mainly due to dimensional scaling and it is not strongly dependent on the size effect parameters. In fact, the overall interconnect distribution does not change significantly with the size effect parameters for any of the technology nodes because the timing driven placement tries to group together the gates that are on the critical paths to minimize the interconnect length, which does not depend on the interconnect resistivity.

We observe that the total area of the circuit scales by 0.22×, 0.25× and 0.39× when the technology advances from 45nm to 22nm, 22nm to 11nm and 11nm to 7nm, respectively. The total circuit area does not change significantly with interconnect size effects because it is determined at the synthesis stage without thoroughly considering the interconnect resistivity. Since we maximize the clock frequency for each design assuming the same area utilization, the total standard cell area does not change significantly even though it depends on the individual sizes of the gates and the total area occupied by buffers, both of which depend on the severity of the interconnect size effects.

The major impact of the interconnect size effects is seen in the minimum target clock period for the LDPC circuit. This impact is twofold: cells tend to become faster as size effects become less severe due to better parasitics and the lower interconnect resistance allows for faster communication between cells. If the size effects can be mitigated and the barrier/liner thickness can be scaled according to ITRS projections, the LDPC circuit speed can be increased by as much as 100% and 80% at the 11- and 7-nm technology nodes, respectively. For the FFT circuit, however, the maximum clock frequency does not depend on the interconnect size effects even though the design is much larger than LDPC because most wires in this design are short enough such that the driver resistance dominates the interconnect resistance.

Comparing the design results for the most pessimistic scenario at various technology generations for the LDPC circuit, it can be seen that the circuit speed does not improve after the 22-nm technology node. For this interconnect-dominated LDPC design, the improvement in device speed with technology scaling is absorbed by the degradation in the interconnect speed. The long wires in the design as illustrated in Fig. 2 for the 7-nm technology node dominate over the improvement in device speed.

## IV. Conclusion

In this work, we investigate the consequences of the impact of size effects on within block interconnects for ICs based on GDSII-level layouts. Size effects impact the speed of the interconnect-dominated LDPC circuit design, but not the much larger FFT design due to its regularity. For designs with long wires such as the LDPC circuit, interconnect performance degradation may dominate over the device speed improvement below the 22-nm technology node.


## Acknowledgment

This work was supported by the Semiconductor Research Corporation program under Task ID 2445.001.


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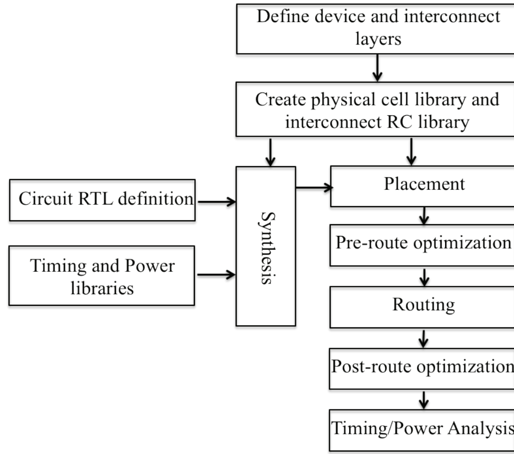


Fig. 1. Overall design and analysis flow

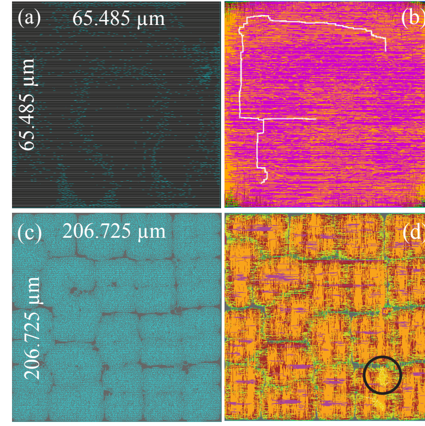


Fig. 2. Design results for the 7-nm technology node considering a pessimistic size effects scenario. (a, b) show placement and routing results for the LDPC design, respectively. (c, d) show placement and routing results for the FFT design, respectively.

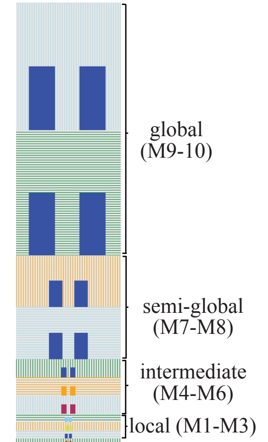


Fig. 3. Metal layer structure shown for the 7-nm technology node

Table I. Interconnect pitch (p), width (w) and thickness (t) for each metal layer at each technology node.

| Layer | Nangate 45nm Library | | | 22nm | | | 11nm | | | 7nm | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | *p (nm)* | *w (nm)* | *t (nm)* | *p (nm)* | *w (nm)* | *t (nm)* | *p (nm)* | *w (nm)* | *t (nm)* | *p (nm)* | *w (nm)* | *t (nm)* |
| M1 | 140 | 70 | 130 | 70 | 35 | 65 | 35 | 17.4 | 32.5 | 21.8 | 10.8 | 20.2 |
| M2-M3 | 140 | 70 | 140 | 70 | 35 | 70 | 35 | 17.4 | 35 | 21.8 | 10.8 | 21.8 |
| M4-M6 | 280 | 140 | 280 | 140 | 70 | 140 | 70 | 35 | 70 | 43.6 | 21.8 | 43.6 |
| M7-M8 | 800 | 400 | 800 | 400 | 200 | 400 | 200 | 100 | 200 | 124.4 | 62.2 | 124.5 |
| M9-M10 | 1600 | 800 | 1600 | 800 | 400 | 800 | 400 | 200 | 400 | 249 | 124.4 | 311.2 |

Table II. Cu resistivity values calculated for each metal layer at each technology node. Specularity and reflectivity parameters are taken as p=0, R=0.43; p=0.2, R=0.3; p=0.25, R=0.13 and p=0.72, R=0 for calculating $\rho_1$, $\rho_2$, $\rho_3$ and $\rho_4$, respectively. The most pessimistic scenario ($\rho_5$) assumes p=0, R=0.43 and a thick barrier/liner layer. All values are normalized to the bulk Cu resistivity, which is 1.8 in μΩ·cm.

| Metal Layer | 45nm | | | | 22nm | | | | | 11nm | | | | | 7nm | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\rho_1$ | $\rho_2$ | $\rho_3$ | $\rho_4$ | $\rho_1$ | $\rho_2$ | $\rho_3$ | $\rho_4$ | $\rho_5$ | $\rho_1$ | $\rho_2$ | $\rho_3$ | $\rho_4$ | $\rho_5$ | $\rho_1$ | $\rho_2$ | $\rho_3$ | $\rho_4$ | $\rho_5$ |
| 1 | 2.38 | 1.96 | 1.65 | 1.42 | 3.69 | 2.84 | 2.22 | 1.77 | 3.86 | 6.32 | 4.59 | 3.37 | 2.46 | 7.72 | 10 | 7.04 | 4.96 | 3.41 | 13.9 |
| 2-3 | 2.36 | 1.94 | 1.64 | 1.42 | 3.67 | 2.82 | 2.21 | 1.75 | 3.84 | 6.27 | 4.56 | 3.33 | 2.43 | 7.67 | 9.93 | 6.98 | 4.89 | 3.36 | 13.8 |
| 4-6 | 1.7 | 1.49 | 1.35 | 1.24 | 2.31 | 1.91 | 1.62 | 1.4 | 2.34 | 3.5 | 2.71 | 2.14 | 1.71 | 3.76 | 5.04 | 3.73 | 2.83 | 2.11 | 5.63 |
| 7-8 | 1.3 | 1.23 | 1.18 | 1.14 | 1.51 | 1.36 | 1.27 | 1.2 | 1.51 | 1.91 | 1.64 | 1.44 | 1.3 | 1.93 | 2.41 | 1.97 | 1.66 | 1.43 | 2.47 |
| 9-10 | 1.19 | 1.16 | 1.13 | 1.12 | 1.29 | 1.22 | 1.17 | 1.14 | 1.29 | 1.49 | 1.36 | 1.26 | 1.18 | 1.49 | 1.73 | 1.52 | 1.36 | 1.25 | 1.74 |

Table III. Cell characterization results for minimum size INV, NAND2 and DFF cells in the original Nangate 45nm library and our predictive 11- and 7-nm libraries. Results are tabulated for the most pessimistic and optimistic size effects scenarios.

| Cell Properties | 45 nm Original Files | | | 11nm | | | | | | 7nm | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | p=0, R=0.43 | | | p=0.72, R=0 | | | p=0, R=0.43 | | | p=0.72, R=0 | | |
| | inv | nand2 | dff | inv | nand2 | dff | inv | nand2 | dff | inv | nand2 | dff | inv | nand2 | dff |
| Delay (ps) | 44.27 | 49.24 | 124.68 | 11.08 | 14.01 | 22.7 | 10.89 | 13.48 | 22.14 | 10.9 | 12.67 | 19.81 | 8.59 | 10.99 | 17.9 |
| Slew (ps) | 31.35 | 35.89 | 34.55 | 8.94 | 9.55 | 4.2 | 8.81 | 9.58 | 4.12 | 8.03 | 8.76 | 3.35 | 9.33 | 9.82 | 3.29 |
| Leak. (pW) | 2843 | 4962 | 42965 | 3055 | 3698 | 28832 | 3055 | 3698 | 28832 | 2438 | 2907 | 22850 | 2438 | 2907 | 22850 |
| Power (fJ) | 0.446 | 0.68 | 3.425 | 0.064 | 0.08 | 0.65 | 0.064 | 0.08 | 0.65 | 0.07 | 0.06 | 0.44 | 0.07 | 0.06 | 0.43 |
| Cap. (fF) | 0.463 | 0.523 | 0.877 | 0.169 | 0.116 | 0.145 | 0.169 | 0.116 | 0.145 | 0.126 | 0.084 | 0.106 | 0.126 | 0.084 | 0.106 |

Table IV. Layout results for multiple technology generations and size effect scenarios.

| Scenario | | Period (ps) | WL (m) | Footprint ($\mu m^2$) | Utilization (%) | Total Power (mW) | Net Switching Power (mW) | Cell Internal Power (mW) | Leakage Power (mW) |
|---|---|---|---|---|---|---|---|---|---|
| 45nm | $\rho_1$ | 1200 | 3.254635 | 207652.9 | 45.1 | 366 | 259.6 | 104.2 | 2.2 |
| 22nm | $\rho_1$ | 1000 | 1.254688 | 45155.03 | 33.95 | 81.3 | 57.5 | 23 | 0.85 |
| | $\rho_4$ | 700 | 1.442086 | 50569.87 | 35.52 | 143.7 | 102 | 40.6 | 1.13 |
| | $\rho_5$ | 1000 | 1.373038 | 44476.66 | 34.51 | 84.3 | 60.2 | 23.2 | 0.87 |
| 11nm | $\rho_1$ | 900 | 0.716144 | 11216.36 | 33.9 | 33.6 | 23.7 | 9.41 | 0.53 |
| | $\rho_4$ | 500 | 0.695486 | 11139.18 | 34.35 | 58.6 | 41.7 | 16.4 | 0.57 |
| | $\rho_5$ | 1000 | 0.656848 | 11206.31 | 33.69 | 29.1 | 20.1 | 8.52 | 0.52 |
| 7nm | $\rho_1$ | 850 | 0.431211 | 4325.4 | 34.09 | 21.2 | 12.2 | 8.65 | 0.42 |
| | $\rho_4$ | 500 | 0.408771 | 4326.14 | 34.15 | 33.9 | 19.6 | 13.9 | 0.43 |
| | $\rho_5$ | 900 | 0.421897 | 4326.14 | 34.17 | 20 | 11.3 | 8.33 | 0.43 |