Analysis and Modeling of DC Current Crowding for TSV-Based 3-D Connections and Power Integrity

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***Abstract*— 3-D integration using through-silicon-vias (TSVs) is emerging as one of the key technology options for continued miniaturization. However, because of increased device and current density, the reliability of the 3-D power grid and its integrity must be studied and analyzed. Due to the geometry of TSVs and connections to the global power grid, significant current crowding can occur. Current densities at these connections can be much higher than the expected average values, so extra care is required for accurate analysis. In prior work, TSVs are modeled as single resistors along with power grid wire segments. Such models do not capture detailed current density distribution and may miss hotspots associated with current crowding. This paper studies current crowding and its impact on 3-D power grid integrity. First, we explore the current density distribution within a TSV and its connections to the global chip power grid. Second, we implement simple TSV models to obtain current density distributions within a TSV and its local environment. These models are checked for accuracy by comparing with models simulated using finite element modeling methods. Finally, the simple TSV models are integrated with the global power grid for detailed chip-scale power analysis.**

***Index Terms*— 3-D, DC current crowding, electromigration (EM), IR, power delivery network (PDN), power integrity, reliability, through-silicon-via (TSV).**

I. Introduction

POWER delivery network (PDN) design has become a challenging task for ICs as technology scales. Since the supply voltage is scaling slower than transistors and interconnects, the current density has been rapidly increasing. The increased current density, along with the high temperature, accelerates transistor and wire degradation and shortens the lifetime of both devices and wires. Today, the current density can reach to several hundred thousands of amperes per square centimeter. At these high current densities, electromigration (EM) becomes significant. PDN design needs to be accurately checked to insure EM current limits are not exceeded and voltage drops (IR) are within specifications before release to manufacturing.

EM and IR drop problems are compounded for 3-D ICs. Specifically, a 3-D PDN provides power supply to all devices in the 3-D stack. The interdie power delivery interconnects, formed by power/ground (P/G) through-silicon-vias (TSVs) or micro-bumps, are unique components in 3-D power grids. These components can carry large amounts of current and may suffer from EM degradation due to an excessive current density as well as have large IR drops. Here again it is important to accurately analyze the 3-D PDN to ensure all EM current limits are not exceeded and all voltage drops are with specifications.

The purpose of this paper is to analyze and model dc current crowding in TSVs and its impact on the power integrity of 3-D PDNs. By power integrity, we mean the impact of current crowding on both EM and IR drop on the PDN. A small cross section of a generic global 3-D PDN is illustrated in Fig. 1. Two dies (top and bottom) are bonded top-face to bottom-back and connected together using vias-last TSVs. Voltage is supplied from the package through C4s. For the bottom die, current is delivered directly from the C4 to Metal 10 and Metal 9. However, for the top die, current is delivered to Metal 10 and Metal 9 through TSVs. Intermediate and local sections of the PDN (using Metal 1 to Metal 8) are connected using local vias to the global PDN, which are not shown in the figure. interdie connections can be made by either directly bonding the landing pads of the bottom-die backside Metal to the top-die Metal 10, or by using micro-bumps. The generic TSV geometry used in this paper has 5-μm diameter and 30-μm height, which is similar to the structure described in [1]. The TSV landing pads are 6 μm $\times$ 6 μm [2] and the global power wires are 2-μm thick. These TSV and PDN structures are used throughout this paper for both isolated TSV modeling and large-scale 3-D PDN modeling.

In this paper, we investigate the dc current density distribution in 3-D IC PDNs with specific focus on the current crowding inside the TSVs and at the connections between TSVs and power wires. We also study the current crowding impact on the effective resistance of the TSV and 3-D power integrity. The contributions of this paper are as follows.

1) The current density distribution inside TSVs and at the connection between TSV and global power wires are investigated in detail. We observe that the effective resistance of the TSV can significantly increase due to current crowding. In addition, the amount of current crowding depends on the thickness and width of the wires connected to the TSV.
2) Discrete resistor models of the TSV are implemented and used to simulate the detailed current density distribution. The accuracy of the discrete models is

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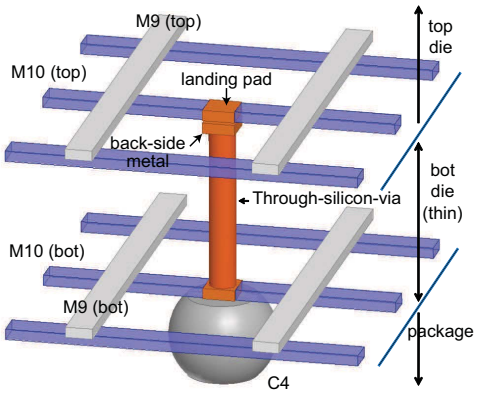

Fig. 1. 3-D connection in a global power delivery network.

determined by comparing with a finite element analysis tool.

3) The discrete resistor TSV models are integrated into the PDN model for detailed chip-scale 3-D PDN analysis using a power grid simulator (PSIM). Simulation results show that PSIM is able to efficiently analyze detailed current density distribution within TSVs in the context of chip-scale PDNs. PSIM can identify regions of high current density or IR drop both across the PDN and within the TSVs providing feedback to help the designer optimize 3-D PDNs.

The organization of this paper is as follows. Section II summarizes the existing work. In Section III, the current density distribution and the voltage drop in a single TSV are analyzed. In Section IV, discrete resistor models of the TSV are implemented and validated. Finally, in Section V, the discrete resistor TSV models are integrated with global PDN wires and simulated together in one model.

II. Review of Existing Works

EM has been studied for many decades and is still an open issue as an unavoidable source of degradation [3]–[5]. In a recent experimental study [6], EM testing on TSVs indicates that voids may form at TSV-to-wire interfaces. Other recent papers have discussed TSV EM modeling. For example, Pak *et al.* [7] studied the EM modeling of TSVs and investigated the impact of TSV mechanical stress on the reliability of neighboring wires. Tan *et al.* [8] analyzed the EM performance of TSV in a silicon interposer, while taking into account the current density, thermal gradient, and stress gradient. However, none of the existing works investigate the current density distribution and current crowding inside TSV-wire connections, where some of the corners may suffer from a large current gradient and are subject to a potential EM reliability issue. It has been suggested that [3] EM may become significant with the current density near or higher than 10 mA/μm^2. The modeling and analysis works referenced above are based on simulations using commercial finite element modeling tools. Although these tools are highly accurate, runtimes for full chip/stack-scale power grid simulation would be computationally prohibitive.

DC current crowding occurs at geometrical bends and corners in the PDN structure, where nonuniform resistive paths can result in large variations of the local current density. Current crowding effect has been studied in ohmic contact resistance of the circular via [9], where an analytical expression has been derived to represent contact resistivity due to current crowding. Although, this paper analyzed 2-D current density distribution and proposed 1-D analytical expression for contact resistivity change, it cannot be used for TSV current modeling where a truly 3-D approach is needed. Other related existing works present measurements of current crowding effect in flip-chip solder joins [10], [11] and copper dual damascene vias [12]. No existing work has discussed current crowding for TSV-based 3-D connections in the context of chip-scale PDN integrity analysis.

Existing works on TSV-based 3-D power delivery network analysis modeled TSVs and power wire segments as single resistors (along with inductors and capacitors). Again this is insufficient to accurately analyze the detailed current density distribution inside P/G TSVs and 3-D PDNs. Huang *et al.* [13] proposed a compact physical modeling approach for 3-D power network analysis. Healy and Lim [14] investigated the impact of the TSV and C4 topology on 3-D power integrity and improved voltage drop and dynamic noise in 3-D power networks. Khan *et al.* [15] analyzed the impact of TSV dimensions and granularity, and C4 spacing on 3-D power delivery design. Jung *et al.* studied the power TSV minimization [16] and analyzed the impact of the power TSV variations on power supply noise [17]. Shayan *et al.* [18] demonstrated the TSV failure impact on power integrity and analyzed several design parameters to mitigate the power noise.

One main goal of this paper is to develop a modeling and simulation methodology for 3-D PDN analysis, which includes the effects of current crowding in TSVs. Although not discussed in this paper, the proposed modeling and simulation methodology is applicable to other 3-D PDN connections, including C4s and micro-bumps. Also not discussed in this paper are model to hardware correlations. As more 3-D test chips are designed and realized, it will be possible to make detailed comparisons using the methodology described in this paper.

III. Current Crowding in 3-D IC

In this section, the current crowding inside a TSV and its local connections to the global PDN are investigated. We discuss the impact of current crowding on the effective TSV resistance and the corresponding voltage drop.

A. Current Density Distribution Inside a TSV

The TSV geometry used to investigate the current density distribution is shown in Fig. 2. This case was chosen specifically to study an asymmetric current distribution and consists of the following components: 1) a TSV with 5-μm diameter and 30-μm height; 2) landing pads (6 μm in width and length); 3) two wires on the top, each 2-μm wide; and 4) one wire on the bottom 6-μm wide. The thickness of wires is 2 μm and the copper resistivity is 18Ω·nm. In typical PDN designs, depending on technology ground-rules, either multiple power wires or a single power wire can connect to a landing pad.

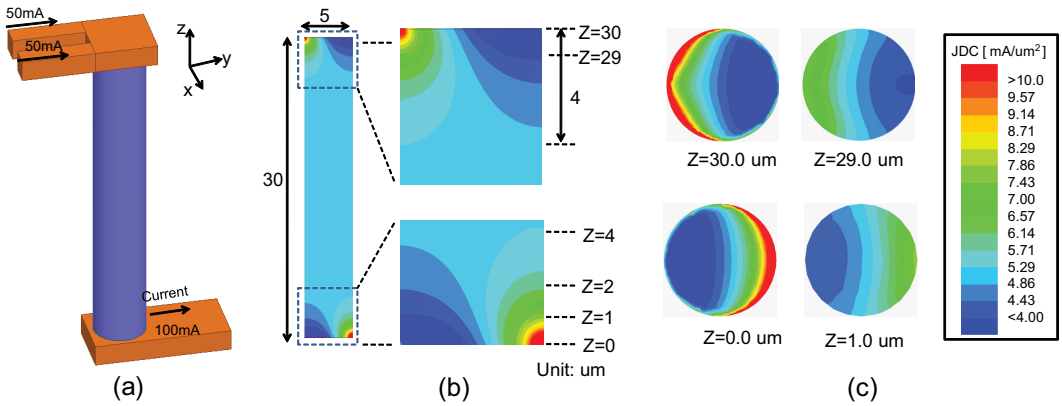

Fig. 2. Current crowding in a test case of a TSV and power wires. (a) TSV geometry: height is 30 μm and diameter is 5 μm. (b) Current density distribution is shown in a ZY plane (side view), and (c) in top-down XY planes for Z = 30.0 μm, 29.0 μm, 1.0 μm, and 0.0 μm.

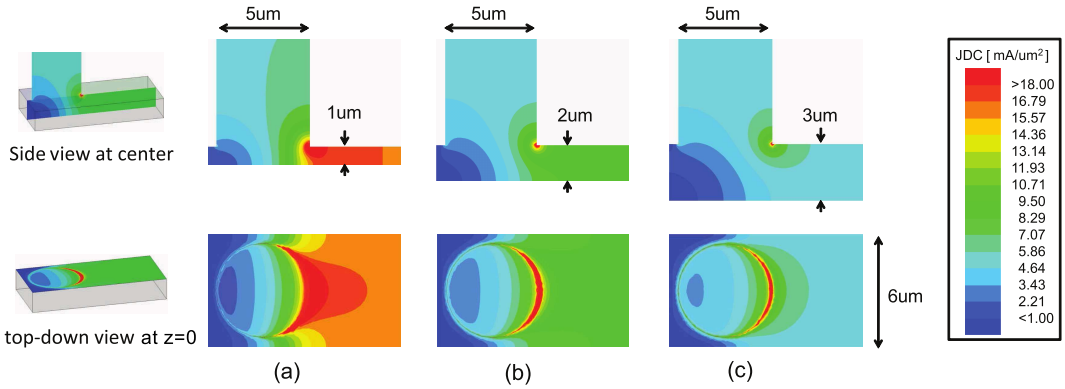

Fig. 3. Ratio of the TSV diameter to the wire thickness affects the current crowding at the connection corner. The TSV diameter is set to 5 μm. The wire width is 6 μm, and the wire thickness increases from (a) 1 μm to (b) 2 μm and (c) 3 μm.

For this example, two current sources are connected at the top-left corner, each sourcing 50 mA. The current sink is the wire at the bottom-right corner. In a real 3-D PDN, power wires typically connect to landing pads from both directions. This test case constrains the current flow direction and allows us to use the simplest possible geometry for investigating the current density distribution in the TSV and its connection to the PDN. ANSYS Q3D Extractor [19] is used to simulate the dc current density distribution and the voltage drop.

The magnitude of current density is plotted for several cross-sections in Fig. 2(b) and (c). In Fig. 2(b), the majority of the current carried by the power wires dives into the top-left edge of the TSV and flows out at the bottom-right edge. In the current crowded corners, the current density reaches over 10 mA/μm^2 nearly twice as large as the average current density which is calculated to be 5.1 mA/μm^2. The current density distribution along the ZY plane shows significant current crowding, which is approximately 4 μm into the TSV from both the top and bottom interfaces in Z direction. In the center region of the TSV (4 μm < Z < 26 μm), the current is distributed extremely uniform across XY cuts of the TSV. Fig. 2(c) shows the magnitude of current density distribution in the XY planes, for Z = 30.0 μm, 29.0 μm, 1.0 μm, and 0.0 μm.

B. TSV Diameter to Wire Thickness Ratio

The amount of current crowding depends on the relative ratio of the TSV diameter to the power wire thickness. The smaller the TSV diameter to wire thickness ratio is, the larger the current crowding at the corners. Fig. 3 shows current density distributions where the TSV diameter is fixed at 5 μm and the wire thickness is changed from 1 μm, 2 μm, to 3 μm. The same structure used in Section III-A is used again here. For thicker wires, a significant amount of the current is shunted across the top of the TSV and through the top wire, whereas for thinner wires, a larger fraction of the current flows tightly around the corner and into the TSV. This is due to the lower resistive path of a thick wire compared with that of a thin wire. For the cases having the same TSV diameter to wire thickness ratio, similar current density distributions will be expected. For example, similar scaled current density distributions are observed for both the 5-μm diameter 1-μm wire thickness and the 10-μm diameter 2-μm wire thickness.

The maximum current density within the TSV due to crowding is shown in Table I. As the TSV diameter is varied from 16 μm to 2 μm, the wire width correspondingly decreases from 18 μm to 3 μm. The wire thickness is held constant at 2 μm, and the input current is held constant at 100 mA. As the TSV diameter decreases, the maximum current density due to crowding changes from more the

TABLE I
IMPACT OF THE TSV DIAMETER ON THE CURRENT CROWDING. THE TSV DELIVERS 100-mA CURRENT, AND THE WIRE THICKNESS IS 2 μm

	case1	case2	case3	case4	case5
TSV diameter (um)	16	8	5	4	2
TSV height (um)	48	48	30	24	12
Wire width (um)	18	10	6	5	3
J_{avg}(mA/um^2)	0.5	2.0	5.1	8.0	31.8
J_{max}(mA/um^2)	5.5	10.4	19.2	25.8	62.0
J_{max}/J_{avg}	11.1	5.2	3.8	3.2	2.0
TSV diameter: wire thickness	8:1	4:1	2.5:1	2:1	1:1

TABLE II
IMPACT OF CURRENT CROWDING ON VOLTAGE DROP THROUGH A TSV. THE THICKNESS OF POWER WIRE VARIES FROM 1 μm TO 3 μm

Wire thickness (um):	1.0	2.0	3.0
voltage drop w/ current crowding (mV)	3.33	3.11	3.02
voltage drop w/o current crowding (mV)	2.75	2.75	2.75
Increase by current crowding (%)	21.1	13.1	9.8

10 times the average current density to just two times the average current density. The decrease of J_{max}/J_{avg}, for smaller TSV diameters, indicates that J_{max} increases slower than J_{avg} when the TSV diameter decreases and the connecting wires are with the same thickness. In other words, the current crowding phenomenon is smaller for the case of small diameter TSVs and thick wires compared with the large diameter TSVs and thin wires. EM checking tools should include these effects for accurate PDN analysis.

C. Impact of Current Crowding on IR Drop

Current crowding inside the TSV changes the effective resistance of the TSV as well as the voltage drop across the TSV. The spreading resistance [20] is caused by the nonparallel current paths between two spatially separated contacts. Due to current crowding, the effective resistance of the TSV is larger than the value obtained using $R_0 = \rho \cdot l/A$ where ρ is the resistivity, l is the length, and A is the cross-sectional area of the TSV.

We use ANSYS Q3D to calculate the voltage drop across the TSV taking into account the spreading resistance. For this set of simulations, we hold the TSV dimensions constant and increase the power wire thickness from 1 μm to 3 μm. The resulting voltage drop through the TSV is shown in Table II. For the case assuming uniform current density and 100-mA total current, the voltage drop across the TSV, $V_0 = \mathrm{IR}_0$ is 2.75 mV, and is not sensitive to the wire thickness. However, for the actual case having nonuniform current density, the voltage across the TSV is sensitive to the wire thickness. As the power wire thickness increases from 1 μm to 3 μm, the voltage drop decreases from 3.33 mV to 3.02 mV, corresponding to 21.1% to 9.8% greater voltage drop than the calculated value.

D. Power-Wire-to-TSV Interface

The current density gradient not only occurs at the TSV interface and within the TSV, but also along the power wires connected to the TSV landing pad as shown in Fig. 4. Far from the wire to TSV connection, the current density inside power wires is relatively uniform. Along the wires in the transition region approaching the TSV interface, the current density can become highly nonuniform, especially for the case where multiple power wires connect to the landing pad as indicated in Fig. 4.

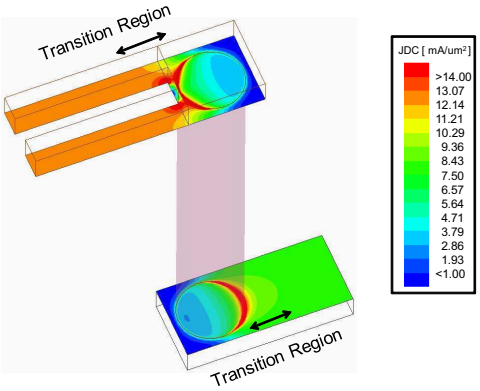

Fig. 4. Current crowding in the power-wire-to-TSV interfaces.

IV. TSV CURRENT CROWDING MODEL

Commercial FEM tools provide accurate simulation on current density distribution. However, using a FEM tool for chip-scale PDN analysis requires very large runtime and computational resources. Simulations on a single TSV can take up to 1 h. A more efficient approach is required.

In traditional PDN modeling, power wire segments and TSVs are modeled as single resistors. This model can only represent uniform current density within a wire segment or a TSV, and is insufficient to accurately capture nonuniform current distributions caused by current crowding. Likewise, it is also insufficient to accurately calculate voltage drop related to the spreading resistance due to current crowding. Here, we describe a simple TSV model which allows modeling of nonuniform current densities within a TSV and the TSV to wire transition regions. The models have been integrated into chip-scale PDN netlists and are simple enough that runtime remains reasonable. A PSIM [21] is then used to solve the power resistance network and analyze current and voltage.

A. 3-D Resistance Network for TSV Modeling

An illustration of the TSV model and the corresponding resistance network is shown in Fig. 5. The TSV model is constructed using rectangular mesh boxes having the structure shown in Fig. 5(a). These rectangular mesh boxes connect with the neighboring boxes using the center-lines as connection points. Each mesh box consists of six resistors: R_{east}, R_{south}, R_{west}, R_{north}, R_{up}, and R_{down} shown in the zoom-in mesh box of Fig. 5(a). The values for these resistors depend on the geometry of each mesh box and how the TSV overlays the box, which will be discussed in Section IV-B.

The 3-D mesh structure of a TSV is composed of two interconnecting orthogonal meshes: a Z-mesh and an XY-mesh. Along the Z direction, the Z-mesh divides the TSV into multiple short cylinders with varying thicknesses. Each short cylinder is then meshed into a 2-D XY-mesh on a virtual

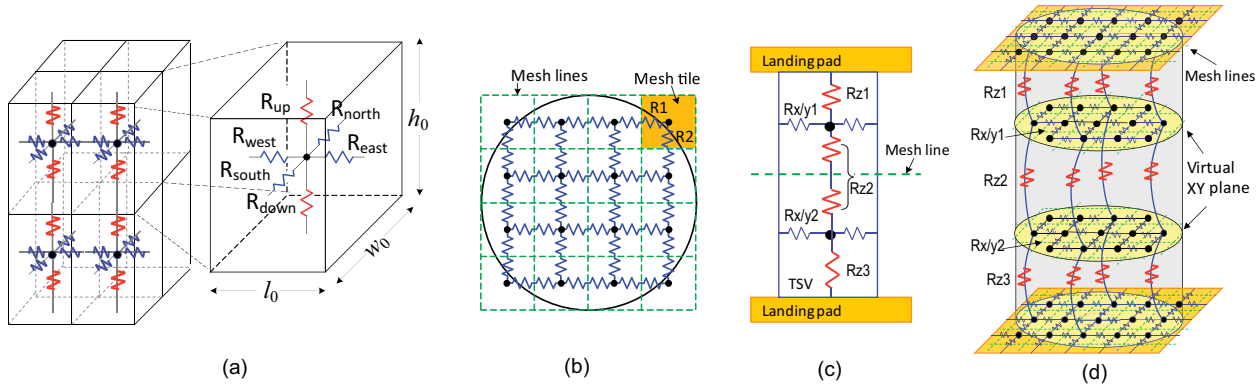

Fig. 5. TSV modeling approach of a 3-D resistance network. (a) Basic rectangular boxes after 3-D meshing. (b) XY-mesh with TSV boundary overlay. Mesh tiles over the TSV boundary partially overlap the actual TSV. (c) Side view. (d) 3-D view of the network.

XY plane located at the center of each cylinder. The resulting model is a nonuniform 3-D resistance network consisting of two types of resistors. The first are resistors along Z-axis [R_{Z1}, R_{Z2}, and R_{Z3} in Fig. 5(c) and (d)] connecting neighboring virtual XY planes. The second are resistors in virtual XY planes [$R_{x/y1}$ and $R_{x/y2}$ in Fig. 5(c) and (d)]. Fig. 5(d) is a schematic in nature. Only two virtual planes and resistors are shown for readability.

The Z locations of XY-planes, referred to as the Z-mesh, are determined by the current gradient in the ZY-plane shown in Fig. 2(b). More cylinders are created in the regions having nonuniform current density (TSV top and bottom) and fewer in the regions of uniform current density (TSV center). The Z-mesh used in the model is a tradeoff between accuracy and runtime. The 30-μm tall TSV was partitioned at Z = 0.0, 0.1, 0.4, 0.9, 2.0, 5.0, 16.0, 27.0, 28.9, 29.4, 29.7, 29.9, 30.0, where the TSV bottom is at Z = 0. Three different XY-mesh sizes were implemented, 0.25 μm. 0.5 μm, and 1.0 μm to check for accuracy and convergence.

B. Modeling of the Basic Rectangular Mesh Box

In general, the resistance of a rectangular box can be expressed as

$$R = \frac{\rho \times l_{\text{eff}}}{w_{\text{eff}} \times h_{\text{eff}}} \tag{1}$$

where ρ is the resistivity of the material, and l_{eff}, w_{eff}, h_{eff} are the effective length, width, and height of the box, respectively.

If a mesh tile is completely covered by the actual TSV geometry, the six resistors in Fig. 5(a) are directly obtained referring to the dimensions of the mesh box:

1) for R_{east} and R_{west}, $l_{\text{eff}} = l_0/2$, $w_{\text{eff}} = w_0$, $h_{\text{eff}} = h_0$;
2) for R_{south} and R_{north}, $l_{\text{eff}} = w_0/2$, $w_{\text{eff}} = l_0$, $h_{\text{eff}} = h_0$;
3) for R_{up} and R_{down}, $l_{\text{eff}} = h_0/2$, $w_{\text{eff}} = l_0$, $h_{\text{eff}} = w_0$.

where w_0, l_0, h_0 are the width, length, and height of the mesh box determined by the XY-mesh and Z-mesh.

Around the TSV boundary, some mesh tiles only partially overlap with the actual TSV geometry as shown in Fig. 5(b). For this case, the TSV-mesh overlap area is calculated as the cross-sectional area in the XY plane (A_{TSV}) for R_{up} and R_{down} calculation

$$R_{\text{up}} = R_{\text{down}} = \frac{\rho \times h_0/2}{A_{\text{TSV}}}. \tag{2}$$

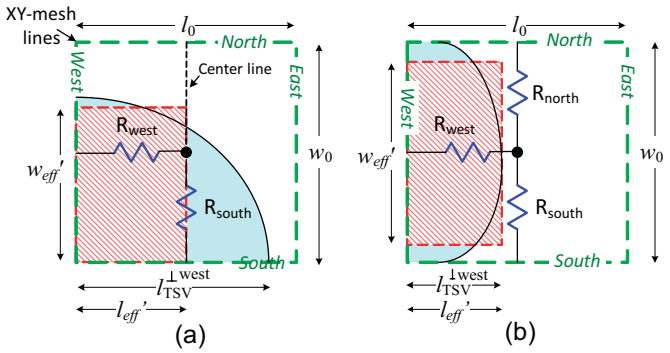

Fig. 6. Modeling of resistor R_{west} for partial overlap mesh tiles. (a) Case I: the TSV (in blue) overlaps with the XY-mesh lines south and west. (b) Case II: the TSV overlaps with the XY-mesh lines south, west, and north. The effective bounding box for R_{west} is shown in red.

If an XY mesh line dir crosses the TSV geometry, where dir $\in$ {east, south, west, north}, Resistor R_{dir} is added in the mesh box. Corresponding to R_{dir}, the TSV-mesh overlap, which is bounded by the mesh line dir and its parallel center line, is modeled as an effective rectangular bounding box. The effective length (l'_{eff}) and width (w'_{eff}) for R_{dir} calculation are expressed as follows:

$$l'_{\text{eff}} = \min\left\{l_{\text{eff}}(R_{\text{dir}}),\ l_{\text{TSV}}^{\perp\text{dir}}\right\} \tag{3}$$

$$l'_{\text{eff}} \times w'_{\text{eff}} = A_{\text{TSV}}^{\text{dir-center}} \tag{4}$$

where $l_{\text{eff}}(R_{\text{dir}})$ is the effective length of Resistor R_{dir} when the TSV fully covers the mesh tile, for instance, $l_{\text{eff}}(R_{\text{west}}) = l_0/2$. $l_{\text{TSV}}^{\perp\text{dir}}$ is the maximum length of the TSV-mesh overlap in the direction perpendicular to the mesh line dir. And $A_{\text{TSV}}^{\text{dir-center}}$ is the area of the TSV-mesh overlap region, which is in between the mesh line dir and the center line parallel to this mesh line.

The value for R_{dir} is calculated as

$$R_{\text{dir}} = \frac{\rho \times l'_{\text{eff}}}{w'_{\text{eff}} \times h_0/2}, \quad \text{dir} \in \{\text{east, south, west, north}\}. \tag{5}$$

Two examples of modeling R_{west} are depicted in Fig. 6, when the TSV and the XY-mesh tile are partially overlapped. The effective rectangular bounding box for R_{west} is shown in red.

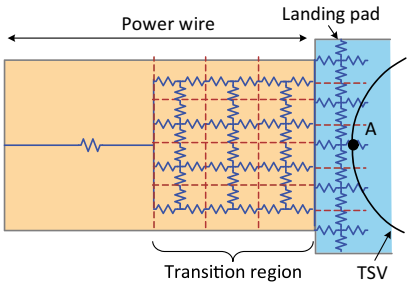

Fig. 7. Meshing the transition region. Using a single resistor in the transition region would incorrectly lead to all of the current being injected into Point A.

C. Modeling of the Transition Region

The transition region is the connection area between the power wires and the TSV landing pad. Nonuniform current gradients can occur in the transition region as shown in Section III-D. It is important to include a meshed version of the transition region in the model in order to simulate the local current density distribution between the power wire and the landing pad. By doing so, current crowding at the TSV-wire interface as well as the TSV effective resistance can be simulated accurately in the context of chip-scale PDN analysis.

An example of meshing in the transition region is shown in Fig. 7, where nonuniform current gradients can occur at the connections between power wires and TSV landing pads. Although the total current flowing into the transition region is equal to that out of the region, the local current density at the landing pad and the TSV edge depends on the meshing structure. Without meshing the transition region, the entire current would flow into the single Point A, which would result in a large, but incorrect, current at the edge of the TSV. By meshing the transition region, the current is not constrained to flow only into Point A but rather is allowed to redistribute as needed to satisfy the equations describing the network.

The length of the transition region and the corresponding mesh granularity affects the modeling accuracy. Modeling a long transition region with a fine grain mesh gives greater accuracy at the expense of larger computational resources. Determination of the transition region length should consider the amount of current crowding at the TSV–wire interface, which as discussed previously, is affected by the dimensions of the TSV, wire thickness, and power wire geometry. For our test case, where the landing pad is 6 μm $\times$ 6 μm and the TSV diameter is 5 μm, a transition region approximately 6-μm long was found to be long enough to adequately model the transition region. A length comparable to the TSV landing pad is a reasonable starting point.

D. Modeling Accuracy

Detailed comparisons between ANSYS Q3D and PSIM using the simplified discrete TSV model are shown in Fig. 8. The current distributions are generated as follows. For the ANSYS Q3D results, we first simulate the current gradient using the internal mesh generator and solver. Next, the current values are mapped into an XY-mesh with granularity of 0.25 μm for any fixed Z. For the PSIM results, we

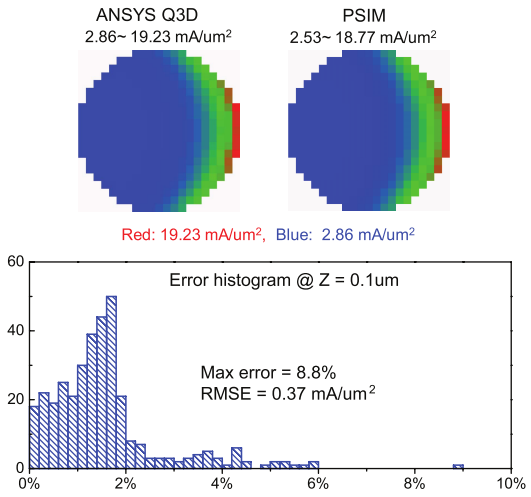

Fig. 8. Current density distributions and the error histogram of ANSYS Q3D and our TSV modeling approach in PSIM at Z = 0.1 μm virtual XY plane.

generate a discrete resistor model using an XY-mesh size of 0.25 μm. The network is then simulated using PSIM. Finally, the current for each mesh tile is extracted and current density is calculated. The current density distribution from ANSYS Q3D and PSIM is plotted for comparison in the top half of Fig. 8. These results are plotting across an XY plane cutting the TSV at Z = 0.1 μm, where the largest current crowding is observed. The corresponding error histogram of the two current densities for all 357 tiles is shown at the bottom of Fig. 8. Here, the error for each tile is defined as the absolute difference between ANSYS Q3D and PSIM.

ANSYS Q3D and PSIM results are in very good agreement. The relative error for each tile is less than 10%, and most are within 5%. The root-mean-square error (RMSE) is 0.36 mA/μm^2, defined as the square root of the arithmetic mean of the square of the error for each tile

$$\sqrt{\left(\sum_{i=1 \text{ to } n}\left(J_i^{\text{Q3D}} - J_i^{\text{PSIM}}\right)^2\right)/n}$$

where i is the ith tile and n is the total number of tiles. The voltage drop from ANSYS Q3D is 3.08 mV and PSIM is 3.07 mV.

Differences between ANSYS Q3D and PSIM are mainly due to constraining the XY-mesh and Z-mesh sizes. While we use low density orthogonal meshing boxes for simplicity, ANSYS Q3D supports more sophisticated meshing structures, such as triangular and tetrahedral shapes. However, PSIM takes less than one s simulation time, whereas ANSYS Q3D takes up to 1 h. This demonstrates that our modeling approach has potential for chip-scale power analysis with reasonable accuracy and acceptable runtime.

The Z-mesh granularity also determines the final accuracy and runtime. As mentioned earlier, a nonuniform partition along the Z direction has been applied, where Z = 0.0, 0.1, 0.4, 0.9, 2.0, 5.0, 16.0, 27.0, 28.9, 29.4, 29.7, 29.9, 30.0. Since current crowding mainly occurs at the TSV-to-wire interfaces, more XY planes (finer Z-mesh granularity) is required to capture these detailed current density distributions. Since the

TABLE III
IMPACT OF THE XY-MESH SIZE ON THE CURRENT DENSITY (mA/μm^2) AND THE VOLTAGE DROP (mV)

mesh (um)	#tiles	Max. Current density RMSE	ANSYS Q3D	PSIM	err (%)	Voltage drop ANSYS Q3D	PSIM	err (%)
0.25	4641	0.25	19.2	18.8	-2.1	3.1	3.10	0.3
0.5	1313	0.34	18.0	20.8	15.6	3.1	3.09	0.7
1.0	325	0.55	12.2	15.6	27.9	3.1	2.99	3.9
–	1	–	19.2	5.1	73.4	3.1	2.75	11.3

current is uniform in the TSV center, fewer XY planes (coarse Z-mesh) are required. Of course, adding more XY planes will improve the accuracy, but at the same time increase the overall simulation time.

E. Impact of XY-Mesh Size

The impact of varying the XY-mesh size on the accuracy of current density and voltage drop is shown in Table III. Here, the Z-mesh is held constant and the XY-mesh size is increased from 0.25 μm, 0.5 μm, to 1.0 μm.

As the mesh tile size is increased, the RMSE of the current density increases from 0.25 mA/μm^2 to 0.55 mA/μm^2, which corresponds to a 4.9% to 10.7% increase compared with the average current density. To find the maximum current density in ANSYS Q3D for a given mesh size, the ANSYS Q3D simulation result must be mapped into each corresponding mesh tile. With increasing mesh tile size, the maximum current density of ANSYS Q3D decreases, the error of the maximum current density increases from 2.1% to 27.9%, and the voltage drop error increases from 0.3% to 3.9%. The cost of using a finer mesh size is that the total number of mesh tiles increases from 325 to 4641. Although this is not a significant increase in simulation time for a single TSV, it is for a chip-scale PDN containing a large number of TSVs. Simulation results using a single resistor are reported in the bottom row of the table. For this case, the errors are quite large compared with ANSYS Q3D. The average current density is 73.4% smaller and voltage drop is 11.3% smaller.

V. CHIP-SCALE 3-D PDN ANALYSIS

In this section, the discrete resistor TSV model proposed above is integrated into the chip-scale power grids. PSIM is then used to analyze the global PDNs which have high current density and contain TSV connections.

A. Chip-Scale PDN Circuit Model

A schematic representation of a small section of a 3-D PDN for two dies is illustrated in Fig. 9. Global power wire segments and local vias are represented as lumped resistors. The 3-D power connection, including TSVs and transition regions, is included using the proposed models. We assume ideal voltage source of 1 V supplied from C4s. The current sinks are located at the intersections of the power grids in each die. Power wires used for these simulations are 2-μm thick and 5-μm wide. The TSV has 30-μm height, 5-μm diameter, and 6 μm $\times$ 6 μm landing pads.

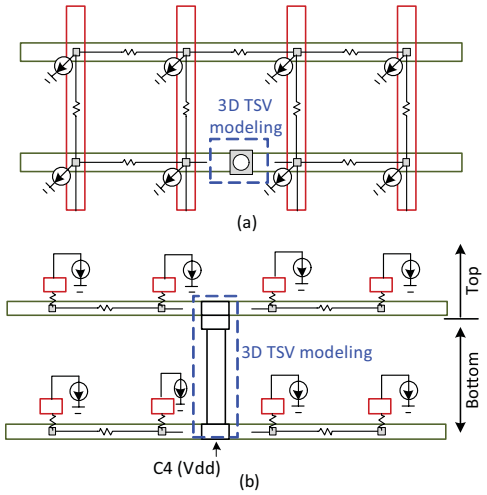

Fig. 9. Circuit model for a two-die TSV-based PDN using the proposed 3-D TSV modeling approach in (a) top-down view and (b) side view.

B. Simulation Results

The global PDN and the power maps in the top and bottom dies are shown in Fig. 10(a) and (b), respectively. The die footprint is 1.4 mm $\times$ 1.4 mm. Each die has a 16 $\times$ 16 array of power wires (purple and yellow) and a thick power ring around the boundary having a width of 15 μm. A 4 $\times$ 4 array of TSVs and C4s is centered in the bottom die. The elements of this array are enlarged as the white blocks for readability. Black boxes at the intersection of power wires represent the current sinks. The TSV model has an XY-mesh of 0.25 μm, and the Z-mesh identical to the one described in Section IV-A.

Power maps for both bottom die (S1) and top die (S2) have a cool spot in the bottom-left corner and a hot spot in the top-right corner. In the center of each die, another two narrow cool spots are placed in the left and right. In the bottom die, the power density is arbitrarily increased from bottom to top and from left to right. And the power map of the top die is a rotation of the power map of the bottom die along 45° diagonal. These power maps result in different current density patterns connecting to the TSVs: 1) symmetric current density, e.g., TSV1 in Fig. 10(b), where all the power wires have high current density and 2) asymmetric current density, e.g., TSV2 in Fig. 10(b), where left power wires have much lower current density than the right power wires.

The voltage drop maps in top and bottom dies are shown in Fig. 10(c) and (d). The top-right corner has the maximum IR drop: 23.0 mV in top and 19.0 mV in bottom. The IR drops in S2 are larger than S1 due to the TSV parasitic resistance. Since TSVs and C4s are aligned, the region closer to TSVs has a smaller IR drop than the region far from TSVs.

Detailed current density distribution in TSV1 and TSV2 in the XY direction (J_{XY}) and Z direction (J_Z) are plotted in Fig. 11. J_{XY} in metal layers S2-M10, S1-BM, and S1-M10 are plotted in Fig. 11(a), (c), and (f), respectively. Fig. 11(b), (d), and (e) plots J_Z through the interface between S1-BM and S2-M10, the top surface of the TSV, and the bottom surface of the TSV, respectively.

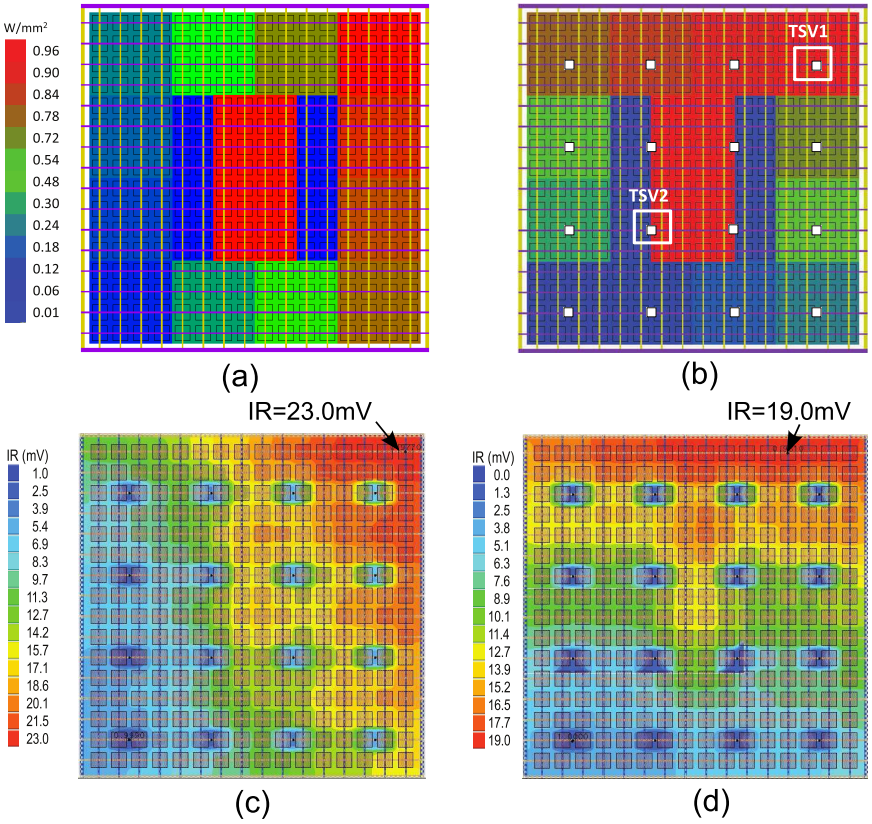

Fig. 10. Power density maps of the (a) top die and (b) bottom die, where TSVs and C4s are aligned and enlarged for readability. Voltage drop map of the (c) top die (max = 23.0 mV), voltage drop map of the (d) bottom die (max = 19.0 mV).

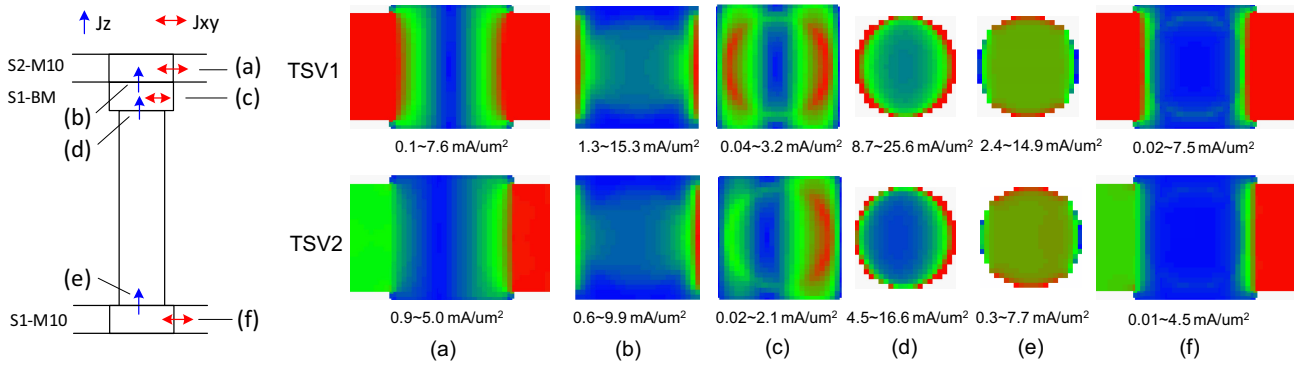

Fig. 11. Current density distribution in XY (J_{XY}) and Z (J_Z) direction of TSV1 and TSV2 in Fig. 10. TSV1 has symmetric current density along power wires; TSV2 has asymmetric current. (a) J_{XY} in metal layers S2-M10, (b) J_Z through the interface between S1-BM and S1-M10, (c) S1-BM, (d) top surface of the TSV, (e) bottom surface of the TSV, and (f) S2-M10.

PSIM can effectively capture the detailed current density distribution inside the 3-D power connection. First, while symmetric current crowding is observed in both edges of TSV1, most of the current crowding occurs at the right edge of TSV2. Second, large current crowding inside TSVs is observed. For TSV1, the maximum current density (J_{max}) in Fig. 11(a) is 7.6 mA/μm^2, where most current concentrate at the connection between the power wire and the landing pad. The current density, J_{max}, through the TSV in Z-direction [Fig. 11(d)] is 25.6 mA/μm^2, which is approximately 2.4 times larger than the wire J_{max}. Third, larger current crowding occurs at the TSV top surface compared with the bottom surface due to the alignment of the TSVs and C4s. The current density, J_Z, flowing through the TSV bottom surface [Fig. 11(e)] is 14.9 mA/μm^2 compared with the top surface of 25.6 mA/μm^2. Fourth, in the bottom TSV surface [Fig. 11(e)], J_Z current crowds at the top and bottom edges instead of concentrating at the left and right edges. This is because large amount of J_{XY} currents flow out from the left and right edges to feed the S1 current sinks. As a result, the current, delivered to the S2 power grid, concentrates at the top and bottom edges. Moreover, current crowding leads to 5.7 mV IR drop through TSV1, which is 3.7% larger than the IR drop without considering the crowding value of 5.5 mV.

In the next sections, the following results are discussed:

1) maximum current density (J_{max}) along the power wires;
2) maximum and average current density (J_{avg}) of the

TABLE IV
IMPACT OF THE TSV MESH SIZE ON CURRENT DENSITY (mA/μm^2) AND IR DROP (mV)

Power grid	#TSV &#C4	Mesh (um)	TSV (um)	Wire	TSV with max(J_{max})			J_{inc} (%) of TSVs			IR_{Bottom}			IR_{Top}		
				J_{max}	J_{max}	J_{avg}	J_{inc}(%)	min	avg	max	min	avg	max	min	avg	max
16×16	4×4	0.25	5	10.5	25.6	10.2	151	151	161	192	2.1	9.5	19.1	3.8	12.7	23.0
16×16	4×4	0.50	5	10.4	20.2	10.1	100	100	105	124	2.4	10.0	19.8	4.1	13.3	23.7
16×16	4×4	1.00	5	10.5	14.3	10.2	41	41	42	48	2.1	9.4	18.9	3.9	12.9	23.1

TABLE V
IMPACT OF THE TSV DIAMETER (μm) ON CURRENT DENSITY (mA/μm^2) AND IR DROP (mV)

Power grid	#TSVs &#C4s	Mesh (um)	TSV (um)	Wire	TSV with max(J_{max})			J_{inc} (%) of TSVs			IR_{Bottom}			IR_{Top}		
				J_{max}	J_{max}	J_{avg}	J_{inc}(%)	min	avg	max	min	avg	max	min	avg	max
16x16	4x4	0.25	4	10.5	33.5	15.7	113	109	113	117	2.2	9.5	19.2	4.3	13.6	24.1
16x16	4x4	0.25	5	10.5	25.6	10.2	151	151	161	192	2.1	9.5	19.1	3.8	12.7	23.0
16x16	4x4	0.25	8	10.4	19.0	4.0	372	372	394	463	2.3	9.9	19.7	3.3	11.8	21.7
16x16	4x4	0.25	16	10.7	10.6	1.0	928	928	986	1177	2.2	9.5	19.2	2.3	9.8	18.8

TABLE VI
IMPACT OF TSV AND C4 OFFSET ON CURRENT DENSITY (mA/μm^2) AND IR DROP (mV) THROUGH TSVS

	# TSVs	# C4s	Wire	TSV with max(J_{max})			J_{inc}(%) of TSVs			IR_{Bottom}			IR_{Top}			TSV w/ max(IR)			Inc (%) of TSV IR		
			J_{max}	J_{max}	J_{avg}	J_{inc}(%)	min	avg	max	min	avg	max	min	avg	max	IR_c	IR_n	Inc.(%)	min	avg	max
Aligned	16	16	10.5	25.6	10.2	151	151	161	192	2.1	9.5	19.1	3.8	12.7	23.0	5.7	5.5	3.7	3.4	4.0	5.2
Offset	16	12	25.2	22.0	8.3	165	149	164	190	10.2	26.5	48.3	29.7	46.7	65.5	4.8	4.5	6.4	5.9	8.0	10.6

TSVs. For multiple TSVs, J_{max} and J_{avg} through each TSV are first measured. The percentage increase (J_{inc}) of J_{max} over J_{avg} for each TSV is then calculated as $J_{inc} = (J_{max} - J_{avg})/J_{avg}$;

3) min/max/avg IR drops in top and bottom dies;
4) IR drop through the TSVs. Two values for the IR drop are reported. The first, IR_c, is calculated, including current crowding, and the second, IR_n, is calculated using the average current without current crowding. The baseline PDN design contains a 16 × 16 power grid on each die, 4 × 4 TSVs and C4s, and TSVs with 5-μm diameter and 0.25-μm mesh size.

C. Impact of TSV Mesh Size

In this section, we increase the mesh size of the TSV model from 0.25 μm, 0.5 μm, to 1.0 μm, keeping the rest of the design fixed. The effect of the mesh size variation on the current density and the IR drop are shown in Table IV. First, notice using a larger mesh size in the TSV model results in lower J_{max} in each mesh tile compared with using a finer mesh size. As the mesh size increases from 0.25 μm to 1.0 μm, J_{max} decreases from 25.6 mA/μm^2 to 14.3 mA/μm^2 and J_{inc} decreases from 151%–192% to 41%–48%. Second, the mesh size does not affect the IR drop of the power grid and wire J_{max} very much. In contrast, significant current crowding is observed in the TSVs for smaller mesh sizes. For the mesh size of 0.25 μm, the J_{max} in the TSV is 25.6 mA/μm^2, which is 110% larger than the TSV J_{avg} of 10.2 mA/μm^2.

D. Impact of TSV Diameter

Starting from the baseline PDN design and power maps described in Section V-B, we increase the TSV diameter from 4 μm, 5 μm, 8 μm, to 16 μm, with mesh size of 0.25 μm, 0.25 μm, 0.5 μm, and 0.5 μm, respectively. Other design factors are fixed. The simulation results of current density and IR drop are shown in Table V. We observe that larger TSVs significantly reduce J_{avg} from 15.7 mA/μm^2 to 1.0 mA/μm^2 and J_{max} of the TSVs from 33.5 mA/μm^2 to 10.6 mA/μm^2. However, J_{max} of TSVs decreases slower than J_{avg} of TSVs. As a result, for the 16-μm diameter TSVs, J_{max} of TSVs is 930%–1180% larger than J_{avg} of the TSVs. For these designs, the TSV diameter only affects IR drops in the top die. IR drops in the bottom die are insensitive to the TSV diameter, where the voltage is directly supplied by C4s from the package. The top die has lower IR drops when using larger TSVs, which is due to the reduced TSV effective resistance and the IR drop through TSVs.

E. Impact of TSV and C4 Offset

Previous simulations assume aligned TSVs and C4s. To study the offset impact on power integrity, we leave 175-μm distance between the TSV and the C4. The offset design has 12 C4s and 16 TSVs. The simulation results are shown in Table VI.

Current crowding has a larger impact on TSV IR drop in the offset design than the aligned design. In Table VI, the second major column from the right compares the IR drop through the TSV for the case with current crowding, IR_c, and without current crowding, IR_n. In the offset design, the values for IR_c are 5.9%–10.6% larger than the values for IR_n. For the aligned design, the values for IR_c are 3.4%–5.2% larger than the values for IR_n. This is mainly because large current crowding occurs in both the top and bottom surfaces of TSVs in the offset design. On the other hand, for the aligned design, only the top interface between the TSV and the backside Metal exhibits large current crowding. Here, the voltage at the bottom interface between TSV and S1-M10 is constantly supplied by C4s.

F. 3-D Power Integrity on Large-Scale PDNs

In this section, five large-scale two-die stacked PDNs are used for 3-D power analysis using PSIM. The power wire

TABLE VII
3-D POWER INTEGRITY ANALYSIS FOR LARGE-SCALE PDNS. WE SHOW THE FOOTPRINT (mm^2), POWER DENSITY (W/mm^2), CURRENT DENSITY ($mA/\mu m^2$), AND IR DROP (mV)

Design	Footprint	Pwr dens.		Power	#TSVs	#C4s	J_{max}_wire		TSV with max(J_{max})			IR_{Bottom}			IR_{Top}			TSV with max(IR)		
		top	bot	grid			top	bot	J_{max}	J_{avg}	J_{inc}(%)	min	avg	max	min	avg	max	IR_c	IR_n	Inc.(%)
PDN1	5×5	0.57	0.57	50×50	144	144	7.0	7.2	9.6	6.8	41	5.1	8.7	15.9	7.9	11.7	19.6	4.1	3.7	11.4
PDN2	6×6	0.40	0.75	60×60	225	225	3.5	6.6	5.0	3.6	40	6.0	9.9	13.3	5.0	7.2	9.2	2.1	1.9	11.4
PDN3	9×9	0.80	0.80	90×90	484	484	13.6	12.1	18.5	13.1	41	4.4	11.3	24.2	6.8	15.6	37.8	7.9	7.1	11.5
PDN4	11×11	0.71	0.91	110×110	729	729	8.7	11.4	11.1	7.5	47	8.1	12.8	25.2	9.7	13.5	24.2	5.1	4.5	11.4
PDN5	15×15	0.47	0.49	150×150	1369	1369	16.2	17.4	23.3	16.3	43	1.8	6.8	34.9	2.7	8.8	49.6	9.9	8.8	12.2

utilization, defined as the power wire area per level per supply per die over the die area, is set to 5%. Assuming the bottom die needs $N_P \times N_P$ power wires, and the TSVs and C4s are placed every fourth wire, the TSV and C4 counts are $(25\%N_P) \times (25\%N_P)$. The power TSVs have 5-$\mu$m diameter with 1.0-$\mu$m mesh size. Power wires have 5-μm width and 2-μm thickness. The local and global power density maps are taken from various published 3-D core-to-memory PDN designs [15], [14], a microprocessor, and power density estimation from International Technology Roadmap for Semiconductors (ITRS) 2005 [22].

The results of power analysis on large-scale PDNs are tabulated in Table VII. First, J_{max} through the TSVs carrying the largest currents is 40%–47% larger than the J_{avg} through the same TSV. As previously discussed, using a coarser mesh size generally underestimates J_{max} on 3-D power connection compared with using finer mesh or using FEM tools. Therefore, it is likely that the actual peak current density is even greater. In a case like this, where greater accuracy may be of interest at a particular location, a model having a smaller mesh size could be used in that location. Second, the wire J_{max} in S1 and S2 depends on the power density of each die, where larger power density (PDN2 and PDN4) in the bottom die results in comparable J_{max} between wires and TSVs; for other designs with lower power density in the bottom die, TSV J_{max} is 13% larger than wire J_{max}. Third, current crowding also increases the IR drop through the TSVs, which is 11.4%–12.2% larger than the IR drop without considering current crowding. Moreover, IR drops in S1 and S2 power grid are also affected by the power density in each die. When each die has comparable power density, the maximum IR in the top die is usually larger than the bottom die; allocating the high power density close to C4s (in the bottom die) helps to reduce the IR drops in the top die.

From the PDN analysis described above, we have demonstrated that power simulation with discrete TSV models integrated into the global PDN netlist can be used to analyze chip-scale 3-D PDNs. Using this methodology, detailed local information regarding the current density distribution and its impact on the voltage drop is now available. This allows the 3-D PDN designer to obtain feedback to assess, correct, and optimize the design. The power simulator can be set up to select different mesh sizes depending on the required resolution of the power analysis. For example, for a large PDN, initially a large mesh size can be used globally to identify the areas of concern associated with hotspots of maximum current density and IR drop. Then for these locally bounded hotspots, the large mesh size models can be replaced with fine mesh size models. In this way, models with different mesh sizes can be used to give different levels of accuracy or resolution analogous to how the different objectives on a microscope give different magnifications.

VI. CONCLUSION

Power integrity analysis, including detailed current density distribution and IR drop is of importance for 3-D PDN design. In this paper, we analyzed and modeled the dc current density distribution inside the TSVs and at the TSV-to-wire connections, implemented discrete resistor models of the TSV and its connecting wires, and integrated these models into global 3-D PDNs for analysis.

The dc current density distribution inside the TSVs and at its local connections to the global wires was extensively analyzed. We observed significant current crowding both near the TSV-wire connections and inside the TSV, which can extend several microns deep into the TSV from the top and bottom surfaces. This current crowding depends on the relative ratio of the TSV diameter to the power wire thickness and increases the effective resistance of the TSV and the corresponding voltage drop compared with the calculations using average values. Discrete resistor models for TSVs and for TSV-wire transition regions were implemented and used to calculate the nonuniform current density distributions and effective voltage drops. The discrete resistor models have good accuracy and acceptable runtime. Furthermore, the mesh size can be tuned to favor either accuracy or runtime. These models were integrated into chip-scale 3-D PDNs, and detailed power integrity analysis was performed for several global 3-D PDNs using PSIM. This methodology can help designers to locate regions having high current density and large voltage drop caused by current crowding. We observed that both the current density and the voltage drop of PDNs can change significantly when current crowding was included. Finally, we studied how modeling and design parameters, such as mesh size, TSV diameter, and TSV/C4 alignment can affect 3-D PDNs.

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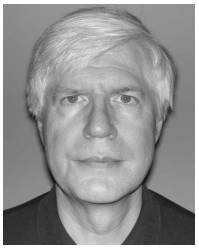

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