Impact of Mechanical Stress on the Full Chip Timing for Through-Silicon-Via-based 3-D ICs

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***Abstract*—In this paper, we study the impact of through-silicon-via (TSV) and shallow trench isolation (STI) stress on the timing variations of 3-D IC. We also propose the first systematic TSV-STI-stress-aware timing analysis and show how to optimize layouts for better performance. First, we generate a stress contour map with an analytical radial stress model for TSV. We also develop a stress model for STI from finite element analysis results. Then, depending on geometric relation between TSVs, STI, and transistors, the tensile and compressive stresses are converted to hole and electron mobility variations. Mobility-variation-aware cell library and netlist are generated and incorporated into an industrial engine for timing analysis of 3-D IC. We observe that TSV stress and STI stress interact with each other, and rise and fall time react differently to stress and relative locations with respect to both TSVs and STIs. Overall, TSV-STI-stress-induced timing variations can be as much as ±15% at the cell level. Thus, as an application to layout optimization, we exploit the stress-induced mobility enhancement to improve performance of 3-D ICs. We show that stress-aware layout perturbation could reduce cell delay by up to 23.37% and critical path delay by 6.67% in our test case.**

***Index Terms*—3-D IC, mobility variation, stress, TSV.**

I. Introduction

3-D IC stacking has gained tremendous interest for IC integration to reduce wire length and footprint. In addition, several dies manufactured by different process technologies can be integrated as one chip with 3-D integration. Through-silicon vias (TSVs) are inserted for wafer-to-wafer connection in 3-D ICs. Tungsten, polysilicon, and copper have been considered as fill material of TSVs. Because of low resistivity, copper is widely used for TSV fill. However, its coefficient of thermal expansion (CTE) differs from CTE of silicon which can cause silicon strain. At 20 °C, CTE of copper is $17\times10^{-6}\,\mathrm{K}^{-1}$, while CTE of silicon is $3\times10^{-6}\,\mathrm{K}^{-1}$. The CTE mismatch causes inevitable stress on silicon. Because copper electroplating and annealing temperature (250 to 350 °C) is higher than operating temperature, tensile stress appears on silicon [1] near TSV at regular operating temperature.

Tensile stress on silicon causes reliability problems such as cracking. In addition, the stress can change mobility of carriers. Therefore, TSV stress induced by CTE mismatch may cause timing violation if the cells on timing critical paths are negatively impacted by the stress. Tensile stress enhances electron mobility. However, hole mobility is either enhanced or degraded depending on stress and the transistor channel direction. Longitudinal (with respect to carrier flow) tensile stress reduces hole mobility, while transverse tensile stress increases the mobility [2]. When TSV-induced tensile stress is 100 MPa in the longitudinal direction, hole mobility degradation can be up to 7.2%, making pMOS transition slow. If the pMOS is on a timing critical path, it can cause unexpected timing violation, which is not detected by the current timing analysis flow.[1]

Another major stress source in ICs is shallow trench isolation (STI). The CTE of silicon dioxide, widely used material for STI fill, is $0.5\times10^{-6}\,\mathrm{K}^{-1}$ at 20 °C. Because it is lower than CTE of both silicon and copper; STI causes compressive stress on active region it surrounds. Oxidation and oxide densification for STI also take place at much higher temperature than TSV annealing temperature. Therefore, the compressive stress caused by STIs is not negligible. Longitudinal compressive stress enhances hole mobility, but degrades electron mobility. If an nMOS on a critical path experiences compressive stress, it can cause unexpected setup and hold time violation as well.

Several papers were published regarding the impact of TSV stress [3] or STI stress [4] on IC performance, but their impact was studied separately.[2] This is the first paper addressing the impact of combined stresses, to our best knowledge. Because TSV/STI stresses are layout dependent, we propose a design flow to analyze timing variation by both, and show its implications for layout optimizations during 3-D IC design.

First, we propose stress-aware static timing analysis (SA-STA) flow. The first step for SA-STA is to generate stress

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[1]The devices in 3-D ICs may experience additional timing changes from process variations. The combined effect of stress and process variations on circuit timing is out of the scope of this paper.

[2]Consideration of other stress enhancement methods such as SiGe is out of the scope of this paper.

map according to TSV/STI positions. Stress calculation is based on analytical model for TSV, a model developed from finite element analysis (FEA) simulation for STI, and linear superposition. Stress map is used to estimate hole and electron mobility variations. Since every cell has different mobility depending on stress and orientation between channel, TSV, and STI, we substitute each cell to another cell having the same topology but having different timing characteristics according to the estimated mobility changes. We incorporate our stress aware design and library to a commercial STA flow.

Next, we show that TSV/STI-induced stresses play an important role to optimize performance by adjusting cell locations to take advantage of enhanced mobility due to the combined stresses. Logic cells on critical paths must be placed such that the mobility inside their pMOS/nMOS is not degraded (if not enhanced) by either TSV- or STI-induced stress. Since hole- and electron-mobility contours are different, pMOS and nMOS should be optimized separately. If a pMOS in a cell is on a critical path, the cell becomes a critical cell for hole mobility optimization. An nMOS critical cell can be optimally placed using the similar procedure.

The contributions of this paper include the following.

1) We propose compact stress and mobility modeling to consider systematic timing variation caused by TSV stress for 3-D ICs.
2) We develop an STI stress model based on results from FEA simulation and a model for STI-stress-induced mobility variation. They allow us to study the impact of interaction between TSV/STI stresses on performance.
3) We show that TSV/STI stresses can change hole mobility significantly, e.g., from −20% to 26%, which was observed to cause more than 15% variation for single cell delay. Thus, it can deteriorate overall chip performance, and must be considered during STA and optimization.
4) This is the first paper dealing with combined stress-aware STA and layout optimization, to our best knowledge.

The rest of the paper is organized as follows. We introduce related work regarding strained silicon and stress impact in Section II. The overall SA-STA and layout optimization flow is shown in Section III. We propose compact mobility modeling for TSV in Section IV and STI in Section V. We present our methodology to handle both TSV and STI stresses simultaneously at the end of Section V. In Section VI, we consider the impact of biaxial TSV stress. In Section VII, we explain how to perform full-chip STA for 3-D ICs under both TSV and STI stresses. Experimental results are shown in Section VIII, and we conclude in Section IX.

II. Related Work and Motivation

Formula (1) shows the relation between stress and strain. E is Young's modulus, E for silicon is 169 GPa [5]. Here, σ is the applied stress, and ϵ is the deformation rate. For example, 169 MPa stress in silicon results in 0.1% strain in silicon

$$\sigma = E \times \epsilon. \tag{1}$$

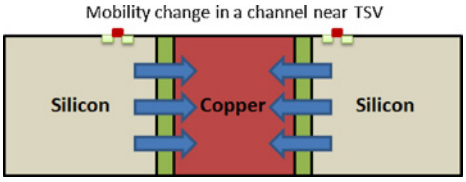

Fig. 1. Thermal stress around TSV.

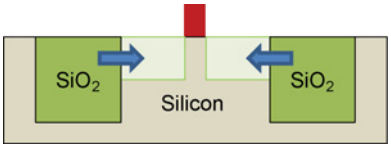

Fig. 2. Thermal stress in active region caused by surrounding STIs.

During 3-D IC manufacturing, stress is caused by CTE mismatch between copper TSV and silicon as shown in Fig. 1. Investigations [6] show that, at 200 °C, an anneal time of 30–60 min is required to achieve reasonable copper layer properties. Since CTE of copper is larger than silicon, at room temperature, copper has less volume compared with that during annealing process because of contraction. Several papers were published to simulate the TSV-induced stress [7], [1] using FEA simulation. They show that TSV can cause tensile stress of more than 200 MPa.

Strained silicon has been used to enhance I_{on} of transistors [8]. Unlike TSV stress, its impact on performance is not layout dependent. Several unwanted stress sources are largely layout dependent, and should be considered during the design step. STI is one of the unintentional stress sources [4], [9] because silicon dioxide used for STI fill pushes out silicon atoms near STI as shown in Fig. 2. Silicon dioxide in STI is generally grown and densified at temperature as high as 1000 °C [10]. Since CTE of silicon dioxide is smaller than silicon, silicon dioxide contracts slower than silicon when cooling down to room temperature. FEA simulation shows that STI can cause compressive stress of more than 200 MPa.

Mobility (μ) change as a function of applied stress (σ) was proposed by the following formula [11]:

$$\frac{\Delta\mu}{\mu} = -\Pi \times \sigma \tag{2}$$

where Π is the tensor of piezoresistive coefficients for holes and electrons, and σ is the applied stress. Tensile stress has positive sign and compressive stress has negative sign.

Since tensile stress increases electron mean free path, it enhances nMOS performance. However, longitudinal tensile stress degrades pMOS performance (as shown on top of Fig. 3) because of band deformation and scattering [12]. With longitudinal stress, Π for electrons is $-3.16\times10^{-10}\,\text{Pa}^{-1}$, and Π for holes is $7.18\times10^{-10}\,\text{Pa}^{-1}$ for (001) wafer surface and ⟨110⟩ channel which are popular manufacturing scheme [13], [11]. For example, when TSV stress is 200 MPa, $(\Delta\mu/\mu)_e$ is 6.32% for nMOS, and $(\Delta\mu/\mu)_h$ is −14.36% for pMOS.

However, if TSV is placed perpendicular to a transistor channel, mobility of both holes and electrons is enhanced [12] because of the stress in that direction. For transverse stress, Π for electrons is $-1.76\times10^{-10}\,\text{Pa}^{-1}$, and Π for holes is

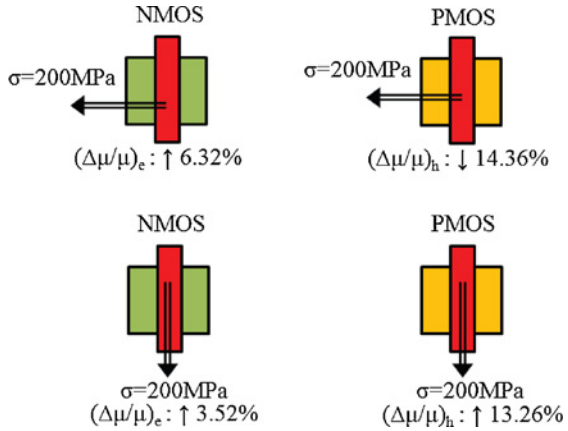

Fig. 3. Mobility change due to tensile stress. Top: $\Delta\mu/\mu$ for longitudinal tensile stress, bottom: $\Delta\mu/\mu$ for transverse tensile stress.

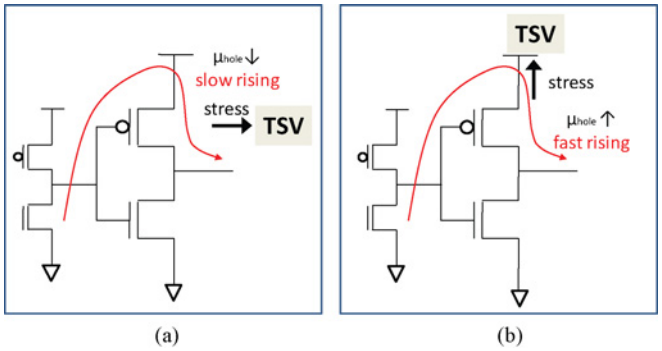

Fig. 4. Buffer delay change due to TSV stress. (a) Slower rising delay with longitudinal tensile stress. (b) Faster rising delay with transverse tensile stress.

$-6.63\times10^{-10}\,\text{Pa}^{-1}$ for (001) surface and ⟨110⟩ channel. Similarly, we can expect $(\Delta\mu/\mu)_\text{e}$ = 3.52%, and $(\Delta\mu/\mu)_\text{h}$ = 13.26% with σ = 200MPa. Empirically, $(\Delta I_\text{on}/I_\text{on})_\text{pMOS}$ is 0.5∼0.9 times of $(\Delta\mu/\mu)_\text{h}$, and $(\Delta I_\text{on}/I_\text{on})_\text{nmos}$ is 0.4∼0.6 times of $(\Delta\mu/\mu)_\text{e}$ [14], [15] because I_on of a transistor is determined by the sum of source, drain, and channel resistance.

Transistor variation due to the stress can change cell timing characteristics. In Fig. 4(a), buffer rising delay increases because of longitudinal tensile stress. Although buffer size is the same in Fig. 4(b), rising delay decreases due to transverse tensile stress. Therefore, TSV stress aware STA and layout optimization are essential steps for 3-D IC design.

Although stress in the direction perpendicular to a transistor channel can affect performance of the transistor, the major stress variation caused by STI is in the horizontal direction. Because of standard cell structure, as suggested in [4] and [9], STI stress in the horizontal direction is the main STI stress that affects mobility. The trend for STI is also different from the trend for TSV because the stress caused by STI is compressive instead of tensile. Longitudinal compressive stress enhances pMOS performance, but degrades nMOS performance.

A transistor-level STI-stress-aware delay analysis was proposed in [4], [16]. The method is not suitable for combined stress-aware STA and optimization for two reasons. First, only mobility variation model was provided after converting stress obtained from TCAD simulation. Because TSV and STI stresses interact with each other, stress from both structures should be combined before converted to mobility variation. Second, the method is based on SPICE simulation. Because of the required simulation time, the method is suitable for only a small number of critical paths; thus limiting its application to late stages of design flow. During early stages, e.g., global and detail placement, delay analysis may be required iteratively, and quick gate-level STI-stress-aware STA is desirable.

The impact of STI stress with layout dependency on circuit performance was investigated in [17]. A parallel 3-D stress simulator was developed using FEA method. The mobility change due to stress is included in the transistor modeling for circuit simulation. The circuit performance can thus be analyzed with the impact of STI stress. Although the method provides accurate stress information, the simulator was capable to simulate circuits containing only dozens of transistors. The long FEA simulation time makes it unsuitable for a design flow that requires the calculation of stress from thousands of STIs after each optimization.

III. Modeling and Design Flow

The overall flow of our 3-D IC design methodology is shown in Fig. 5. Our stress driven design flow consists of three steps. The first step is to calculate TSV/STI stresses and mobility change. Since FEA stress simulation that provides accurate solution takes several hours for one TSV, we use the analytical model proposed in [1]. Mobility change can be calculated by extension of (2). We explain the process and device modeling for a single TSV, and extend them to consider multiple TSVs in Section IV. For STI stress, a model is developed from results obtained from FEA simulations of STI stress. Mobility change caused by STI stress can be calculated in the same way as TSV stress. We explain the process and device modeling for a single STI, and extend them to consider STIs on both sides of each cell in Section V.

The second step is 3-D SA-STA. We use PrimeTime as an STA engine. In Section VII, we explain how to deal with Verilog netlist and timing library to consider mobility variation. The timing result can be used for layout optimization. Intuitively, if a pMOS in a cell is on a critical path, the cell should be moved to the region of a TSV that has positive $(\Delta\mu/\mu)_\text{h}$, or moved in such a way that surrounding STIs cause positive $(\Delta\mu/\mu)_\text{h}$. Finally, we can run STA iteratively to verify the layout optimization effect. In this paper, we demonstrate the potential for layout optimization to improve timing in Section VIII-C. We ran STA to identify a critical path, performed manual perturbation on the path, and reran STA to verify the timing improvement on the path.[3]

IV. Mobility Variation Under TSV-Induced Stress

In this paper, we assume that TSV is in cylindrical shape which is widely used for better manufacturability. FEA-based TSV simulation was proposed in [1] and [7]. The simulation

[3]Readers are referred to our related work [18] that performs automatic placement optimization to improve full-chip timing under TSV stress consideration.

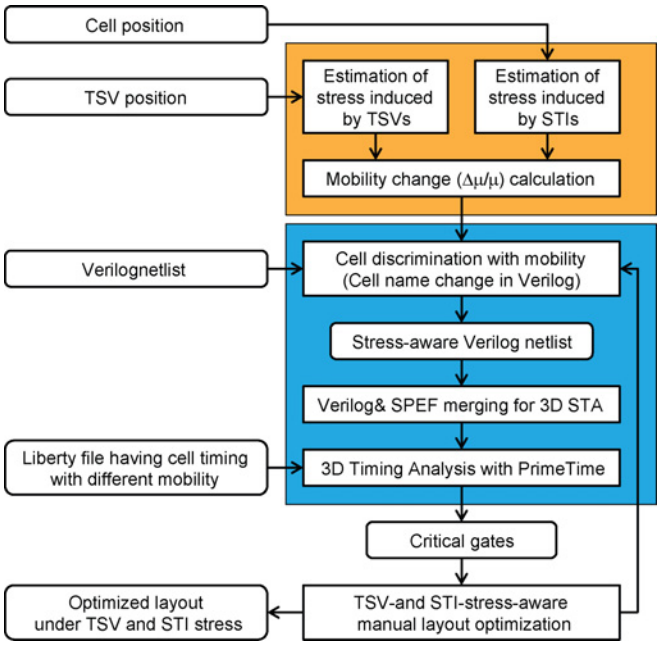

Fig. 5. Overall flow for TSV/STI stress modeling and analysis.

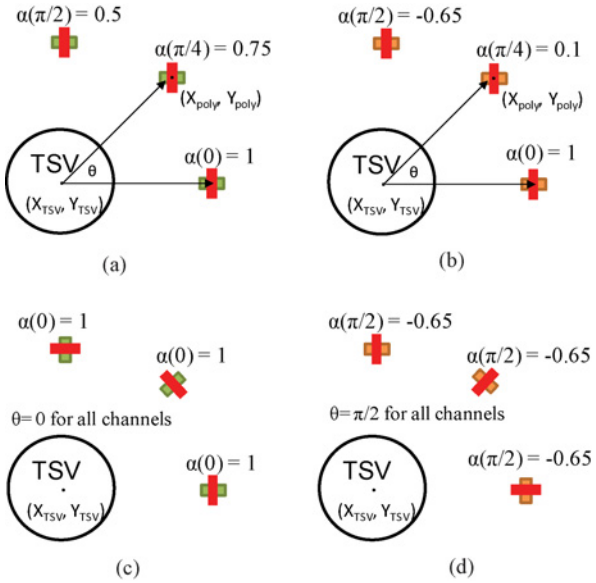

Fig. 6. Optimal orientation of MOSFET to maximize the mobility for (001) surface, ⟨110⟩ channel. (a) nMOS mobility variation. (b) pMOS mobility variation. (c) Optimal placement for the best nMOS performance. (d) Optimal placement for the best pMOS performance.

approaches provide accurate solution with long runtime which is not acceptable for our design flow that should calculate stress for thousands of TSVs iteratively after each optimization. Assuming 2-D radial plain stress, we use the following analytical solution which is known as *Lamé* stress solution [1]:

$$\sigma_{\mathrm{rr}} = -\frac{B\Delta\alpha\Delta T}{2}\left(\frac{R}{r}\right)^2. \tag{3}$$

The analytical stress model provides a relatively accurate solution [1]. In (3), B is biaxial modulus, $\Delta\alpha$ is CTE difference between copper and silicon, ΔT is temperature difference between copper annealing and operating temperature. R is TSV radius, and r is distance from TSV center. We assume that ΔT is 250 °C which is the case of 25 °C for room temperature and 275 °C for copper annealing temperature which is relatively low annealing temperature [6]. The formula shows that the thermal stress near TSV depends on the ratio of TSV radius and distance from TSV center.

Formula (2) provides an efficient way to calculate mobility variation due to σ_{rr}. As we observed in Section II, mobility change depends on not only σ_{rr} but also orientation between applied force and transistor channel. The empirical value for showing the relation of mobility change and the channel direction was proposed in [12]. We extend (2) to consider stress and the channel direction in (4) as follows:

$$\frac{\Delta\mu}{\mu}(\theta) = -\Pi \times \sigma_{\mathrm{rr}} \times \alpha(\theta)\,\theta = \tan^{-1}\left|\frac{Y_{\mathrm{TSV}} - Y_{\mathrm{poly}}}{X_{\mathrm{TSV}} - X_{\mathrm{poly}}}\right| \tag{4}$$

where $\alpha(\theta)$ is the orientation factor as a function of θ which is defined as the degree between the center of TSV and the center of a transistor channel when the transistor is placed vertically as shown in Fig. 6(a) and (b). We obtained $\alpha(\theta)$ from the measured data published in [12]. Π is the piezoresistive coefficient at $\theta = 0$ which works as longitudinal stress.

In Fig. 6(a), if nMOS is on right side of TSV, θ becomes zero, and $\alpha(0)$ becomes one, which enhances nMOS mobility at its maximum. However, if nMOS is on upper side of TSV, $\alpha(\pi/2)$ is 0.5, which means that nMOS mobility increase is half of the enhancement at $\theta = 0$. pMOS shows opposite trends, which has the best mobility enhancement at $\theta = \pi/2$. At $\theta = 0$, pMOS becomes slower than the case of no stress. Fig. 6(c) and (d) shows the transistor direction for the best performance. Although the mixed channel direction is not allowed due to patterning difficulty, the observation provides a way to optimize layout for 3-D ICs.

The top of Fig. 7 shows a contour map for hole mobility variation. Hole mobility decreases in the horizontal direction, while it increases in the vertical region. 45° direction has no hole mobility change. Contour map for electron mobility variation is presented in the bottom of Fig. 7. As we see in Fig. 6(a), the horizontal direction has more mobility enhancement zone.

Since we use many TSVs for signaling, power/ground, and clock network, we need to consider stress effect for multiple TSVs. Each TSV works as stress source to silicon. When a position in a wafer is strained by multiple stress sources, linear superposition can provide the multiple stress solution [1], [19]. The error of less than 2% between FEA simulation and linear superposition was reported in [19]. It is possible to use linear superposition to estimate stress caused by TSVs nearby a cell. We propose mobility variation for multiple TSVs as follows:

$$\frac{\Delta\mu}{\mu_{\mathrm{TSV}}} = \sum \frac{\Delta\mu}{\mu}(\theta) = -\Pi \sum_{i\in \mathrm{TSVs}} (\sigma_i \times \alpha(\theta_i)) \tag{5}$$

where σ_i is tensile stress caused by ith TSV, $\alpha(\theta_i)$ is the orientation factor of ith TSV. θ_i is the degree between center of ith TSV and a point that we want to get mobility variation.

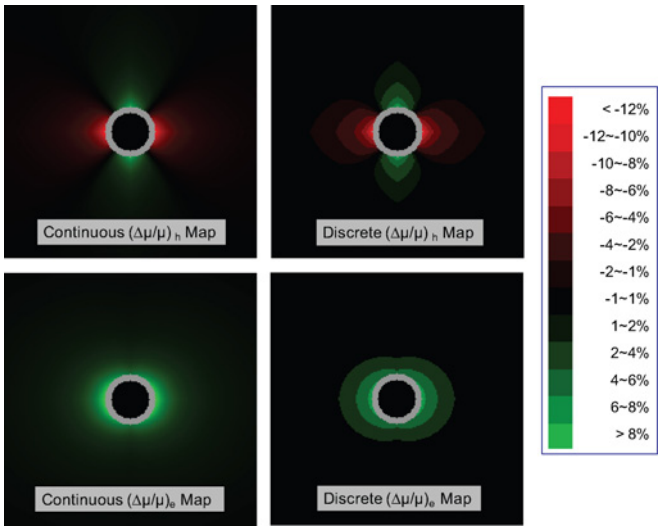

Fig. 7. Mobility contour map for a TSV. Top: contour map for hole mobility variation. Bottom: contour map for electron mobility variation.

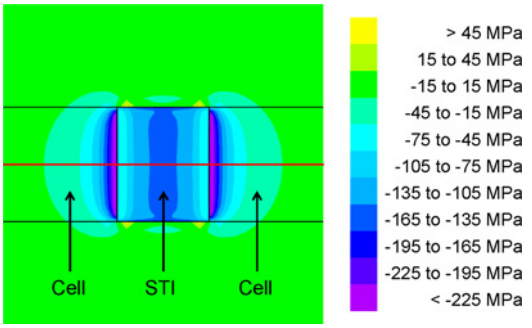

Fig. 8. Contour of stress (FEA simulation) caused by STI in the horizontal direction.

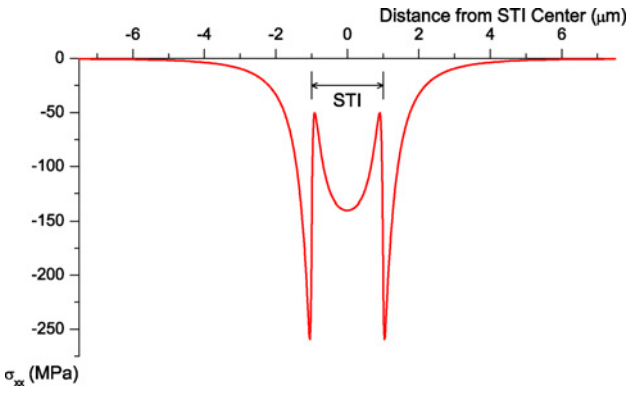

Fig. 9. Stress (FEA simulation) on a horizontal line across the center of the STI in Fig. 8.

V. Mobility Variation Under STI-Induced Stress

We use ANSYS, a commercial FEA simulator, to simulate stress caused by STI in this paper. An example of simulation result is shown in Fig. 8. The contour of stress in the horizontal direction caused by an STI in a plane of silicon is illustrated. Note that negative stress represents compressive stress. Compressive stress caused by an STI can be higher than 100 MPa on silicon surface close to the STI, or even higher than

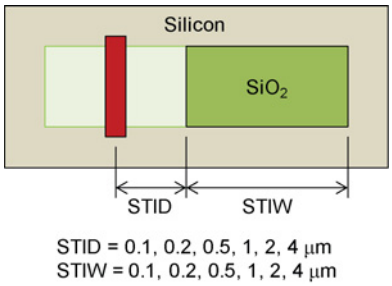

Fig. 10. Setup for FEA simulations used to model STI stress.

200 MPa on silicon surface adjacent to the STI. We observe that contour lines in the area close to the STI are parallel to left and right edges of the STI. Therefore, we approximate that the magnitude of horizontal stress caused by an STI is uniform in the vertical direction. This approximation results in some error at a position far from an STI and off its center; however, the actual magnitude of the stress at the position is relatively small, and so is its impact on the mobility variation.

The horizontal stress, caused by the STI, on a horizontal line across the center of the STI is shown in Fig. 9. The far left area of the STI is stress free. Stress magnitude increases as distance from center of the STI decreases, and rapidly increases in the area adjacent to the STI. Inside STI, stress is still compressive although its magnitude drops sharply. The trend reverses when we move away from STI center to the right.

The simulation setup used to develop an STI stress model is shown in Fig. 10. A patch of STI made of silicon dioxide is deposited on a silicon surface. STI stress mainly depends on two major parameters [4], distance to STI edge (STID) and width of STI (STIW). Their values used for FEA simulations are listed under the figure. Other dimensions of STI are from NCSU 45-nm cell library. The combinations of the two parameters result in 36 simulations. Because STI stress in the horizontal direction is the main stress that affects mobility [4], [9], we measure stress along the x-axis σ_{xx} at the channel.

The simulation results are shown in Figs. 11 and 12. In Fig. 11, we observe that the magnitude of STI stress rapidly decreases with the distance from the edge of STI. In Fig. 12, we observe that the magnitude of STI stress rapidly increases with the width of STI initially, but does not change much after a certain width. The first observation hints that the magnitude of STI stress is inversely proportional to STID, and the second observation hints that the magnitude of STI stress is an exponential saturation curve with respect to STIW. We use surface fitting tool in MATLAB to curve fit the model. Because stress caused by STI is nonlinear, we model it with a custom equation. Both STID and STIW are independent variables, and σ_{xx} is the dependent output variable. The tool finds the coefficients of the model automatically. The two observations lead us to model STI stress in the following form:

$$\sigma_{xx} = \frac{\alpha(1 - e^{\beta \cdot \mathrm{STIW}}) + \chi}{\mathrm{STID}^{\delta} + \epsilon} \tag{6}$$

where α, β, χ, δ, and ϵ are curve-fitting coefficients, and their value are -37.51, -3.24, 0.8601, 1.594, and 0.1317, respectively. The coefficient of determination for this model is 0.9987, and the root mean square error is 2.843 MPa.

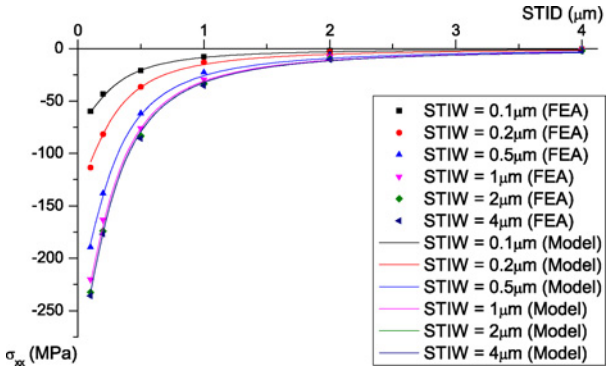

Fig. 11. STI stress (FEA simulation and model) at different distances.

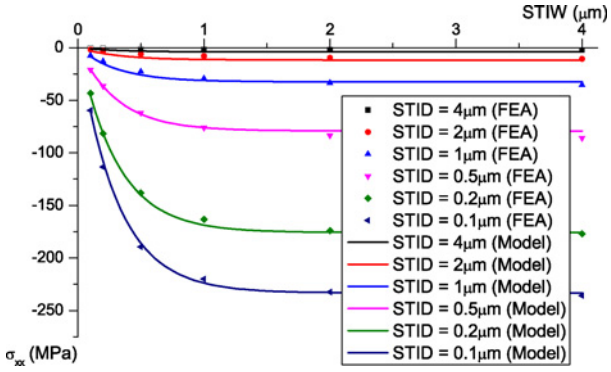

Fig. 12. Stress (FEA simulation and model) induced by different STI widths.

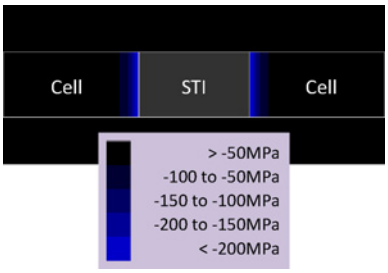

Fig. 13. Contour map of stress (model) for a single 4 μm-wide STI.

Based on the model, we generate a contour map of STI stress. The contour for a 4 μm-wide STI is shown in Fig. 13. We observe that compressive stress of more than 200 MPa is close to the STI edge, but the stress magnitude rapidly drops below 100 MPa in the horizontal direction. Note that the area occupied by STI is gray in the contour. By using σ_{xx} obtained from (6) in (2), the contour map for hole and electron mobility variation can be generated as shown in Fig. 14(a) and (b), respectively. From the contour, we observe that hole mobility is only enhanced by STI stress, whereas electron mobility is only degraded. Both the enhancement and degradation take place on left and right sides of the STI.

Similar to the case for multiple TSVs in Section IV, it is possible to use linear superposition to estimate stress caused by STIs on both left and right sides of a cell. We validate by FEA simulations that linear superposition can be used to combine the stress. Two STI patches are deposited on a silicon surface with varying STID, STIW_1, and STIW_2. For each setting, three simulations are performed: one STI on the left, one STI on the right, and both STIs. The resulting σ_{xx} at the channel from the first two simulations are added, and compared with the third simulation. The error of less than 3% between FEA simulation and linear superposition is observed in all cases. We propose mobility variation for multiple STIs as

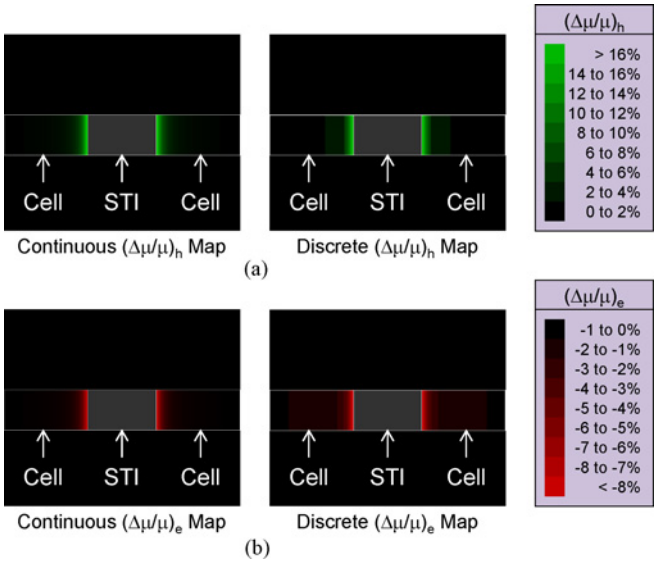

Fig. 14. Contour maps of mobility (model) for an STI. (a) Hole mobility variation. (b) Electron mobility variation.

$$\left(\frac{\Delta\mu}{\mu}\right)_{\text{STI}} = \sum \frac{\Delta\mu}{\mu} = -\Pi \sum_{i\in\text{STIs}} \sigma_{xx_i} \tag{7}$$

where σ_{xx_i} is the compressive stress caused by ith STI on left or right side of the cell.

Although the works in [4], [16] studied the impact of STI stress, only mobility variation model was provided after converting stress obtained from TCAD simulation. Because TSV and STI stresses interact with each other in 3-D ICs, both stresses should be combined before converted to mobility variation. Therefore, STI stress model in (6) is necessary. We first validate by FEA simulations that linear superposition can be used to combine the effect of both TSV and STI stresses. A patch of STI deposited on a silicon surface containing a TSV is simulated with varying TSV position, STID, and STIW. For each setting, three simulations are performed: only TSV, only STI, and both TSV and STI. The resulting σ_{xx} at the channel from the first two simulations are added, and compared with the third simulation. The results from the simulations and linear superposition are shown in Table I. The error of less than 4% between FEA simulations and linear superposition is observed in almost all the cases. In the few cases that the error is more than 4%, the magnitude of the stress is less than 9 MPa while the error is less than 2 MPa, which are insignificant compared to other cases. It is possible to use linear superposition to estimate stress caused by both TSV and STI during early design stages. We propose the mobility variation for both TSV and STI as

$$\left(\frac{\Delta\mu}{\mu}\right)_{\text{total}} = \left(\frac{\Delta\mu}{\mu}\right)_{\text{TSV}} + \left(\frac{\Delta\mu}{\mu}\right)_{\text{STI}} \tag{8}$$

TABLE I
FEA SIMULATION AND LINEAR SUPERPOSITION OF TSV AND STI

TSVX (μm)	TSVY (μm)	STID (μm)	STIW (μm)	$\sigma_{xx_{TSV}}$ (MPa)	$\sigma_{xx_{STI}}$ (MPa)	σ_{xx} (MPa)	Super-position (MPa)	Error (%)
0	5	0.1	0.1	−137.03	−15.27	−150.23	−152.30	1.38
0	5	4	0.1	−136.04	−0.08	−136.10	−136.12	0.01
0	5	4	4	−136.65	−0.59	−137.26	−137.24	−0.02
0	10	0.1	0.1	−29.71	−15.27	−44.65	−44.98	0.75
0	10	4	0.1	−29.75	−0.08	−29.81	−29.83	0.07
0	10	4	4	−29.76	−0.58	−30.19	−30.35	0.54
5	0	0.1	0.1	152.80	−15.30	133.53	137.50	2.97
5	5	0.1	0.1	8.76	−15.28	−7.12	−6.52	−8.45
5	5	4	0.1	6.93	−0.08	7.00	6.86	−2.06
5	5	4	4	7.27	−0.59	8.20	6.68	−18.60
5	10	0.1	0.1	−11.63	−15.27	−26.90	−26.90	−0.01
5	10	4	0.1	−11.60	−0.08	−11.64	−11.68	0.30
5	10	4	4	−11.60	−0.59	−11.82	−12.19	3.10
10	0	0.1	0.1	41.36	−15.28	25.09	26.08	3.94
10	0	4	0.1	41.41	−0.08	41.23	41.34	0.25
10	5	0.1	0.1	22.22	−15.28	6.33	6.94	9.61
10	5	4	0.1	22.27	−0.08	22.18	22.20	0.09
10	5	4	4	22.25	−0.60	21.69	21.65	−0.16
Average absolute error								2.91

VI. MOBILITY VARIATION UNDER BIAXIAL STRESS

TSV-induced stress is biaxial in nature. In [20], the biaxial stress-induced carrier mobility variation is defined as follows:

$$\frac{\Delta\mu}{\mu} = -(\pi'_{11}\sigma_{xx} + \pi'_{12}\sigma_{yy}) \tag{9}$$

where π'_{11} and π'_{12} are piezoresistive coefficients defined along the reference axes of (100) wafer, and σ_{xx} and σ_{yy} are stress in Cartesian coordinate system. For hole, π'_{11} and π'_{12} are $7.18\times10^{-10}\,\text{Pa}^{-1}$ and $-6.63\times10^{-10}\,\text{Pa}^{-1}$, respectively, and for electron, π'_{11} and π'_{12} are $-3.12\times10^{-10}\,\text{Pa}^{-1}$ and $-1.76\times10^{-10}\,\text{Pa}^{-1}$, respectively [20].

To utilize (9), σ_{xx} and σ_{yy} must be converted from TSV-induced stresses σ_{rr} and $\sigma_{\theta\theta}$ in cylindrical coordinate system. In [1], $\sigma_{\theta\theta} = -\sigma_{\text{rr}}$ for *Lamé* analytical stress solution in (3). We use the method described in [19] for conversion. STI-induced stress must be added to total stress after conversion. The total σ_{xx} and σ_{yy} are computed by

$$\sigma_{xx} = \sum_{i\in\text{TSVs}} \sigma_{xx_i} + \sum_{j\in\text{STIs}} \sigma_{xx_j}$$
$$\sigma_{yy} = \sum_{i\in\text{TSVs}} \sigma_{yy_i} \tag{10}$$

where σ_{xx_i} and σ_{xx_j} are the stress along the x-axis caused by ith TSV and jth STI (on left or right side of the cell), respectively, and σ_{yy_i} is the stress along the y-axis caused by ith TSV. We compare the result between considering uniaxial stress and considering biaxial stress in Section VIII-D.

VII. TIMING ANALYSIS WITH STRESS CONSIDERATION

In this section, we explain how to incorporate the mobility variation into cell level STA flow.

A. Timing Analysis for 3-D ICs

Although topology of a cell is the same, its timing characteristic is changed by stress. Fig. 15 shows an example

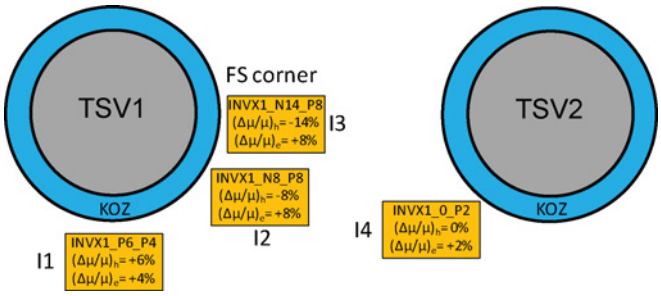

Fig. 15. Timing corner determination according to mobility variation.

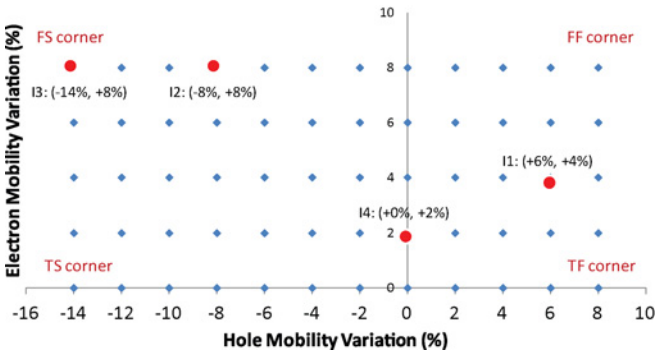

Fig. 16. Timing corner with TSV stress.

that cells having the same topology and size can be in different timing corners systematically determined by TSVs (and STIs). When two TSVs are near three inverters, cell characteristics are different at different positions. From (8), we can determine $\Delta\mu/\mu$ at any point for a given layout. After mobility calculation, our framework renames cells such that mobility variation is included in Verilog netlist. For example, `I2` is renamed to `INVX1_P-8_N+8` which means −8% hole mobility and 8% electron mobility in Fig. 15.

We prepare a Verilog netlist and a parasitic extraction file (SPEF) per die. In addition, we make a top level Verilog netlist that instantiates the dies and connects them using wires which correspond to TSV connections. Then we make a top level SPEF file for the TSV connections. With a proper timing constraint file, we can run PrimeTime to get 3-D STA results.

B. Timing Library for Mobility Variation

To consider the systematic variation during STA, we characterize a cell with different mobility corners as shown in Fig. 16. Hole mobility variation is from −14% to 8%, and electron mobility variation is up to 8% to cover stress caused by TSVs in Fig. 15. Inverter `I1` in Fig. 15 matches the corner near FF corner, whereas `I3` is in FS corner. With mobility-variation-aware library and Verilog netlist having renamed cells, we can run PrimeTime to perform STA with TSV and STI stresses.

To cover mobility variation caused by multiple TSVs, we need to extend the mobility variation range ($-20\% \le (\Delta\mu/\mu)_{\text{h}} \le 8\%$, $0\% \le (\Delta\mu/\mu)_{\text{e}} \le 14\%$). In addition, to consider both TSV and STI stresses, the mobility variation range needs to be extended even further. The mobility variation ranges needed to be covered for different stress sources are illustrated in Fig. 17. Because of their opposite kinds of stress,

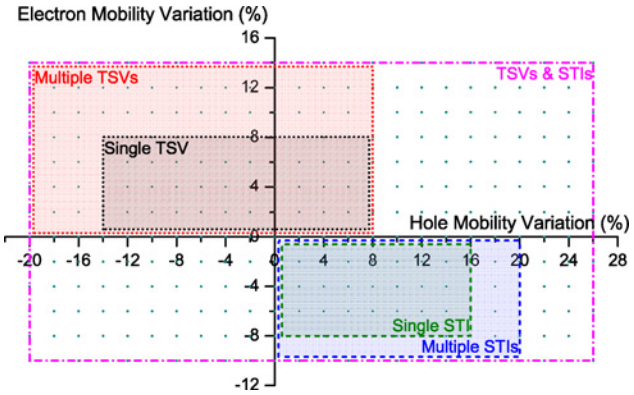

Fig. 17. Extended timing corner with both TSV and STI stresses.

the mobility variation range needed to be covered for TSV and STI hardly overlaps with each other. The interaction between both TSV and STI stresses requires more than merely adding the covered mobility variation range for both of them.

If mobility step is 2%, we need to characterize 312 (= 24 × 13) libraries with different mobility values, which is prohibitive. However, we observe that rising delay variation only depends on $(\Delta\mu/\mu)_h$, and falling delay variation only depends on $(\Delta\mu/\mu)_e$ from Fig. 18. When we simulate inverter rising delay with mobility variation, electron mobility variation does not contribute to the delay. Similarly, we observe that falling delay only depends on electron mobility variation. We also observe that hole mobility variation can cause more than 20% pMOS performance variation, and electron mobility variation can enhance nMOS performance up to 7.5%. We use inverter in NCSU library and PTM SPICE model [21] to obtain Fig. 18. Therefore, we can fix $(\Delta\mu/\mu)_e$ when we sweep $(\Delta\mu/\mu)_h$. Characterizing 37 (= 24 + 13) libraries is enough to cover the entire mobility set. If mobility step is 4%, 20 (= 13 + 7) libraries are required. Since delay variation has semi-linear dependency on mobility variation, we can use interpolation for the mobility value between two libraries.

VIII. Experimental Results

We implemented our 3-D SA-STA in C++ and tested on a 3 GHz Linux machine with 4 GB RAM. We generated the mobility-aware library based on NCSU 45-nm cell library with 2% mobility step. We used TSV size of 5 μm, TSV parasitic capacitance of 70 fF and resistance of 0.1Ω. The keep-out zone (KOZ) size is set to 0.5 μm.

A. Full Chip Mobility Variation Map

First, we show the efficiency of our compact stress and mobility modeling for TSV. When we want to find $\Delta\mu/\mu$ at any point on a die, we can obtain the value promptly. We generate mobility contour in Fig. 19 (die size: 175^2 μm^2, #TSVs: 462) in only 14.9 s. The stress simulation time for all the designs are also provided in Table II. The proposed STA with compact process/device model is fast enough to be used for iterative optimization purpose. Fig. 19(a) shows an observation for layout optimization that the leftmost and

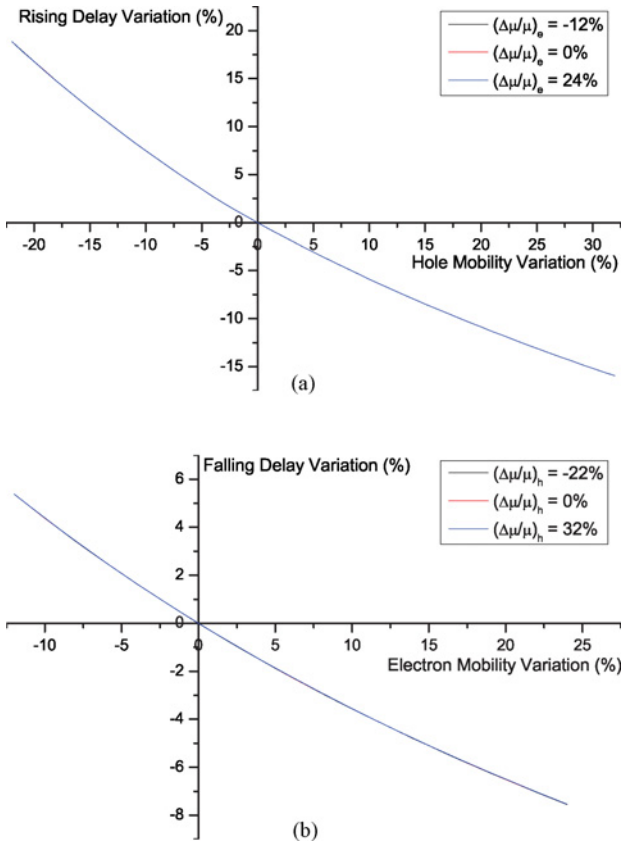

Fig. 18. Inverter delay variation with different $(\Delta\mu/\mu)_h$ and $(\Delta\mu/\mu)_e$. (a) Rising delay dependency on $(\Delta\mu/\mu)_h$. (b) Falling delay dependency on $(\Delta\mu/\mu)_e$.

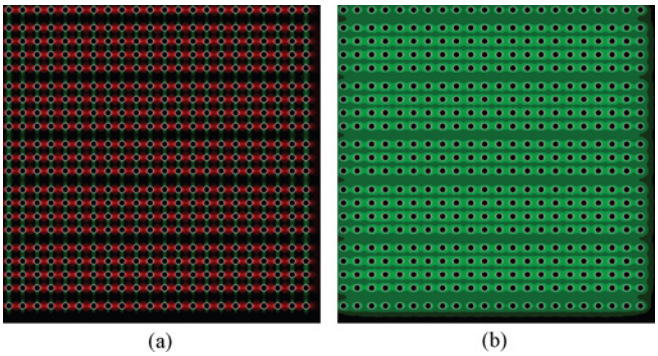

Fig. 19. Mobility variation contour maps for 22×21 TSV array. (a) Hole. (b) Electron.

rightmost sides have wider hole mobility enhanced zone than the middle area because the region has less mobility degradation by horizontally placed neighboring TSVs.

Next, we generate mobility contour in Fig. 20 (die size: 220^2 μm^2, number of TSVs: 600, number of number of cells: 3422) while considering both TSV and STI stresses. The contour is noticeably different from Fig. 19 in two ways. First, because we are not interested in the stress inside STI for this paper, we show the area occupied by STI in gray. Second, the trend of mobility variation changes, i.e., we observe increasing area of hole mobility enhancement but decreasing area of electron mobility enhancement. This phenomenon is largely due to the inclusion of STI stress.

TABLE II
BENCHMARK CIRCUITS

Circuits	No. of Cells	No. of Nets	No. of TSVs	Profile	Runtime
ex	14 864	15 045	1483	Execution unit	15
8051	15 712	15 755	1575	Microcontroller	17
8086	19 895	19 909	1987	Microprocessor	18
MAC2	29 706	29 980	2971	Arithmetic unit	29
ethernet	77 234	77 381	7748	Network controller	70
RISC	88 401	89 154	8837	Microprocessor	79
b18	103 711	103 948	10 367	Multiprocessors	94
des_perf	109 181	109 416	10 916	Data encryption	96
vga_lcd	126 379	126 484	12 638	Display controller	132
b19	168 943	169 476	16 869	Multiprocessors	155

We also provide the runtime for mobility contour generation in seconds.

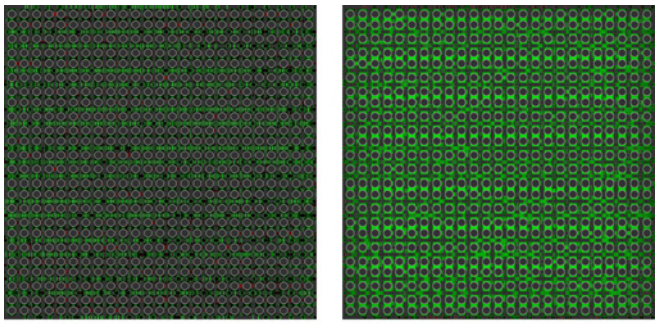

Fig. 20. Mobility variation contour maps for a layout considering both TSV and STI stresses. (a) Hole. (b) Electron.

B. Full Chip Timing Analysis Results

In this experiment, we compare our SA-STA with no stress case. Ten benchmark circuits used to show the timing variation are listed in Table II. The area utilization of each circuit is around 70%. All whitespace is occupied by STI. The total amount of STI is in the same range (30–70%) as other STI-related works [22]. The circuits are placed for wire length minimization with neither TSV nor STI stress consideration. The hole and electron mobility variation of each circuit is shown in Table III. The timing results are shown in Table IV.

When we consider only TSV stress effect, hole and electron mobility variation of all circuits are in the same ranges as shown in Table III. Hole mobility variation in each circuit ranges from −18% to 6%; whereas, electron mobility variation ranges from 0 to around 13%. Although the mobility variations of all circuits are in the same ranges, their timing variation is different. The change of longest path delay (LPD) of the circuits has variation from −5.65% to 6.52%. Some circuits have timing gain while some circuits have timing penalty. On average, the impact of TSV stress on LPD is 2.82%. For random placement, the impact of hole and electron mobility variation may compensate each other, and result in low combined enhancement/degradation in timing for some cases because the average of carrier (both hole and electron) mobility variation is close to zero. In many cases, however, the impact of hole and electron mobility variation is in the same direction, resulting in significant changes (either enhancement or degradation) of LPD. If we consider TSV stress effect during cell and TSV placement, we can expect performance improvement for every circuit. The change of total negative slack (TNS) has variation from −28.48% to 50.43%, which is bigger than the variation of the change of LPD. That motivates the need of TSV-stress-aware layout optimization.

When we consider only STI stress effect, hole and electron mobility variation of all circuits are exactly in the same ranges as shown in Table III. Hole mobility variation in each circuit ranges from 0 to 19.72%; whereas, electron mobility variation ranges from −8.68 to 0%. The carrier mobility variation of all circuits are in the exact same range because STI stress depends heavily on the relative size of cell and its adjacent STIs. Wide cells or cells far away from narrow STIs have no carrier mobility variation; whereas, the narrowest cell in the library having wide STIs on both of its sides results in the highest carrier mobility variation. The change of LPD of the circuits has variation from −5.92% to 1.92%, and the average LPD variation is 4.11%. Most circuits have timing gain because, for random placement, the average of carrier (both hole and electron) mobility variation is much higher than zero. In addition, STI is pervasive on IC layout. Without considering STI stress, STA only reports pessimistic timing result. Including STI stress, the pessimism in timing results decreases. TNS is significantly reduced by 50.07% on average because several violating paths become nonviolating. Wide variation of the change of both LPD and TNS suggests the importance of STI-stress-aware layout optimization.

Finally, when we consider both TSV and STI stresses, the range of hole and electron mobility variation of all circuits shifts from the range when only TSV or only STI stress is considered as shown in Table III. Hole mobility variation in each circuit ranges from −14% to 25%; whereas, electron mobility variation ranges from −8.68 to around 11%. The change of LPD of the circuits has variation from −5.56% to 2.89%, and the average LPD variation is 3.19%. The changes are in the same direction as the changes considering only STI stress. However, the magnitude of the change decreases because of the interaction between TSV and STI stresses. As pointed out by earlier results, TSV stress tends to increase the LPD; whereas, STI stress tends to decrease the LPD. The impact of both stresses partially cancels each other, resulting in decreased magnitude of LPD decrease. Compared to the changes considering only STI stress, some circuits have timing gain while some circuits have timing penalty. This variation suggests that TSV stress still has significant impact on timing even after STI stress is considered. TNS is significantly reduced by 45.49% on average. Therefore, both TSV and STI stresses can be exploited together for performance improvement. The potential to exploit them to improve timing is revealed as shown in the next experiment.

C. Placement Optimization Results

We manually optimize the critical path in des_perf to present the potential benefit of TSV-stress-aware layout optimization. We do not consider STI stress in this experiment so that we can study the impact of only TSV. Before optimization, the path delay is 8.720 ns with TSV-stress-aware timing analysis. We could reduce the delay to 8.138 ns with small

TABLE III
COMPARISON OF MOBILITY VARIATION RANGE

Circuit	With TSV Stress		With STI Stress		With Both TSV and STI Stresses	
	Hole Mobility Variation (%)	Electron Mobility Variation (%)	Hole Mobility Variation (%)	Electron Mobility Variation (%)	Hole Mobility Variation (%)	Electron Mobility Variation (%)
ex	−18.63 to +6.00	0.00 to +13.28	0.00 to +19.72	−8.68 to 0.00	−14.88 to +25.21	−8.68 to +10.86
8051	−18.88 to +6.36	0.00 to +13.42	0.00 to +19.72	−8.68 to 0.00	−13.88 to +24.95	−8.68 to +11.01
8086	−17.88 to +6.34	0.00 to +12.73	0.00 to +19.72	−8.68 to 0.00	−13.70 to +25.53	−8.68 to +11.15
MAC2	−17.46 to +6.31	0.00 to +12.50	0.00 to +19.72	−8.68 to 0.00	−13.39 to +25.82	−8.68 to +10.71
ethernet	−17.80 to +6.34	0.00 to +12.61	0.00 to +19.72	−8.68 to 0.00	−14.06 to +25.93	−8.68 to +11.00
RISC	−17.91 to +6.40	0.00 to +12.85	0.00 to +19.72	−8.68 to 0.00	−14.25 to +26.05	−8.68 to +11.30
b18	−18.63 to +6.32	0.00 to +13.39	0.00 to +19.72	−8.68 to 0.00	−14.88 to +25.87	−8.68 to +11.42
des_perf	−18.59 to +6.20	0.00 to +13.44	0.00 to +19.72	−8.68 to 0.00	−14.49 to +25.85	−8.68 to +11.49
vga_lcd	−18.65 to +6.37	0.00 to +13.39	0.00 to +19.72	−8.68 to 0.00	−14.35 to +25.96	−8.68 to +11.75
b19	−17.94 to +6.46	0.00 to +13.02	0.00 to +19.72	−8.68 to 0.00	−14.43 to +25.83	−8.68 to +11.49

TABLE IV
LONGEST PATH DELAY (LPD) AND TOTAL NEGATIVE SLACK (TNS) COMPARISON IN ns

Circuit	Without Stress		With TSV Stress		With STI Stress		With Both TSV and STI Stresses	
	LPD	TNS	LPD	TNS	LPD	TNS	LPD	TNS
ex	12.009	−8.815	11.881 (−1.06%)	−7.215 (−18.15%)	11.686 (−2.69%)	−5.280 (−40.10%)	11.577 (−3.59%)	−4.348 (−50.67%)
8051	5.041	−144.035	5.370 (6.52%)	−145.363 (0.92%)	4.768 (−5.42%)	−60.450 (−58.03%)	4.761 (−5.56%)	−61.351 (−57.41%)
8086	9.283	−19.317	9.423 (1.50%)	−26.779 (38.63%)	8.734 (−5.92%)	−3.495 (−81.90%)	8.888 (−4.26%)	−7.194 (−62.76%)
MAC2	7.797	−87.337	7.905 (1.38%)	−93.422 (6.97%)	7.435 (−4.64%)	−46.541 (−46.71%)	7.525 (−3.49%)	−49.861 (−42.91%)
ethernet	9.294	−474.917	9.484 (2.05%)	−463.344 (−2.44%)	9.472 (1.92%)	−492.182 (3.64%)	9.562 (2.89%)	−480.541 (1.18%)
RISC	8.583	−57.101	8.098 (−5.65%)	−40.840 (−28.48%)	8.434 (−1.73%)	−27.864 (−51.20%)	8.387 (−2.29%)	−17.779 (−68.86%)
b18	12.522	−41.301	12.838 (2.53%)	−62.128 (50.43%)	12.013 (−4.06%)	−22.024 (−46.67%)	12.308 (−1.71%)	−30.331 (−26.56%)
des_perf	8.467	−40.298	8.720 (2.99%)	−45.054 (11.80%)	8.026 (−5.21%)	−10.090 (−74.96%)	8.294 (−2.04%)	−11.513 (−71.43%)
vga_lcd	8.228	−0.991	8.456 (2.78%)	−1.191 (20.25%)	7.835 (−4.77%)	−0.671 (−32.27%)	8.078 (−1.82%)	−0.875 (−11.71%)
b19	13.389	−126.528	13.618 (1.71%)	−145.533 (15.02%)	12.760 (−4.70%)	−43.996 (−65.23%)	12.821 (−4.25%)	−48.795 (−61.44%)
Average Absolute Change			(2.82%)	(19.31%)	(4.11%)	(50.07%)	(3.19%)	(45.49%)

Percentage of changes is shown in parenthesis.

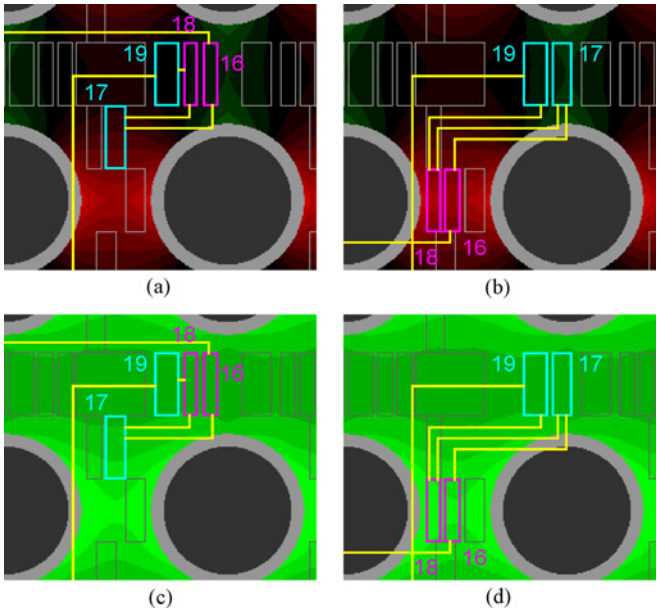

Fig. 21. Cell perturbation to take advantage of TSV-stress-induced mobility variation. (a) Hole mobility contour with original cell placement. (b) Hole mobility contour after cell perturbation. (c) Electron mobility contour with original cell placement. (d) Electron mobility contour after cell perturbation.

layout perturbation, which is 6.67% improvement. It is even less than the path delay without stress, which is 8.467 ns in Table IV. We adjust each cell position with small perturbation to gain timing. The maximum timing gain in a cell is 23.37% improvement.

Fig. 21 shows how cell relocation works for timing optimization. We capture the placement result on a die with TSV-stress-induced mobility variation contours. Cell 17 and 19 are hole-mobility critical cells because the timing arc is rising on the path. Therefore, we perturb the cells to be placed close to green area in hole-mobility contour. However, Cell 16 and 18 are electron-mobility critical. Therefore, we push the cells to have more mobility enhancement in Fig. 21(c) and (d).

Next, we manually optimize the same critical path in des_perf when considering only STI stress to present the potential benefit of STI-stress-aware layout optimization. When we perturb a cell, the STI surrounding the cell changes. We update the changes in position and dimension of the STI before computing stress map and mobility change of devices inside the cells. Before optimization, the path delay is 7.989 ns with STI-stress-aware timing analysis. We could reduce the delay to 7.651 ns with small layout perturbation which is 4.22% improvement. We adjust each cell position with small perturbation to gain timing. The maximum timing gain in a cell is 17.51% improvement.

Fig. 22 shows how cell relocation works for this timing optimization. We capture the placement result on a die with STI-stress-induced mobility variation contours. Like previous experiment, Cell 17 and 19 are hole-mobility critical cells because the timing arc is rising on the path. Surrounding them by wide STIs improves hole mobility. However, Cell

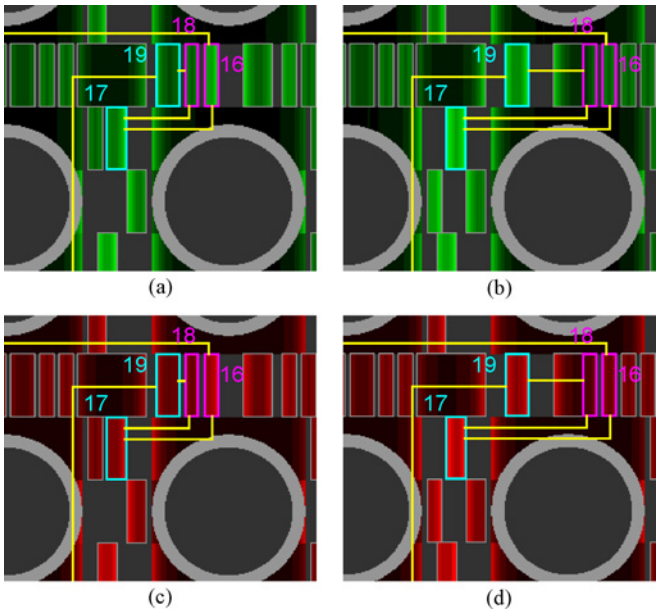

Fig. 22. Cell perturbation to take advantage of STI-stress-induced mobility variation. (a) Hole mobility contour with original cell placement. (b) Hole mobility contour after cell perturbation. (c) Electron mobility contour with original cell placement. (d) Electron mobility contour after cell perturbation.

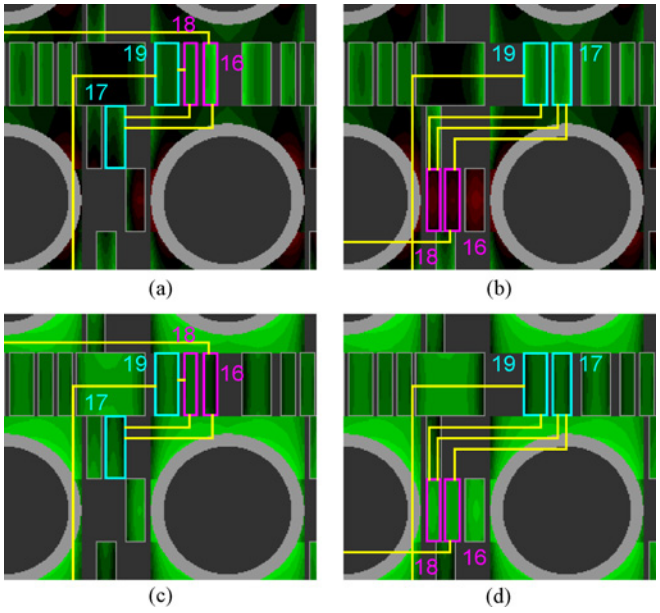

Fig. 23. Cell perturbation to take advantage of TSV-STI-stress-induced mobility variation. (a) Hole mobility contour with original cell placement. (b) Hole mobility contour after cell perturbation. (c) Electron mobility contour with original cell placement. (d) Electron mobility contour after cell perturbation.

16 and 18 are electron-mobility critical. Therefore, we move the cells to reduce mobility degradation by having only narrow STIs surrounding them as shown in Fig. 22(c) and (d). Note that manual optimization when considering only STI stress is more difficult than when considering only TSV stress. When only TSV stress is considered, moving cells does not change mobility-variation contour. When only STI stress is considered, moving a cell changes dimension of STI surrounding it, thus its delay may not be improved as much as expected.

TABLE V
GATE OPTIMIZATION CONSIDERING BOTH TSV AND STI STRESSES ON THE TARGET PATH WITH PERTURBATION

Cell	Original Gate	Optimized Gate	Timing Arc	Orig. D (ps)	Opt. D (ps)	Reduc. (%)
	Input port	Input port				
1	I1_P+6_N+4	I1_P-8_N+10	Fall	49.85	44.62	10.49
2	I1_P+4_N+4	I1_P+20_N+0	Rise	29.15	24.01	17.63
3	I1_P+4_N+4	I1_P-6_N+8	Fall	167.51	166.46	0.63
4	I1_P+6_N+4	I1_P+16_N+2	Rise	428.15	374.05	12.64
5	I1_P+6_N+4	I1_P-2_N+6	Fall	178.81	163.86	8.36
6	I1_P+10_N+2	I1_P+18_N+2	Rise	677.35	614.72	9.25
7	I1_P+20_N-8	I1_P+6_N-2	Fall	914.05	949.16	−3.84
8	I1_P+4_N+4	I1_P+16_N+2	Rise	1489.17	1261.57	15.28
9	I1_P+18_N-2	I1_P+18_N-2	Fall	352.66	391.58	−11.04
10	I1_P+20_N-4	I1_P+20_N-4	Rise	175.74	147.00	16.35
11	I4_P+18_N-2	I4_P+18_N-2	Fall	102.76	89.22	13.18
12	M_P+2_N+8	M_P-10_N+10	Fall	409.04	410.91	−0.46
13	M_P-10_N+10	M_P-2_N+8	Rise	874.10	800.69	8.40
14	AO_P-10_N+8	AO_P-10_N+8	Fall	538.98	553.49	−2.69
15	NA_P+10_N+4	NA_P+12_N+4	Rise	749.84	702.28	6.34
16	I1_P+16_N+2	I1_P-6_N+8	Fall	852.80	888.45	−4.18
17	NO_P+4_N+6	NO_P+12_N+4	Rise	240.80	222.78	7.48
18	I1_P+10_N+4	I1_P-8_N+8	Fall	46.81	44.56	4.81
19	OA_P+6_N+6	OA_P+10_N+4	Rise	16.58	17.53	−5.73
	DFFPOSX1	DFFPOSX1	Rise	0.11	0.12	−9.09
Path Delay				8294.26	7867.06	5.15

Gate $I1$ is INVX1, $I4$ is INVX4, M is MUX2X1, AO is AOI21X1, NA is NAND3X1, NO is NOR2X1, and OA is OAI21X1.

Finally, we manually optimize the same critical path in des_perf when considering both TSV and STI stresses to reveal the impact of the interaction between both stresses. When we perturb a cell, the STI surrounding the cell changes. We update the changes in position and dimension of the STI before computing stress map and mobility change of devices inside the cells. Before optimization, the path delay is 8.294 ns with TSV-STI-stress-aware timing analysis. We could reduce the delay to 7.867 ns with small layout perturbation which is 5.15% improvement. Table V shows the gates on the path. We can see the cell renaming according to the mobility variation. We adjust each cell position with small perturbation to gain timing. The maximum timing gain in a cell is 17.63% improvement.

Fig. 23 shows how cell relocation works for this timing optimization. We capture the placement result on a die with TSV-STI-stress-induced mobility variation contours. Like previous experiment, Cell 17 and 19 are hole-mobility critical cells because the timing arc is rising on the path. Besides moving them to the area that TSVs provide improvement on rise time, surrounding them by wide STIs improves hole mobility. However, Cell 16 and 18 are electron-mobility critical. Therefore, we push the cells to have more mobility enhancement provided by TSVs as shown in Fig. 23(c) and (d). Note that manual optimization when considering both TSV and STI stresses is more difficult than when considering only TSV stress. When only TSV stress is considered, moving cells does not change mobility-variation contour. When both TSV and STI stresses are considered, moving a cell to exploit TSV stress changes dimension of STI surrounding it, thus its delay may not be improved as much as expected.

TABLE VI
COMPARISON OF MOBILITY VARIATION RANGE CONSIDERING BIAXIAL STRESS

Circuit	With TSV Stress		With STI Stress		With Both TSV and STI Stresses	
	Hole Mobility Variation (%)	Electron Mobility Variation (%)	Hole Mobility Variation (%)	Electron Mobility Variation (%)	Hole Mobility Variation (%)	Electron Mobility Variation (%)
ex	−31.69 to +22.04	−2.17 to +3.12	+0.00 to +19.72	−8.57 to +0.00	−27.87 to +41.01	−10.66 to +1.78
8051	−32.76 to +21.98	−2.16 to +3.23	+0.00 to +19.72	−8.57 to +0.00	−26.91 to +40.40	−10.56 to +1.48
8086	−31.20 to +22.07	−2.17 to +3.07	+0.00 to +19.72	−8.57 to +0.00	−24.58 to +41.41	−10.64 to +1.51
MAC2	−30.86 to +22.23	−2.19 to +3.04	+0.18 to +19.72	−8.57 to −0.08	−24.81 to +41.36	−10.70 to +1.91
ethernet	−31.06 to +22.26	−2.19 to +3.06	+0.00 to +19.72	−8.57 to +0.00	−25.81 to +41.66	−10.67 to +1.95
RISC	−30.98 to +22.33	−2.20 to +3.05	+0.00 to +19.72	−8.57 to +0.00	−26.47 to +42.03	−10.76 to +1.94
b18	−32.33 to +22.22	−2.19 to +3.18	+0.00 to +19.72	−8.57 to +0.00	−27.87 to +41.89	−10.74 to +1.78
des_perf	−32.21 to +22.29	−2.19 to +3.17	+0.00 to +19.72	−8.57 to +0.00	−26.47 to +41.65	−10.68 to +1.87
vga_lcd	−31.05 to +22.18	−2.18 to +3.06	+0.00 to +19.72	−8.57 to +0.00	−26.48 to +41.39	−10.68 to +1.72
b19	−30.89 to +22.33	−2.20 to +3.04	+0.00 to +19.72	−8.57 to +0.00	−26.37 to +41.45	−10.66 to +1.78

TABLE VII
LONGEST PATH DELAY (LPD) AND TOTAL NEGATIVE SLACK (TNS) COMPARISON IN ns CONSIDERING BIAXIAL STRESS

Circuit	With TSV Stress				With STI Stress				With Both TSV and STI Stresses			
	LPD		TNS		LPD		TNS		LPD		TNS	
ex	11.956	(0.63%)	−8.040	(11.43%)	11.686	(0.00%)	−5.277	(-0.06%)	11.628	(0.44%)	−4.716	(8.45%)
8051	4.993	(−7.01%)	−137.521	(−5.39%)	4.768	(0.00%)	−60.456	(0.01%)	4.726	(−0.73%)	−53.539	(−12.73%)
8086	9.514	(0.97%)	−31.776	(18.66%)	8.734	(0.00%)	−3.495	(0.00%)	8.948	(0.67%)	−8.385	(16.55%)
MAC2	8.051	(1.86%)	−104.278	(11.62%)	7.434	(−0.02%)	−46.363	(-0.38%)	7.681	(2.07%)	−61.506	(23.36%)
ethernet	9.598	(1.20%)	−478.693	(3.31%)	9.472	(0.00%)	−492.012	(-0.03%)	9.677	(1.21%)	−494.384	(2.88%)
RISC	8.605	(6.26%)	−87.493	(114.23%)	8.434	(0.00%)	−27.835	(-0.10%)	8.456	(0.82%)	−34.576	(94.47%)
b18	13.226	(3.01%)	−96.353	(55.09%)	12.013	(0.00%)	−22.024	(0.00%)	12.720	(3.35%)	−45.776	(50.92%)
des_perf	8.843	(1.41%)	−50.559	(12.22%)	8.026	(0.00%)	−10.090	(0.00%)	8.403	(1.30%)	−13.050	(13.35%)
vga_lcd	8.679	(2.63%)	−1.523	(27.85%)	7.835	(0.00%)	−0.671	(0.00%)	8.280	(2.50%)	−1.024	(17.14%)
b19	13.740	(0.89%)	−167.897	(15.37%)	12.760	(0.00%)	−43.986	(−0.02%)	12.957	(1.06%)	−55.979	(14.72%)
Average Abs. Change		(2.59%)		(27.52%)		(0.00%)		(0.06%)		(1.41%)		(25.46%)

Percentage of change from corresponding uniaxial stress is shown in parenthesis.

D. Comparison between Uniaxial and Biaxial Stresses

In this experiment, we consider biaxial TSV-induced stress when computing carrier mobility variation as described in Section VI. The hole and electron mobility variation of all circuits when only TSV stress, only STI stress, and both TSV and STI stresses are considered is shown in Table VI. When biaxial TSV-induced stress is considered, the range of carrier mobility variation increases significantly for the first and the last cases. When only STI-induced stress is considered, the results for uniaxial and biaxial stresses are not much different.

The timing results when biaxial stress is considered are shown in Table VII. When only STI-induced stress is considered, the timing results for uniaxial and biaxial stresses are not much different as well. On average, the difference between the LPD when uniaxial stress is considered and when biaxial stress is considered is less than 3%. The difference between TNS when uniaxial stress is considered and when biaxial stress is considered is more noticeable at 25%.

For some circuits (8051 and RISC), when only TSV stress is considered, the difference between the LPD under uniaxial vs. biaxial stress is noticeable. However, when both TSV and STI stresses are considered, the difference becomes negligible. The additional stress along the x-axis caused by STI stress mitigates the perceivable impact of the cause of the difference. Thus, uniaxial stress can be used with an acceptable error when the LPD is computed under both TSV and STI stresses.

IX. CONCLUSION

In this paper, we developed the first-order compact model for TSV-stress-induced mobility variation and STI-stress-induced mobility variation. We also proposed a design methodology to analyze the systematic variation and optimize layout by locating critical cells in a mobility enhanced region of TSVs or changing STIs surrounding them. Our TSV-STI-stress-aware timing analysis framework for 3-D ICs also opens the opportunity for stress-aware layout optimizations, such as placement and TSV-STI optimizations. To provide a complete picture of the impact of TSV and STI, future work includes additional consideration of the impact of STI stress in the vertical direction on the mobility and threshold voltage due to effective width narrowing.

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