

TSV Stress-Aware Full-Chip Mechanical Reliability Analysis and Optimization for 3-D IC

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Abstract—In this paper, we propose an efficient and accurate full-chip thermomechanical stress and reliability analysis tool and design optimization methodology to alleviate mechanical reliability issues in 3-D integrated circuits (ICs). First, we analyze detailed thermomechanical stress induced by through-silicon vias in conjunction with various associated structures such as landing pad and dielectric liner. Then, we explore and validate the linear superposition principle of stress tensors and demonstrate the accuracy of this method against detailed finite element analysis simulations. Next, we apply this linear superposition method to full-chip stress simulation and a reliability metric named the von Mises yield criterion. Finally, we propose a design optimization methodology to mitigate the mechanical reliability problems in 3-D ICs. Our numerical experimental results demonstrate the effectiveness of the proposed methodology.

Index Terms—3-D IC, mechanical reliability, stress, through-silicon via (TSV).

I. INTRODUCTION

DUE TO THE coefficients of thermal expansion (CTE) mismatch between through-silicon via (TSV) fill material, such as copper (Cu), and silicon substrate, thermomechanical stress is induced during fabrication process and thermal cycling of TSV structures. This thermomechanical stress can affect device performance [1] or drive crack growth in 3-D interconnects [2], [3]. Most previous works focused on modeling the thermomechanical stress and reliability of a single TSV in isolation. These simulations are performed using finite element analysis (FEA) methods that are computationally expensive or infeasible for full-chip analysis. Furthermore, some works used unrealistic TSV structures, such as an extremely large landing pad (LP), mainly because the design context is not considered.

In this paper, we propose a full-chip TSV thermomechanical stress and reliability analysis flow as well as a design optimization

methodology to reduce mechanical reliability problems in TSV-based 3-D integrated circuits (ICs). We use von Mises yield criterion as a mechanical reliability metric and show impacts of design parameters, such as TSV size, LP size, liner thickness, and keep-out-zone (KOZ) size, on the mechanical reliability.

The main contributions of this paper include the following.

- 1) *Modeling*: Compared with existing works, we simulate more detailed and realistic TSV structures and study their impact on stress as well as a mechanical reliability metric. We also model the impact of chip operating temperature on stress and reliability.
- 2) *Full-chip analysis*: We validate the principle of linear superposition of stress tensors against FEA simulations and apply this methodology to generate a stress map and a reliability metric map on a full-chip scale.
- 3) *Design optimization*: We present design methods to reduce von Mises stress, which is a mechanical reliability metric, on full-chip 3-D IC designs by tuning design parameters, such as LP size, liner thickness, KOZ size, and TSV placement.

II. DETAILED BASELINE MODELING

The analytical 2-D radial stress model, known as *Lamé* stress solution, was employed to address the TSV thermomechanical stress effect on device performance in [1]. This 2-D plane solution assumes an infinitely long TSV embedded in an infinite silicon substrate and provides stress distribution in silicon substrate region, which can be expressed as follows [4]:

$$\begin{aligned}\sigma_{rr}^{\text{Si}} &= -\sigma_{\theta\theta}^{\text{Si}} = -\frac{E\Delta\alpha\Delta T}{2} \left(\frac{D_{\text{TSV}}}{2r}\right)^2 \\ \sigma_{zz}^{\text{Si}} &= \sigma_{rz}^{\text{Si}} = \sigma_{\theta z}^{\text{Si}} = \sigma_{r\theta}^{\text{Si}} = 0\end{aligned}\quad (1)$$

where σ^{Si} is stress in silicon substrate, E is Young's modulus, $\Delta\alpha$ is mismatch in CTE, ΔT is differential thermal load, r is the distance from TSV center, and D_{TSV} is TSV diameter.

Even though this closed-form formula is easy to handle, the 2-D solution is applicable only to the structure with TSV and substrate, hence inappropriate for the realistic TSV structure with LP and liner. Also, it does not capture the 3-D nature of a stress field near the wafer surface around TSVs where devices are located. Moreover, the TSV-substrate interface region near the wafer surface is known to be a highly problematic area for mechanical reliability [3]. In our paper, the wafer surface

Manuscript received June 18, 2011; revised October 24, 2011 and December 27, 2011; accepted February 7, 2012. Date of current version July 18, 2012. This work was supported in part by the National Science Foundation, under Grants CCF-1018216 and CCF-1018750, in part by the SRC Interconnect Focus Center, in part by the IBM Faculty Award, and in part by Intel Corporation. This paper was recommended by Associate Editor Y.-W. Chang.

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Digital Object Identifier 10.1109/TCAD.2012.2188400

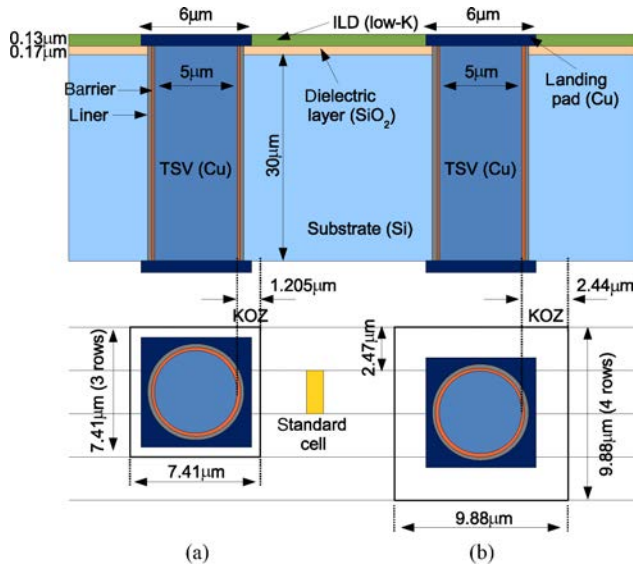


Fig. 1. Baseline TSV structure. (a) TSV_A cell occupying three standard cell rows (KOZ = 1.205 μm). (b) TSV_B cell occupying four standard cell rows (KOZ = 2.44 μm).

TABLE I
MATERIAL PROPERTIES

Material	CTE (ppm/K)	Young's Modulus (GPa)	Poisson's Ratio
Cu	17	110	0.35
Si	2.3	130	0.28
SiO ₂	0.5	71	0.16
Low K	20	9.5	0.3
BCB	40	3	0.34
Ti	8.6	116	0.32
Ta	6.8	186	0.34

means the silicon surface right below substrate (Si)–dielectric layer (SiO₂) interface.

Although the authors in [3] proposed a semianalytic 3-D stress model, it is only valid for TSV with a high aspect ratio. Also, their TSV structure only includes TSV and silicon substrate, hence we cannot apply their model to TSV that contains LP and dielectric liner because of the change in boundary conditions. Furthermore, since their model is only applicable to a single TSV in isolation, it cannot be directly used to assess mechanical reliability issues in a full-chip scale.

Since there is no known analytical stress model for a realistic TSV structure, 3-D FEA models for a TSV structure are created to investigate the stress distribution near wafer surface. To realistically examine the thermomechanical stress induced by TSVs, our baseline simulation structure of a TSV is based on the fabricated and the published data [2], [5]–[7] as shown in Fig. 1.

We construct two TSV cells, i.e., TSV_A and TSV_B, which occupy three and four standard cell rows in NCSU 45-nm technology [8]. We define 1.205 μm and 2.44 μm from TSV edge as KOZ in which no cell is allowed to be placed for TSV_A and TSV_B cells, respectively. Our KOZ sizes are slightly larger than the one for the single TSV case for digital circuits in [9]. Our baseline TSV diameter, height, Cu diffusion barrier

thickness, liner thickness, and LP size are 5 μm, 30 μm, 50 nm, 125 nm, and 6 μm, respectively, unless specified, which are close to the data in [5]. We use SiO₂ and Ti as a baseline liner and a Cu diffusion barrier material, respectively. The material properties used for our experiments are listed in Table I. We use the FEA simulation tool ABAQUS to perform experiments, and all materials are assumed to be linear elastic and isotropic. Also, perfect adhesion is assumed at all material interfaces [10].

A. 3-D FEA Simulation

Before discussing the detailed stress modeling results, we introduce the concept of a stress tensor. Stress at a point in an object can be defined by the nine-component stress tensor as follows:

$$\sigma = \sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix}$$

where the first index i indicates that the stress acts on a plane normal to the i axis and the second index j denotes the direction in which the stress acts. If index i and j are same, we call this a normal stress, otherwise a shear stress. Since we adopt a cylindrical coordinate system in this modeling for the cylindrical TSV, indexes 1, 2, and 3 represent r , θ , and z , respectively.

B. Impact of TSV Liner and LP

Fig. 2 shows FEA simulation results of normal stress components σ_{rr} , $\sigma_{\theta\theta}$, and σ_{zz} along an arbitrary radial line from the TSV center at the wafer surface with $\Delta T = -250^\circ\text{C}$ of thermal load. That is, we assume TSV structure is annealed at 275 °C and cooled down to 25 °C to mimic the manufacturing process [3], [4], [11]. We also assume that the entire TSV structure is stress free at the annealing temperature.

In our 3-D FEA simulations, we consider TSV surrounding structures such as dielectric liner and LP, while the 2-D model considers only TSV and substrate that are infinitely long in z -direction. Due to this structural difference, we observe the huge discrepancy between 2-D solution and 3-D stress results at the TSV edge. It is widely known that most of mechanical reliability failures occur at the interface between different materials, hence this TSV edge is the critical region for the reliability. Therefore, 2-D solution does not predict mechanical failure mechanism for TSVs correctly. Also, SiO₂ liner, which acts as a stress buffer layer, reduces σ_{rr} stress at the TSV edge by 35 MPa compared with the case without LP and liner. The LP also helps decrease stress magnitude at the TSV edge.

We also employ benzocyclobutene (BCB), a polymer dielectric material, as an alternative TSV liner material [3], [4]. Since Young's modulus, which is a measure of the stiffness of an elastic material, of BCB is much lower than Cu, Si, and SiO₂, this BCB liner can absorb the stress effectively induced by CTE mismatch. Fig. 3 shows the impact of liner material and its thickness on σ_{rr} stress component. As liner thickness increases, stress magnitude at the TSV edge noticeably decreases, especially for the BCB liner case.

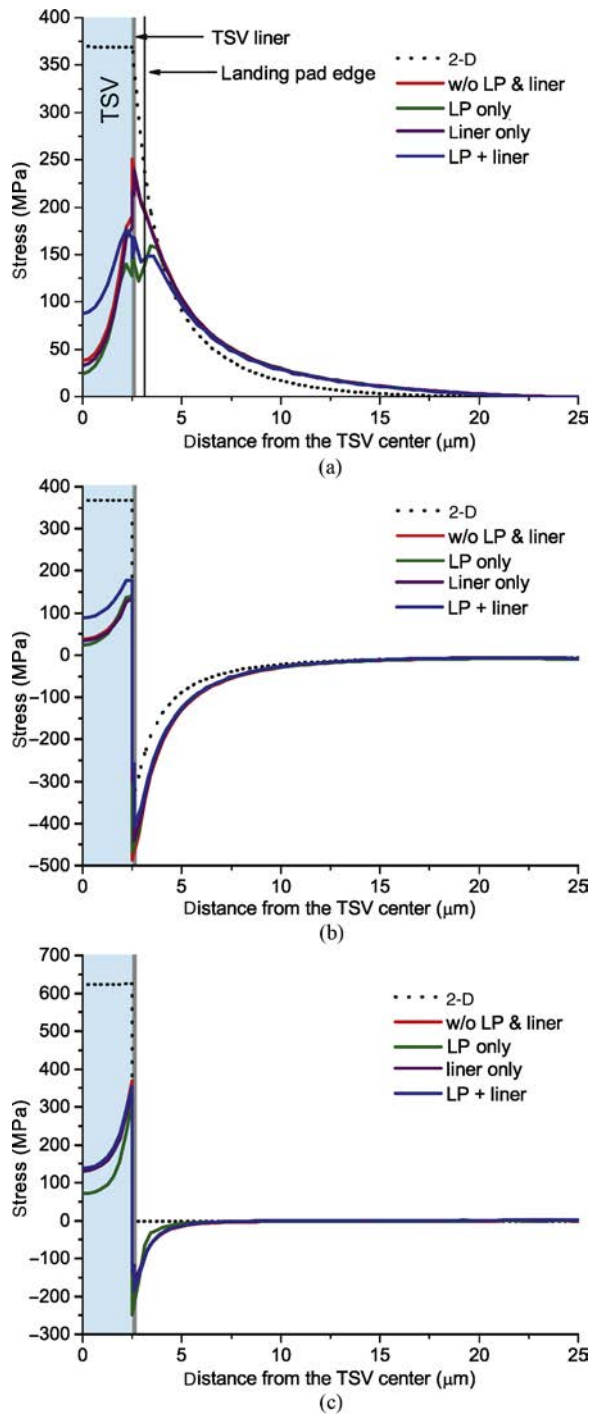


Fig. 2. Effect of TSV structures on normal stress components. (a) σ_{rr} stress. (b) $\sigma_{\theta\theta}$ stress. (c) σ_{zz} stress.

It is evident from these experiments that modeling stress distribution considering surrounding structures such as liner and LP is important to analyze the thermomechanical stress around TSVs more accurately. We construct a stress library by varying TSV diameter/height, LP size, and liner material/thickness to enable full-chip thermomechanical stress and reliability analysis with different TSV structures.

C. Impact of Cu Diffusion Barrier

For Cu-based interconnects, a barrier layer is needed to prevent Cu diffusion into both dielectrics and Si substrate.

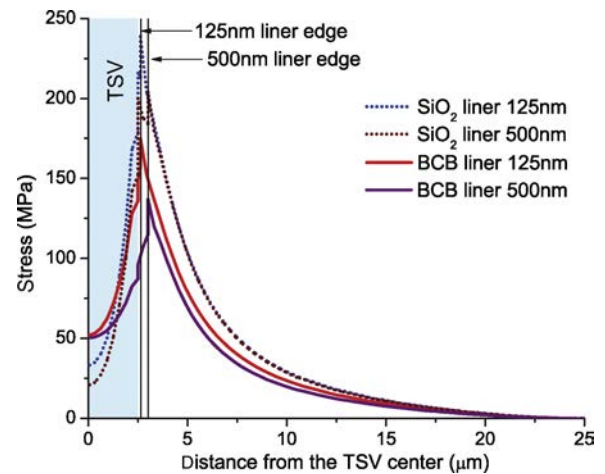


Fig. 3. Effect of liner material/thickness on σ_{rr} stress.

TABLE II
EFFECT OF YOUNG'S MODULUS OF BARRIER MATERIAL ON
VON MISES STRESS AT TSV-BARRIER INTERFACE

	Young's Modulus (GPa)								
	25	50	75	100	125	150	175	200	225
Stress (MPa)	559	572	575	612	674	740	806	875	943

Young's modulus of Ta changes while CTE and Poisson's ratio remain the same.

This Cu diffusion induces degradation of dielectric layers, hence forms mid-gap defects in Si substrate. These defects serve as a recombination center and reduce the minority carrier lifetime [12]. Therefore, Cu diffusion barrier is deposited between Cu TSV and dielectric liner.

Some previous works ignored Cu diffusion barrier material such as Ti and Ta in FEA simulations, since this barrier thickness is only a small fraction of SiO₂ liner thickness, e.g., one-tenth of liner thickness in general. Hence, its impact on stress distribution is negligible [2], [6].

However, thermomechanical stress is highly dependent on Young's modulus as well as CTE mismatch. As shown in Table I, CTE of both Ti and Ta are in between Cu and Si, hence it is unlikely that these barrier materials induce additional stress around TSV on top of stress induced by CTE mismatch between Cu and Si. However, Ta is the stiffest material used in this paper. Materials with high Young's modulus cannot absorb stress efficiently. Thus, there is a high chance of stress build-up at this TSV-barrier (Ta) interface.

Fig. 4 shows the impact of both Ta and Ti barrier material on the stress and mechanical reliability around TSV. In this experiment, we use a 500-nm-thick SiO₂ liner and 50-nm and 100-nm-thick Ta and Ti barrier. We observe a huge increase in stress magnitude in the case of Ta barrier at TSV-barrier interface. For example, in the case of $\sigma_{\theta\theta}$ stress component shown in Fig. 4(a), we see 241 MPa and 232 MPa increase in compressive stress at TSV-barrier interface for 50-nm and 100-nm-thick Ta barriers, respectively, compared with no barrier case. However, there is a negligible change in stress with Ti barrier. This stress increase with Ta barrier also worsens von Mises stress, which is a reliability metric

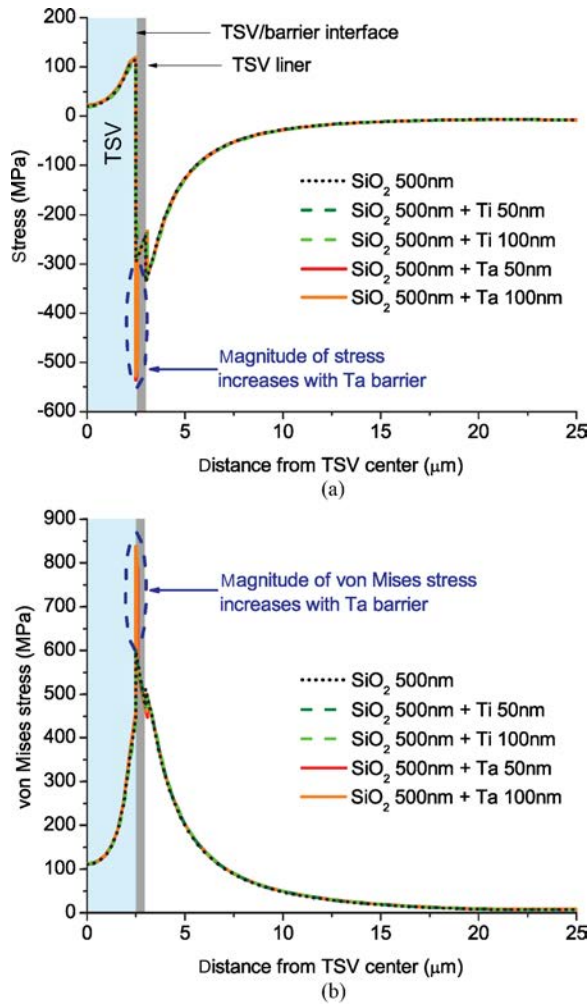


Fig. 4. Effect of Cu diffusion barrier on stress. (a) $\sigma_{\theta\theta}$ stress. (b) von Mises stress.

and is discussed in detail in Section III-C, as shown in Fig. 4(b).

To further verify that Young's modulus is the key parameter affecting stress magnitude at TSV–barrier interface, we change Young's modulus of Ta from 25 GPa to 225 GPa with 25 GPa step while CTE and Poisson's ratio are unchanged. Table II thus shows that as Young's modulus increases, maximum von Mises stress at TSV–barrier interface increases as well. Therefore, barrier material for Cu TSV should be chosen carefully to suppress additional mechanical reliability problem on top of existing concerns. Thus, we use Ti as a Cu diffusion barrier material throughout this paper.

D. Stress Influence Zone

The magnitude of thermomechanical stress induced by TSV is highest at the TSV edge. However, as Fig. 2 shows, the magnitude of every normal stress component decays fast, and at around $25\ \mu\text{m}$ from the TSV center, stress is almost negligible. For efficient and fast full-chip stress analysis, it is crucial to confine stress analysis to the manageable extent. Thus, we define a stress influence zone as a circle with a radius of $25\ \mu\text{m}$ from the TSV center for our baseline TSV with $5\ \mu\text{m}$

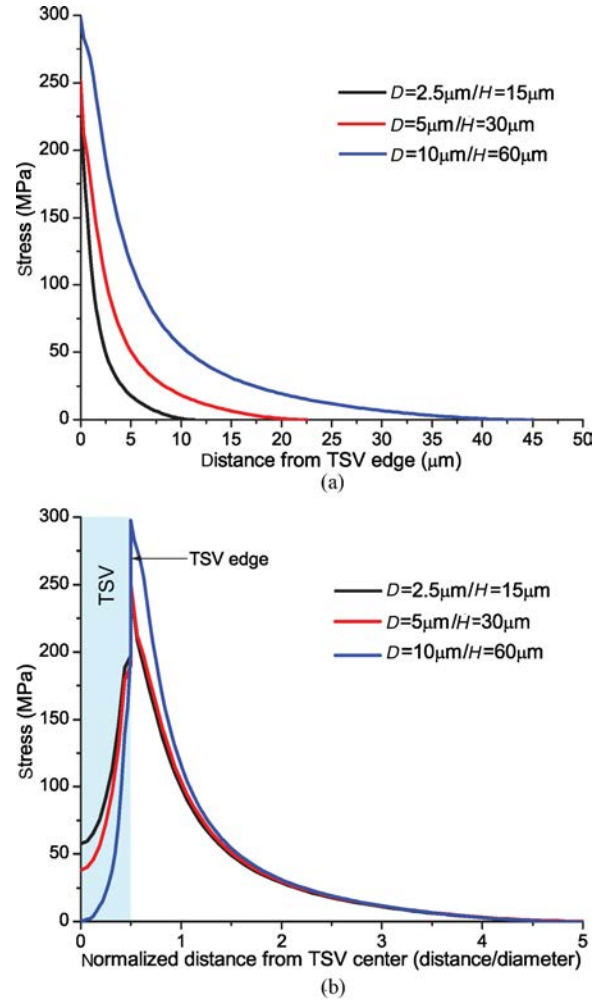


Fig. 5. Effect of TSV size on stress influence zone. (a) σ_{rr} stress from TSV edge. (b) σ_{rr} stress along normalized distance (distance/TSV diameter).

diameter. Beyond the stress influence zone, we neglect stress induced by the TSV under consideration.

We further investigate the impact of TSV size on stress influence zone. We use three different TSV diameters with a same aspect ratio of 6: TSV small ($H/D = 15/2.5\ \mu\text{m}$), TSV medium ($H/D = 30/5\ \mu\text{m}$), and TSV large ($H/D = 60/10\ \mu\text{m}$), where H/D is TSV height/diameter. Fig. 5(a) shows the magnitude of σ_{rr} stress component from TSV edge, and we see that stress magnitude of smaller TSV decays and reaches zero faster.

Fig. 5(b) shows stress magnitude along the normalized distance from TSV center, i.e., r/D_{TSV} , where r is the distance from TSV center and D_{TSV} is the TSV diameter. Even though there are differences in stress magnitude inside TSV and up to $1 \times \text{TSV diameter}$, stress magnitudes are almost identical beyond that distance. In the 2-D solution shown in (1), we see that magnitude of σ_{rr}^{Si} and $\sigma_{\theta\theta}^{\text{Si}}$ is proportional to $(D_{\text{TSV}}/2r)^2$. That is why we observe similar stress curve along the normalized distance.

Most importantly, we observe that stress magnitude becomes negligible at around $5 \times \text{TSV diameter}$ for all three cases. Therefore, we set stress influence zone as $5 \times \text{TSV diameter}$ in our paper.

E. Anisotropic Material Property of Silicon

Up to this point, all materials are assumed to be isotropic for simplicity. However, Si is an anisotropic material with elastic behavior that depends on which crystal direction the structure is being stretched. The possible values of Young's modulus (E) for Si range from 130 GPa to 188 GPa and those for Poisson's ratio (ν) range from 0.048 to 0.4. Thus, the choice of this value can affect analysis results significantly [13]. Also, recent study showed that TSV-induced stress measurement data matches well with FEA simulation results with anisotropic Si material property [14]. In this section, we examine the impact of anisotropic material property of Si on stress distribution compared with the isotropic material property.

Elasticity is the relationship between stress (σ) and strain (ϵ). Hooke's law describes this relationship in terms of stiffness C , i.e., $\sigma = C\epsilon$. For isotropic uniaxial cases, stiffness C can be represented by a single value of Young's modulus E . In an anisotropic material, a fourth-rank stiffness tensor with $3^4 = 81$ terms is required to describe the elasticity. Fortunately, due to cubic symmetry of Si, the elastic properties can be expressed in terms of orthotropic material constants. An orthotropic material is one that contains at least two orthogonal planes of symmetry, and Si, with cubic symmetry, can be described this way. The orthotropic elasticity of Si can be expressed with reference axes of a standard (100) Si wafer, which are [110], $[\bar{1}10]$, and [001], as follows:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{bmatrix} = \begin{bmatrix} c1 & c5 & c6 & 0 & 0 & 0 \\ c5 & c1 & c6 & 0 & 0 & 0 \\ c6 & c6 & c2 & 0 & 0 & 0 \\ 0 & 0 & 0 & c3 & 0 & 0 \\ 0 & 0 & 0 & 0 & c3 & 0 \\ 0 & 0 & 0 & 0 & 0 & c4 \end{bmatrix} \begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{yz} \\ \epsilon_{zx} \\ \epsilon_{xy} \end{bmatrix}$$

where orientation specific constants $c1$, $c2$, $c3$, $c4$, $c5$, and $c6$ are 194.5, 165.7, 79.6, 50.9, 35.7, and 64.1, all in GPa, respectively. This stiffness tensor translates to $E_x = E_y = 169$ GPa, $E_z = 130$ GPa, $\nu_{yz} = 0.36$, $\nu_{zx} = 0.28$, and $\nu_{xy} = 0.064$ [13].

Fig. 6 shows stress comparison between anisotropic and isotropic Si (Young's modulus = 130 GPa and Poisson's ratio = 0.28) material properties. We see that stress magnitude with anisotropic Si is significantly higher than isotropic Si case largely due to higher Young's modulus, especially along x -direction as shown in Fig. 6(a). We also observe the same trend in y -direction ($=\sigma_{yy}$ stress). However, there is a small difference in z -direction stress component compared with other directions shown in Fig. 6(b). This can be explained by the same Young's modulus $E_z = 130$ GPa for both anisotropic and isotropic Si.

In general, we observe higher stress level by adopting anisotropic Si material property compared with isotropic Si case mostly due to higher Young's modulus. Although FEA simulation with isotropic Si provides a good understanding of stress distribution, proper material properties need to be used to accurately assess thermomechanical reliability of TSV-based 3-D ICs.

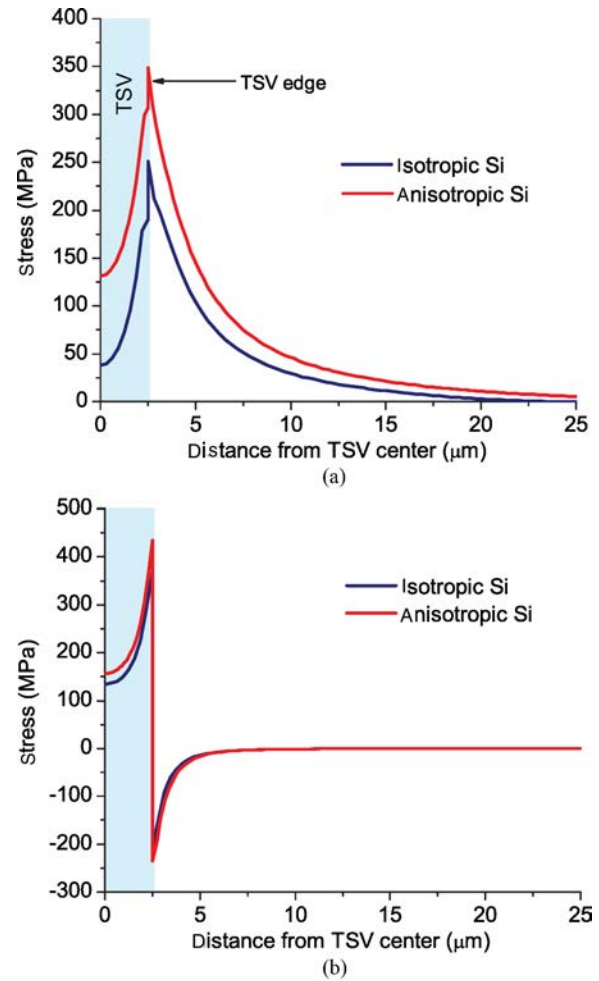


Fig. 6. Effect of anisotropic Si material property on stress. (a) σ_{xx} stress. (b) σ_{zz} stress.

III. FULL-CHIP RELIABILITY ANALYSIS

FEA simulation of thermomechanical stress for multiple TSVs require huge computing resources and time, thus it is not suitable for full-chip analysis. In this section, we present a full-chip thermo-mechanical stress and reliability analysis flow. To enable a full-chip stress analysis, we first explore the principle of linear superposition of stress tensors from individual TSVs. Based on the linear superposition method, we build full-chip stress map and then compute von Mises yield metric to predict mechanical reliability problems in TSV-based 3-D ICs.

A. Linear Superposition Principle

A useful principle in the analysis of linearly elastic structures is that of superposition. The principle states that if the displacements at all points in an elastic body are proportional to the forces producing them, the body is linearly elastic. The effect, i.e., stresses and displacements, of a number of forces acting simultaneously on such a body is the sum of the effects of the forces applied separately. We apply this principle to compute the stress at a point by adding the individual stress tensors at that point caused by each TSV as follows:

$$S = \sum_{i=1}^n S_i$$

where S is the total stress at the point under consideration and S_i is the individual stress tensor at this point due to the i th TSV.

B. Stress Analysis With Multiple TSVs

First, based on the observation that the stress field of a single TSV in isolation is radially symmetrical due to the cylindrical shape of a TSV, we obtain stress distribution around a TSV from a set of stress tensors along an arbitrary radial line from the TSV center in a cylindrical coordinate system. To evaluate a stress tensor at a point affected by multiple TSVs, a conversion of a stress tensor to a Cartesian coordinate system is required. This is due to the fact that we extract stress tensors from a TSV whose center is the origin in the cylindrical coordinate system; hence, we cannot perform a vector sum of stress tensors at a point from each TSV that has a different center location. That is why we need a universal coordinate system, i.e., Cartesian coordinate system in our case.

Then, we compute a stress tensor at the point of interest by adding up stress tensors from TSVs affecting this point. We set a TSV stress influence zone as $25 \mu\text{m}$ from the center of a TSV with $5 \mu\text{m}$ diameter, as discussed in Section II-D.

Let the stress tensor in Cartesian and cylindrical coordinate system be S_{xyz} and $S_{r\theta z}$, respectively, as follows:

$$S_{xyz} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix}, S_{r\theta z} = \begin{bmatrix} \sigma_{rr} & \sigma_{r\theta} & \sigma_{rz} \\ \sigma_{\theta r} & \sigma_{\theta\theta} & \sigma_{\theta z} \\ \sigma_{zr} & \sigma_{z\theta} & \sigma_{zz} \end{bmatrix}.$$

The transform matrix Q is in the form as follows:

$$Q = \begin{bmatrix} \cos \theta & -\sin \theta & 0 \\ \sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

where θ is the angle between the x -axis and a line from the TSV center to the simulation point. A stress tensor in a cylindrical coordinate system can be converted to a Cartesian coordinate system using conversion matrices $S_{xyz} = Q S_{r\theta z} Q^T$.

C. Mechanical Reliability Analysis

In order to evaluate if computed stresses indicate possible reliability concerns, a critical value for a potential mechanical failure must be chosen. The von Mises yield criterion is known to be one of the most widely used mechanical reliability metric [15]–[17]. If the von Mises stress exceeds a yielding strength, material yielding starts. Prior to the yielding strength, the material will deform elastically and will return to its original shape when the applied stress is removed. However, if the von Mises stress exceeds the yielding point, some fraction of the deformation will be permanent and nonreversible even if applied stress is removed.

There is a large variation of yielding strength of Cu in the literature, from 225 MPa to 600 MPa, and it has been reported to depend upon thickness, grain size, and temperature [15]. We use 600 MPa as a yielding strength of Cu in our experiments. The yielding strength of silicon is 7000 MPa, which will not be reliability concerns for the von Mises yield criterion.

TABLE III
VON MISES STRESS COMPARISON BETWEEN FEA SIMULATIONS AND
LINEAR SUPERPOSITION METHOD

# TSV	FEA		Linear Superposition		Max % Error	
	# Node	Runtime	# Simulation Point	Runtime	Inside TSV	Outside TSV
1	153K	21 m 35 s	1.M	20.63 s	1.0	-0.4
2	282K	58 m 11 s	1.2M	26.21 s	3.3	-0.8
3	358K	1 h 28 m 24 s	1.44M	36.43 s	4.8	-1.3
5	546K	1 h 59 m 05 s	1.68M	56.02 s	12.7	-1.9
10	1124K	4 h 34 m 14 s	2.24M	65.32 s	13.6	-2.0

The von Mises stress is a scalar value at a point that can be computed using components of a stress tensor shown as follows:

$$\sigma_v = \sqrt{\frac{(\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{zz} - \sigma_{xx})^2 + 6(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{zx}^2)}{2}}. \quad (2)$$

By evaluating von Mises stress at the interface between TSV and dielectric liner, where highest von Mises stress occurs, we can predict mechanical failures in TSVs.

D. Validation of Linear Superposition Method

In this section, we validate the linear superposition of stress tensors against FEA simulations by varying the number of TSVs and their arrangement. We set minimum TSV pitch as $10 \mu\text{m}$ for all test cases. Stress tensors along a radial line from the TSV center in a single TSV structure (stress tensor list) are obtained through FEA simulation with $0.1 \mu\text{m}$ interval. In our linear superposition method, simulation area is divided into uniform array style grid with $0.05 \mu\text{m}$ pitch. If the stress tensor at a grid point under consideration is not obtainable directly from the stress tensor list, we compute stress tensor at the point using linear interpolation with adjacent stress tensors in the list.

Table III shows some of our comparisons. First, we observe huge runtime reduction in our linear superposition method. Note that we perform FEA simulations using four CPUs while only one CPU is used for our linear superposition method. Even though our linear superposition method performs stress analysis on a 2-D plane at the wafer surface, whereas FEA simulation is performed on entire 3-D structure, we can perform stress analysis for other planes in a similar way if needed. Also, runtime in our linear superposition method shows linear dependency on the number of simulation points, which is closely related to the number of TSVs under consideration. Thus, our linear superposition method is highly scalable, hence applicable to full-chip scale stress simulations. More details on scalability is discussed in Section III-G.

Most importantly, error between FEA simulations and the linear superposition method is practically negligible. Results show that our linear superposition method overestimates stress magnitude inside TSV. However, though maximum % error inside TSV of ten TSVs case is as high as 13.6%, stress magnitude difference between FEA and our method is only 5.0 MPa. Also, since most mechanical problem occurs at the

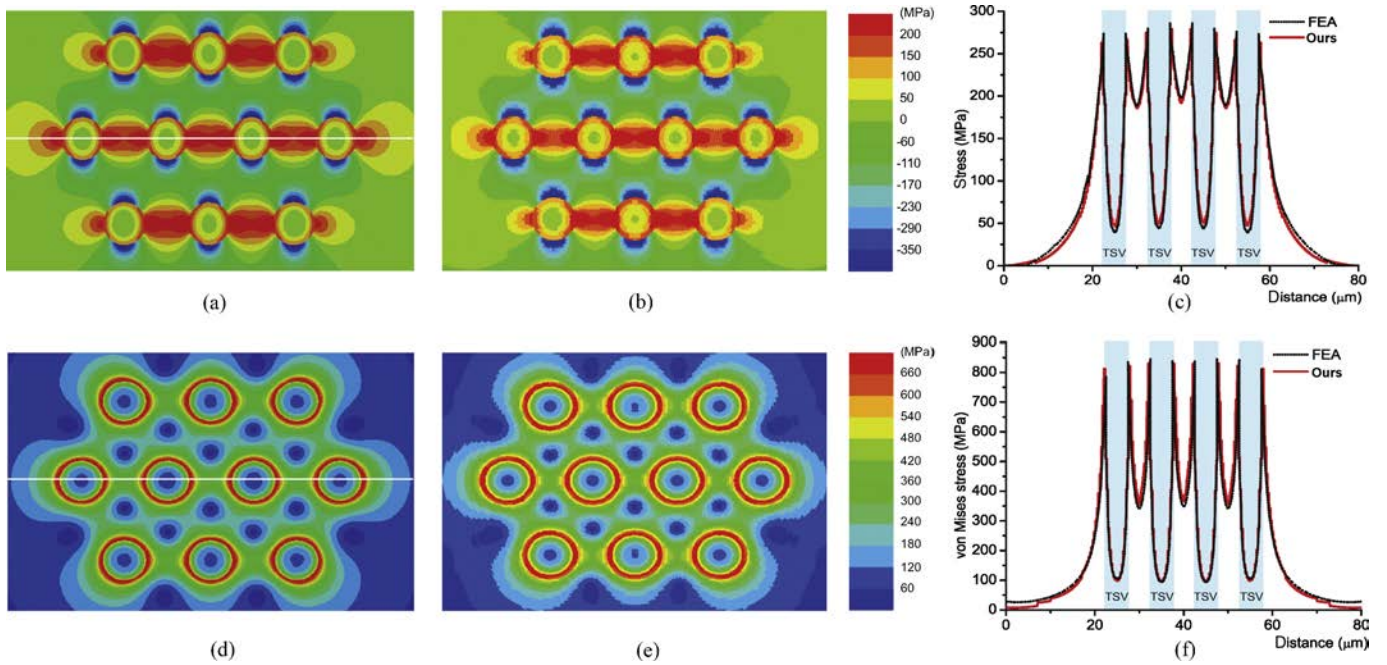


Fig. 7. Sample stress comparison between FEA simulation and linear superposition method. (a) FEA result (σ_{xx}). (b) Ours (σ_{xx}). (c) FEA versus ours (σ_{xx}) along the white line in (a). (d) FEA result (von Mises stress). (e) Ours (von Mises stress). (f) FEA versus ours (von Mises stress) along the white line in (d).

TABLE IV

ERROR IN MAXIMUM VON MISES STRESS IN MPa (AND % ERROR) AT TSV EDGE BETWEEN FEA SIMULATION AND LINEAR SUPERPOSITION FOR BOTH ISOTROPIC AND ANISOTROPIC SI

Si Property	# TSV (Pitch = 10 μm)			
	2	3	5	10
Isotropic	4.1 (0.5%)	-6.9 (-0.8%)	-5.7 (-0.7%)	-7.0 (-0.9%)
Anisotropic	-12.1 (-1%)	-16.3 (-1.4%)	-16.8 (-1.5%)	-18.3 (-1.6%)

interface between different materials, this error inside TSV does not pose a serious impact on our reliability analysis. Fig. 7 shows the stress map of σ_{xx} component and the von Mises stress map for one of test cases that contains ten TSVs, and it clearly shows that our linear superposition method matches well with the FEA simulation result.

We also examine the feasibility of linear superposition with anisotropic Si material properties. Even though elastic properties of Si depend on the orientation of the structure, fortunately, Young's modulus along x ([100]) and y ($[\bar{1}10]$) direction are same, i.e., $E_x = E_y = 169$ GPa. Since our focus is stress on the device layer, which is on the xy -plane, it is possible that the linear superposition method still holds with anisotropic Si elastic properties, though E_z is different from E_x and E_y .

Fig. 8 shows that the linear superposition method still matches well with the FEA simulation result with anisotropic Si material property. Although the error increased compared with the isotropic Si case as listed in Table IV, it is still promising to use the linear superposition method for anisotropic Si case. We also observe a huge increase in maximum von Mises stress at TSV edge, 314 MPa in this case, with anisotropic Si case due to higher Young's modulus in the xy -plane. This is expected as discussed in Section II-E.

TABLE V

MAXIMUM ERROR (IN MPa) IN VON MISES STRESS BETWEEN FEA SIMULATION AND LINEAR SUPERPOSITION

# TSV	Location	TSV Pitch (μm)				
		7.5	10	15	20	25
2	Inside	16.5	7.8	3.3	1.8	1.7
	Outside	8.9	2.8	0.7	-1.1	-0.7
3	Inside	15.4	6.9	5.5	2.5	1.6
	Outside	7.2	2.3	-1.2	-0.8	-0.5

E. Limit of Linear Superposition Method

We observe that higher % error occurs inside TSV in Section III-D. In this section, we further investigate the limit of our linear superposition method. In our approach, we first obtain stress tensors along a radial line from TSV center to substrate in a single TSV structure through FEA simulation. That is, stress tensors are obtained across at least two different materials. Then, we use linear superposition principle to compute stress tensor at a point with stress tensors that we prepared. This point under consideration could be either inside TSV (Cu) or outside TSV (silicon substrate).

In a full chip, most of simulation points are outside TSV. The stress tensor in the substrate region is computed by adding up stress tensors that are from the substrate region in a single TSV structure. In other words, all the stress tensors in the substrate region are computed by using stress tensors from the substrate region, which is the same material.

However, computing stress tensors inside TSV is different. For example, assume that there is one TSV (TSV1) that affects a point P inside another TSV (TSV2) shown in Fig. 9(a). The stress tensor from TSV1 that affects P is originated from the silicon substrate region, while the stress tensor from TSV2 that affects P is obtained from Cu. Thus, the stress tensor at

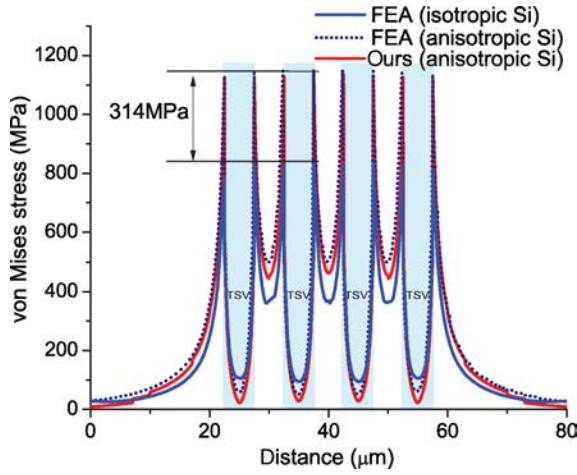


Fig. 8. von Mises stress comparison between isotropic and anisotropic Si. Stress is taken along the white line in Fig. 7(d).

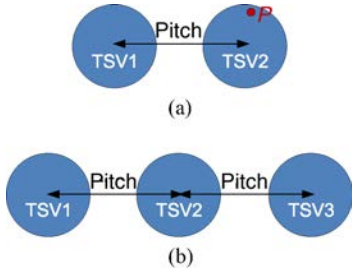


Fig. 9. Simulation structures for limit of linear superposition method. (a) Two TSVs. (b) Three TSVs.

P is calculated by adding stress tensors from two different materials.

Even though we use linear elastic model for whole structure, due to the difference in material properties between Cu and silicon, stress effect induced by nearby TSVs acting on the TSV under consideration is different between inside and outside the TSV. Therefore, error from linear superposition is inevitable, especially inside TSV.

Intuitively, if TSV pitch becomes smaller, error between FEA simulation and our approach, i.e., stress (ours)–stress (FEA), will be larger due to high stress magnitude. To further explore this, we compare two TSVs structure by varying TSV pitch from $7.5\ \mu\text{m}$ to $25\ \mu\text{m}$ shown in Fig. 9(a). Table V shows the maximum error between FEA simulation and our linear superposition method for both inside and outside TSV. For example, at $7.5\ \mu\text{m}$ pitch, error is $17.0\ \text{MPa}$ inside TSV and $8.8\ \text{MPa}$ outside TSV shown in Fig. 10(a). However, this maximum error inside TSV occurs in the TSV center where stress magnitude is lowest inside TSV, hence mechanical reliability at this location is not a concern. Also, the highest error outside TSV is found at the center location between TSVs. Nonetheless, the trend of stress magnitude remains same and the error is not significant. Moreover, $7.5\ \mu\text{m}$ pitch with $5\text{-}\mu\text{m}$ -diameter TSV is too extreme case for current TSV fabrication process. Therefore, error induced by our linear superposition method is practically negligible.

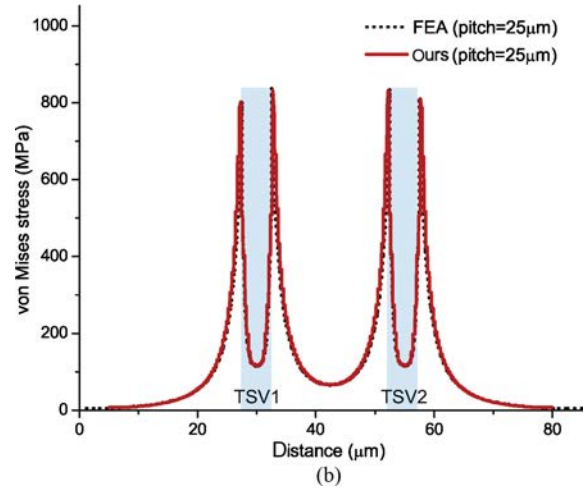
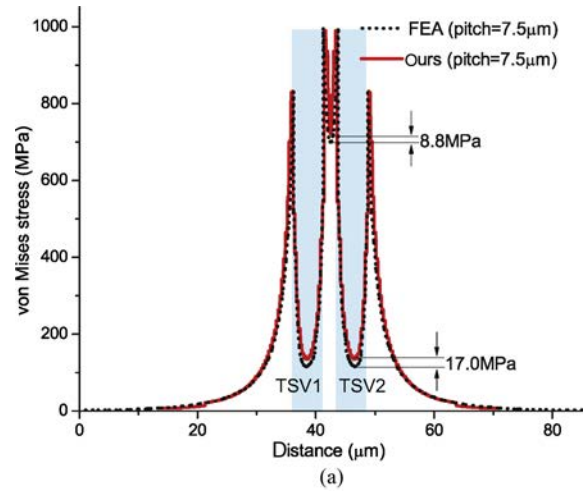


Fig. 10. von Mises stress along the center line in Fig. 9(a) with two TSVs with different pitches. (a) Two TSVs with pitch of $7.5\ \mu\text{m}$. (b) Two TSVs with pitch of $25\ \mu\text{m}$.

We further examine whether an additional TSV worsens error. We use three TSVs structure shown in Fig. 9(b). As similar to two TSVs case, maximum error occurs at TSV2 center. However, as Table V shows, an additional TSV does not aggravate simulation errors. Thus, our approach is suitable for full-chip analysis with an acceptable error.

F. Full-Chip Analysis Flow

Our full-chip thermomechanical stress and reliability analysis flow is shown in Fig. 11. We first perform a detailed FEA simulation of a single TSV and provide the stress tensors along a radial line from the TSV center as an input to our simulation engine. We also provide the locations of the TSVs from 3-D IC layout along with a thermal map to the simulation engine.

The basic algorithm for generating stress and reliability maps is illustrated in Algorithm 1. We first start to find a stress influence zone from each TSV. Then, we associate the points in the influence zone with the affecting TSV. Next, for each simulation point under consideration, we look up the stress tensor from the TSV found in the association step, and use the coordinate conversion matrices to obtain stress tensors in the Cartesian coordinate system. We visit an individual TSV affecting

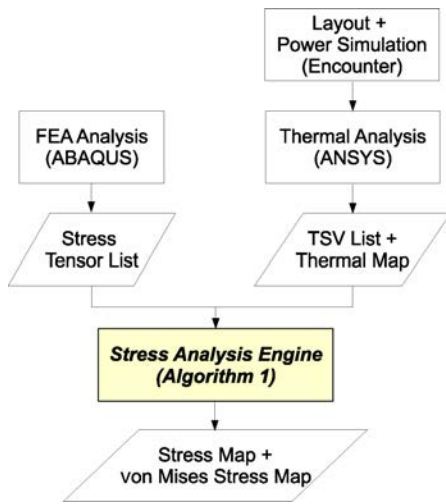


Fig. 11. Simulation flow.

this simulation point and add up their stress contributions. Once we finish the stress computation at a point, we obtain the von Mises stress value using (2). The complexity of this algorithm is $O(n)$, where n is the number of simulation points.

G. Scalability of Algorithm

To verify the scalability of our linear superposition method, we apply our algorithm to 10, 100, 1000, 10 000, and 100 000 TSVs that are regularly placed across a chip with $15 \mu\text{m}$ pitch. Note that entire chip area is divided into uniform array style grid with $0.2 \mu\text{m}$ pitch in these experiments.

Table VI shows that runtime increases almost linearly as the number of simulation points increases. Our algorithm visits each simulation point and calculates stress tensor at this point by linearly superposing stress tensors from TSVs located within a stress influence zone as shown in Algorithm 1. Since the number of TSVs affecting a single point is a small constant in most cases, the number of simulation points dominates entire runtime.

We also observe that simulation time per each grid point increases as the number of TSVs increases, and saturates beyond 10 000 TSVs case. At first, the number of TSVs that affect a point under consideration increases as total number of TSVs increases, hence a single point requires more time to compute stress tensor. However, after certain point, increasing total number of TSVs does not affect the simulation time per point. This is due to a finite stress influence zone, and hence a finite number of TSVs affecting a simulation point.

Note that these test cases in which TSVs are regularly placed across a chip are worst cases in terms of runtime. This is because almost every simulation point needs stress computation, since it is highly likely to be within a stress influence zone of a certain TSV. However, in case TSVs are only placed in some part of the chip or irregularly placed, runtime can reduce significantly since there could be nonnegligible number of simulation points that are outside of the stress influence zone of any TSVs, which are filtered out in the first *for loop* of our Algorithm 1.

Even though runtime for 100 000 TSVs case is as long as 10h, we can decrease it by parallel computing. For this, we

Algorithm 1: Full-chip stress and reliability analysis flow

Input: TSV list T , stress library, thermal map (optional)

Output: stress map, von Mises stress map

```

for each TSV  $t$  in  $T$  do
   $c \leftarrow$  center of  $t$ ;
   $r \leftarrow$  FindStressInfluenceZone( $c$ );
  for each point  $r'$  in  $r$  do
     $r'.TSV \leftarrow t$ ;
  end
end

for each simulation point  $p$  do
  if  $p.TSV \neq \emptyset$  then
    for each  $t \in p.TSV$  do
       $d \leftarrow$  distance( $t, p$ );
       $S_{cyl} \leftarrow$  FindStressTensor( $d, temperature$ );
       $\theta \leftarrow$  FindAngle(line tp, x axis);
       $Q \leftarrow$  SetConversionMatrix( $\theta$ );
       $S_{Cart} \leftarrow Q S_{cyl} Q^T$ ;
       $p.S_{Cart} \leftarrow p.S_{Cart} + S_{Cart}$ ;
    end
  end
   $vonMises(p) \leftarrow$  ComputeVonMises( $p.S_{Cart}$ );
end
  
```

TABLE VI
SCALABILITY TO FULL-CHIP ANALYSIS

# TSV	Area ($\mu\text{m} \times \mu\text{m}$)	# Simulation Point	Runtime	Time/Point
10	60×60	90K	3.6 s	$40 \mu\text{s}$
100	165×165	680K	25.4 s	$37 \mu\text{s}$
1000	495×495	6.1M	5 m 55 s	$58 \mu\text{s}$
10 000	1515×1515	57.4M	1 h 3 m	$66 \mu\text{s}$
100 000	4770×4770	568.8M	10 h 12 m	$65 \mu\text{s}$

TABLE VII
BENCHMARK CIRCUITS

Circuit	TSV Placement	TSV Cell Size ($\mu\text{m} \times \mu\text{m}$)	Wirelength (mm)	Area ($\mu\text{m} \times \mu\text{m}$)
Irreg _A	Irregular	7.41×7.41	9060	960×960
Reg _A	Regular	7.41×7.41	9547	960×960
Irreg _B	Irregular	9.88×9.88	8884	1000×1000
Reg _B	Regular	9.88×9.88	9648	1000×1000

first divide entire chip area by a user-defined window. To avoid any mismatch while merging subsolutions, we need to consider TSVs that are located outside the current window but affect the point inside the current window. For example, in the case of $5\text{-}\mu\text{m}$ -diameter TSV whose influence zone is $25 \mu\text{m}$, we need to compute stress from TSVs located within both $25 \mu\text{m}$ distance from each side of the window in outward direction and the current window. Then, we can compute stress considering all TSVs affecting the window under consideration, and each subsolution becomes independent of other subsolutions. Therefore, full-chip thermomechanical stress and reliability analysis is scalable with our approach.

IV. FULL-CHIP SIMULATION RESULTS

We implement a TSV-aware full-chip stress and reliability analysis flow in JAVA and C++. Four variations of an industrial circuit, with changes in TSV placement style and

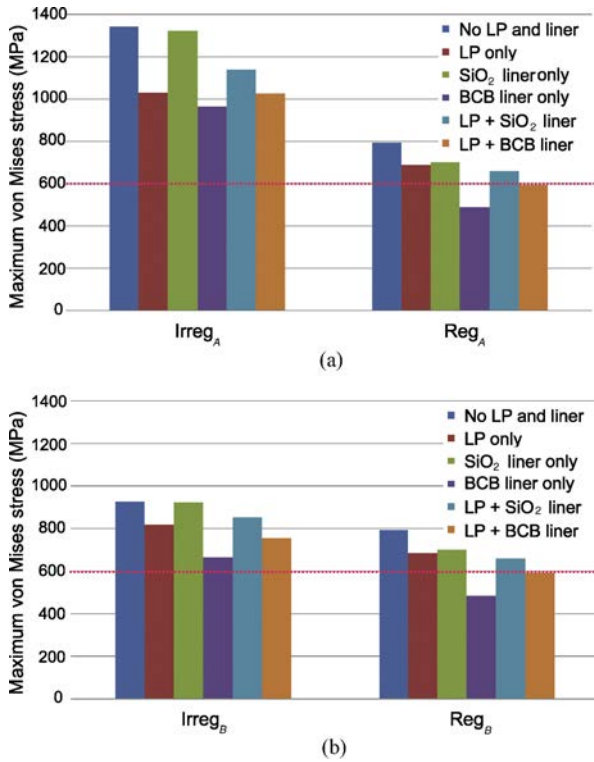


Fig. 12. Impact of TSV structure, TSV placement style, and KOZ size on the maximum von Mises stress. (a) Designs with TSV_A cell (KOZ = 1.205 μm). (b) TSV_B cell (KOZ = 2.44 μm).

TSV cell size, are used for our analysis, which are listed in Table VII. The number of TSVs and gates are 1472 and 370K, respectively, for all cases. These circuits are synthesized using Synopsys Design Compiler with the physical library of 45-nm technology, and final layouts are obtained using Cadence SoC Encounter. All circuits are designed to two-die-stacked 3-D ICs.

We use our in-house 3-D placer for TSV and cell placement, and details of TSV and cell placement algorithms can be found in [18]. In the regular TSV placement scheme, we preplace TSVs uniformly on each die, and then place cells, while TSVs and cells are placed simultaneously in the irregular TSV placement scheme. The irregular TSV placement shows better wirelength than the regular case [18]. We use a gate-level 3-D IC design methodology for these circuits as a baseline and compare these with block-level designs in Section IV-G.

A. Overall Comparison

In this section, we discuss the impact of TSV structure, TSV placement style, and KOZ size on the thermomechanical reliability in 3-D ICs. We perform full-chip stress and reliability analysis on our benchmark circuits based on our stress modeling results with different TSV structures.

Fig. 12 shows the maximum von Mises stress in our benchmark circuits. We first observe that designs with irregular TSV placement show worse maximum von Mises stress than those with the regular TSV placement. This is mainly because TSVs can be placed closely in case of the irregular TSV placement scheme to minimize wirelength. Fig. 13 shows the

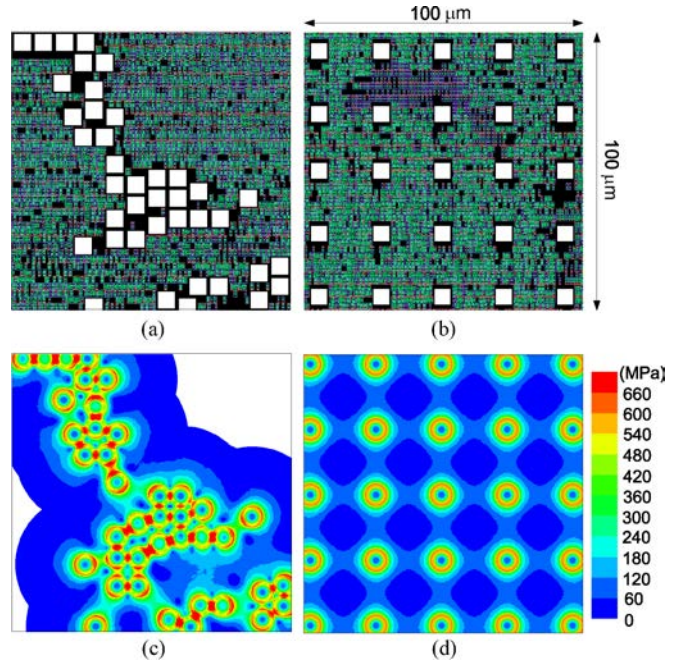


Fig. 13. Closeup shots of layouts and von Mises stress maps. (a) Irreg_A. (b) Reg_A. (c) von Mises stress map of Irreg_A. (d) von Mises stress map of Reg_A.

part of von Mises stress maps of Irreg_A and Reg_A circuits, and we see that most of TSVs in the Irreg_A circuit exceed Cu yielding strength (600 MPa).

Second, as the KOZ size becomes larger, stress level reduces significantly for the irregular TSV placement case. By enlarging the KOZ size, i.e., increasing TSV cell size in our design flow, TSV pitch increases accordingly. This in turn reduces stress interference between nearby TSVs and hence decreases von Mises stress level of TSVs. However, for the regular TSV placement case, since the TSV pitch of Reg_A (23.5 μm) and Reg_B (25 μm) is similar and also interference from nearby TSVs is negligible at this distance, there is no noticeable difference in maximum von Mises stress.

Third, these results show the importance of using an accurate TSV stress model to assess the mechanical reliability of 3-D ICs. There are significant differences in the von Mises stress depending on the existence of structures surrounding a TSV, such as LP or liner. It is possible that we might overestimate the reliability problems by using a simple TSV stress model not considering LP or liner. However, most of these test cases violate the von Mises yield criterion for Cu TSV. Section IV-E shows how TSV liners help reduce the violations.

B. Impact of TSV Pitch

TSV pitch is the key factor that determines stress magnitude in the substrate region between TSVs. In this section, we explore the effect of TSV pitch on von Mises stress. We place TSVs regularly on a 1 × 1 mm² chip. We use 1600, 2500, 4356, and 10000 TSVs whose pitches are 25, 20, 15, and 10 μm, respectively. We obtain two datasets: one without LP, liner,

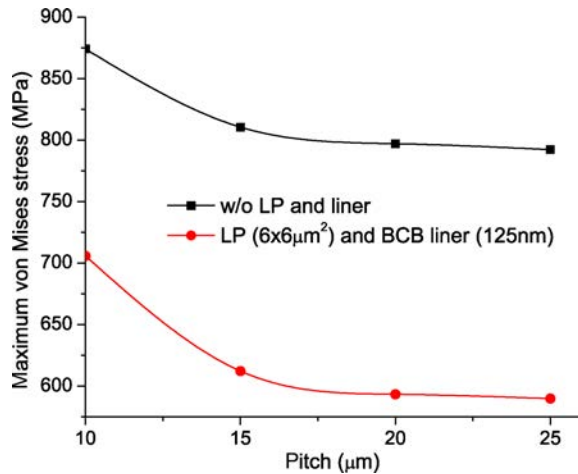


Fig. 14. Impact of TSV pitch on maximum von Mises stress.

TABLE VIII
IMPACT OF TSV SIZE ON THE MAXIMUM VON MISES STRESS

TSV Placement	Max von Mises Stress (MPa)		
	TSV Large	TSV Medium	TSV Small
Irregular	1224.6	1126.4 (8% ↓)	902.7 (26% ↓)
Regular	749.3	654.6 (13% ↓)	449.3 (40% ↓)

Numbers in parentheses are % reduction compared to TSV large case.

TABLE IX
IMPACT OF A LP SIZE ON VON MISES CRITERION

Circuit	LP $6 \times 6 \mu\text{m}^2$		LP $8 \times 8 \mu\text{m}^2$	
	Max Stress (MPa)	# Violating TSVs	Max Stress (MPa)	# Violating TSVs
Irreg _B	839.6	1472	815.3 (3% ↓)	1472 (0% ↓)
Reg _B	654.2	1472	606.7 (7% ↓)	1472 (0% ↓)

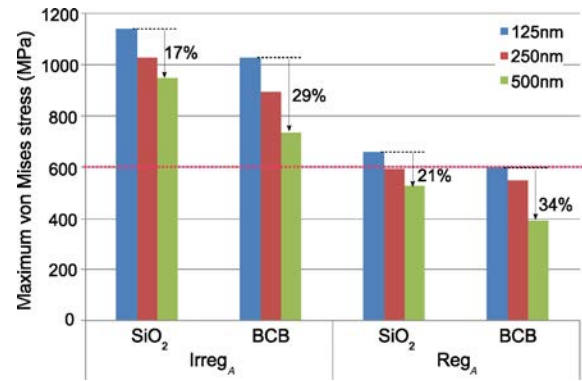
Numbers in parentheses are % reduction compared to LP $6 \times 6 \mu\text{m}^2$ case.

and barrier, and another with $6 \times 6 \mu\text{m}^2$ LP, 125-nm-thick BCB liner, and 50-nm-thick Ti barrier.

We first observe that von Mises stress magnitude decreases with increasing pitch and starts to saturate at around $15 \mu\text{m}$ pitch shown in Fig. 14. This is understandable since the stress magnitude induced by a single TSV becomes negligible at the similar pitch. Also, the layout using TSVs with LP and BCB liner shows a similar trend with lower von Mises stress magnitude than the case without these structures.

C. Impact of TSV Size

To investigate the effect of the TSV size, we use three different sizes of TSV with a same aspect ratio of 6: TSV small ($H/D = 15/2.5 \mu\text{m}$ and $\text{KOZ} = 1.22 \mu\text{m}$), TSV medium ($H/D = 30/5 \mu\text{m}$ and $\text{KOZ} = 1.202 \mu\text{m}$), and TSV large ($H/D = 60/10 \mu\text{m}$ and $\text{KOZ} = 1.175 \mu\text{m}$), where H/D is TSV height/diameter. Note that these TSV cells are occupying two, three, and five standard cell rows, respectively, which are selected to minimize the KOZ size difference between them. By setting similar KOZ size, we can focus on the impact of TSV size solely. Additionally, we set the LP width that is $1 \mu\text{m}$ larger than the corresponding TSV diameter and use 125-nm-

Fig. 15. Impact of liner thickness on the maximum von Mises stress of circuits with TSV_A cell.

thick SiO₂ liner and 50-nm-thick Ti barrier for all cases for fair comparisons.

Table VIII shows the maximum von Mises stress. Both irregular and regular TSV placement schemes benefit from smaller TSV diameter significantly. This is mainly because the magnitude of normal stress components decay proportional to $(D/2r)^2$, where r is the distance from the TSV center.

D. Impact of LP Size

We now explore the impact of LP size, which is normally determined by considering TSV alignment, on reliability issues. Designs with TSV_B cells with 125-nm-thick SiO₂ liner and 50-nm-thick Ti barrier are used. We compare the maximum von Mises stress and the number of violating TSVs with two different LP size shown in Table IX.

These results show that the regular TSV placement benefits more von Mises stress reduction from the larger LP size. This is because the stress reduction in a single TSV directly translates to the overall stress magnitude decrease in a full-chip scale for the regular TSV placement case. However, increasing the LP size does not improve von Mises stress significantly. Also we see that all TSVs do not satisfy von Mises criterion for every test case. This is because only the magnitude of σ_{rr} stress component at the wafer surface is reduced due to Cu LP, while other stress components hardly changes with a larger LP size.

E. Impact of Liner Thickness

In this section, we examine the impact of liner thickness on von Mises stress. We use designs with both TSV_A cells and TSV_B cells and set the LP size $6 \times 6 \mu\text{m}^2$ and $8 \times 8 \mu\text{m}^2$, respectively. We also use 50-nm-thick Ti barrier for all cases. Fig. 15 shows the maximum von Mises stress results with liner thickness of 125 nm, 250 nm, and 500 nm.

We observe that liner thickness has a huge impact on the von Mises stress magnitude, since the thicker liner effectively absorbs thermomechanical stress at the TSV–liner interface. Especially, the BCB liner shows significant reduction in the maximum von Mises stress compared with SiO₂ liner due to extremely low Young's modulus shown in Table I. For example, 500-nm-thick BCB liner reduces the maximum von Mises stress by 29% for the Irreg_A and satisfies the von Mises yield criterion for all circuits with a regular TSV placement.

TABLE X

IMPACT OF LINER THICKNESS ON THE NUMBER OF TSVs VIOLATING VON MISES CRITERION

Circuit	Liner Material	# Violating TSVs		
		125 nm	250 nm	500 nm
Irreg _A	SiO ₂	1462	1426 (2% ↓)	1281 (12% ↓)
	BCB	1389	1147 (17% ↓)	329 (76% ↓)
Reg _A	SiO ₂	1472	0 (100% ↓)	0 (100% ↓)
	BCB	0	0 (-)	0 (-)
Irreg _B	SiO ₂	1472	1236 (16% ↓)	64 (96% ↓)
	BCB	974	502 (48% ↓)	0 (100% ↓)
Reg _B	SiO ₂	1472	0 (100% ↓)	0 (100% ↓)
	BCB	0	0 (-)	0 (-)

Numbers in parentheses are % reduction compared to the 125-nm-thick liner case.

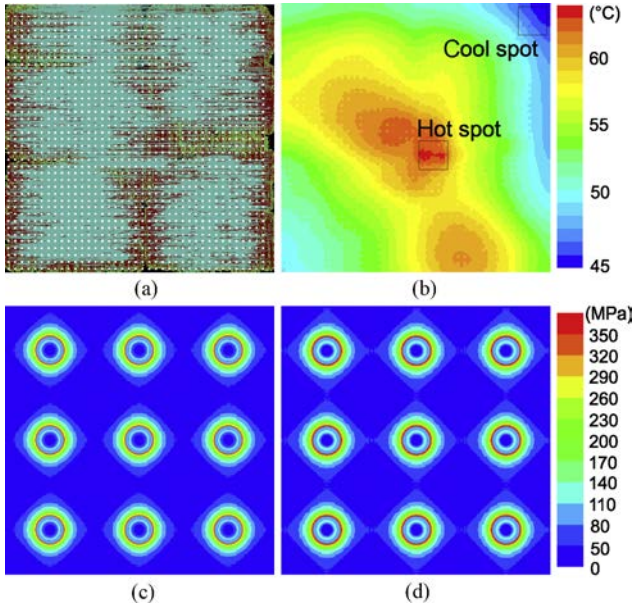


Fig. 16. Impact of temperature ($^{\circ}\text{C}$) during a chip operation on von Mises stress. (a) Layout of Reg_A. TSV LPs are white rectangles. (b) Thermal map. (c) von Mises stress map in the hot spot. (d) von Mises stress map in the cool spot.

Table X shows the number of TSVs violating von Mises criterion. Even though there are still many TSVs not satisfying von Mises criterion for the Irreg_A circuit, it is possible to reduce von Mises stress if we place TSVs carefully considering this reliability metric during a placement stage.

F. Impact of Chip Operation Temperature

Up to this point, we only consider the residual stress caused by the manufacturing process. Now, we examine the reliability problem during the chip operation phase. Our full-chip thermal simulation flow is as follows. We first generate a power map using SoC Encounter and then feed this to ANSYS Fluent with in-house add-ons that enable a steady-state thermal analysis for GDSII-level 3-D ICs shown in Fig. 16(b).

Depending on the temperature distribution across the die area, each TSV experiences a different thermal load. Thus, the significance of mechanical reliability problem of an individual TSV might be different from each other. To support

TABLE XI

COMPARISON BETWEEN GATE-LEVEL AND BLOCK-LEVEL DESIGN

Design Level	TSV Pitch (μm)	# TSV	Wirelength (mm)	Area ($\mu\text{m} \times \mu\text{m}$)	Max Stress (MPa)
Gate	Irregular 23.5	1472	9060	960×960	729.3
		1472	9547	960×960	386.4
Block	15	368	8259	950×1130	414.5
	10	394	8028	1080×1000	519.9
	7.5	333	7933	980×1090	716.2

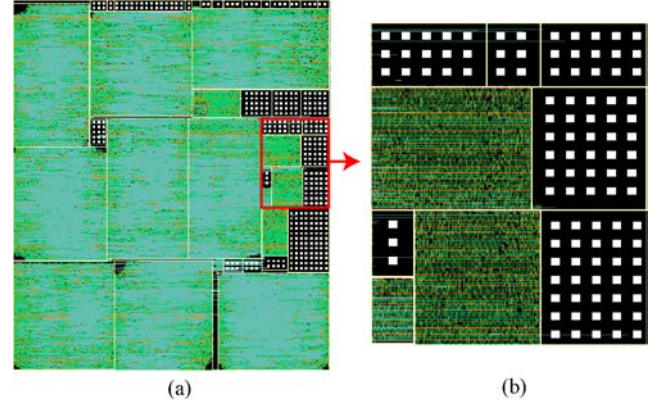


Fig. 17. Layout of block-level design (TSV pitch = $15 \mu\text{m}$). White rectangles are TSV LPs. (a) Full-chip layout. (b) Closeup shot of the red box in (a).

temperature-dependent stress analysis, we build stress library with wide range of thermal load.

We use the Reg_A circuit for this experiment since TSVs in the regular TSV placement scheme shows uniform von Mises stress distribution, which enables us to observe the impact of an operating temperature across the die easily. We use 500-nm-thick BCB liner for this experiment.

We observe that the cool spot experiences higher von Mises stress, since the temperature difference from the stress-free temperature, 275°C in our case, is larger in the cool spot than in the hot spot. However, since the maximum temperature difference across the die is only 20°C , the impact of an operating temperature on the TSV reliability across the die is not significant. In our test case, the difference of the maximum von Mises stress between two spots is 30.4 MPa . Also, both the hot and the cool spot experience less maximum von Mises stress compared to the residual stress case, again due to the reduced thermal load.

However, the reduction of von Mises stress during a chip operation cannot recover the material yielding failure if it already exists, since this is a nonreversible failure mechanism.

G. Reliability of Block-Level 3-D Design

Even though the gate-level 3-D design has the potential of highest optimization, the block-level design is attractive in the sense that we can reuse already highly optimized 2-D intellectual property blocks. In this section, we study the reliability issues in block-level 3-D designs. Three-dimensional block-level designs are generated using an in-house 3-D floorplanner that treats a group of TSVs as a block shown in Fig. 17. We use a 500-nm-thick BCB liner for this experiment.

TABLE XII
IMPACT OF TSV RE-PLACEMENT ON VON MISES STRESS DISTRIBUTION,
WIRELENGTH, AND LONGEST PATH DELAY

	von Mises Stress (MPa)				WL (mm)	LPD (ns)
	480–540	540–600	600–660	660–		
Original	0.100%	0.041%	0.011%	0.002%	9060	3.607
Re-placement	0.092%	0.036%	0.009%	0.0%	9081	3.636

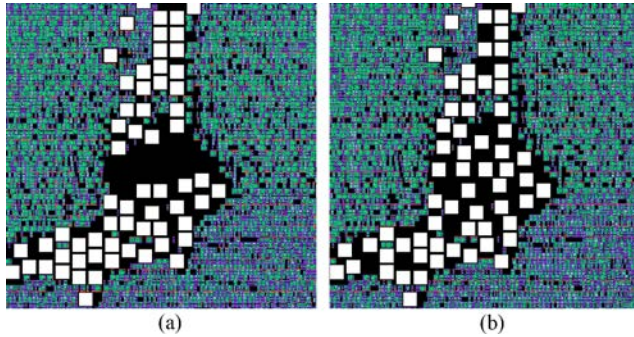


Fig. 18. TSV re-placement to reduce von Mises stress. TSV LPs are white rectangles. (a) Original layout. (b) After TSV re-placement.

We vary the TSV pitch inside TSV blocks to examine its impact on layout quality as well as reliability issues. Table XI shows that block-level designs use less number of TSVs, show shorter wirelength, and occupy more area than gate-level designs. Experimental results show that we can control the von Mises stress with area overhead in block-level design, since the TSV pitch in block-level design is controllable. Another benefit of block-level design is that we can localize the thermomechanical reliability problems only to nearby TSV blocks.

H. Impact of TSV Re-Placement

In this section, we manually optimize TSV locations to show the potential benefit of TSV reliability-aware layout optimization while minimizing the change in layout. We use the Irreg_A circuit that shows worst von Mises stress and employ 500-nm-thick BCB liner for this experiment. Our related study with this BCB liner on the maximum von Mises stress versus TSV-to-TSV pitch shows that 10 μm pitch is a reasonable choice to reduce von Mises stress considering some safety margin. We reposition densely placed TSVs to nearby white spaces if available to reduce the von Mises stress shown in Fig. 18.

Table XII shows the distribution of von Mises stress higher than 480 MPa across the die, wirelength, and longest path delay before and after the TSV re-placement. We perform 3-D static timing analysis to analyze timing using Synopsys PrimeTime with TSV parasitic information included. We see the reduction in high von Mises stress region after TSV re-placement. With small perturbations of TSV locations, we could reduce the von Mises stress level and decrease the number of violating TSVs from 329 to 261, which is 21% improvement with only 0.23% wirelength and 0.81% longest path delay increase, respectively. This small test case shows

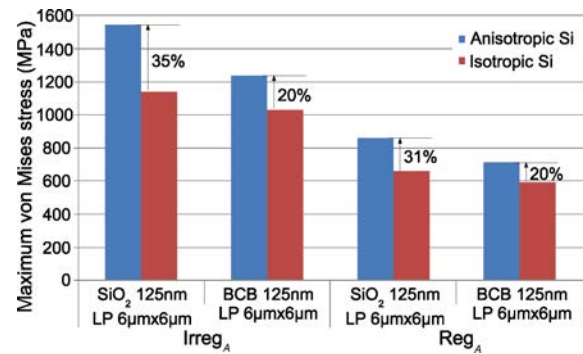


Fig. 19. Maximum von Mises stress comparison between isotropic and anisotropic Si.

the possibility of a layout optimization without degrading performance too much.

I. Comparison Between Isotropic and Anisotropic Si

In this section, we compare von Mises stress between isotropic and anisotropic Si material property in full-chip scale. We use 125-nm-thick liner, 50-nm-thick Ti Barrier, and $6 \times 6 \mu\text{m}^2$ LP. Fig. 19 shows the increased mechanical reliability problems considering the anisotropic Si elastic property; maximum von Mises stress increases more than 30% and around 20% with SiO₂ liner and BCB liner, respectively.

Young's modulus for x and y -direction of anisotropic Si is 30% higher than that of isotropic Si, and this translates to the stress magnitude increase. BCB liner, again, shows better stress absorption capability even with the anisotropic Si property. However, this clearly shows the importance of using proper material properties to assess the mechanical reliability problems in TSV-based 3-D ICs during design stages.

V. CONCLUSION

In this paper, we showed how TSV surrounding structures such as LP and dielectric liner affect stress fields and mechanical reliability in 3-D ICs. We also presented an accurate and fast full-chip stress and mechanical reliability analysis flow based on linear superposition principle of stress tensors. This approach can be applicable to mechanical reliability-aware placement optimization for 3-D ICs.

Our results showed that TSV pitch and size, liner material and its thickness, and TSV placement are key design parameters to reduce the mechanical reliability problems in TSV-based 3-D ICs.

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