TSV Density-driven Global Placement for 3D Stacked ICs

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***Abstract*— Via-first through-silicon vias (TSVs) are manufactured through bulk silicon and connected to landing pads in metal layers. Landing pads are made large enough to cover the top surface of TSVs entirely so that TSV-to-landing pad connections become invulnerable to uncertainties such as misalignment between TSVs and landing pads. Large landing pads, however, could lead to metal density mismatch problems, which result in nonuniform topography.**

In this paper, we investigate the metal density mismatch problem in 3D ICs and propose a TSV density-driven 3D global placement algorithm to minimize topography variation in 3D IC layouts. The experimental results show that we achieve $1.86\times$ improvement in the range of metal 1 densities and $2.10\times$ improvement in the maximum metal 1 density gradient with just 2.3% wirelength overhead. We also present additional studies such as the impact of landing pad size on metal density.

I. Introduction

Topography variation in metal layers is becoming more serious as technology advances beyond $65nm$ and $45nm$, and as a result, semiconductor manufacturers require strict and tight metal density rules. In addition, it is also required to minimize the range of metal density[1] and the maximum metal density gradient[2] because topography is determined mainly by underlying feature density [1], [2]. Moreover, topography is cumulative, so the smaller the topography variation in lower metal layers is, the smaller the topography variations of upper metal layers are [3].

Meanwhile, three-dimensional integrated circuits (3D ICs) are emerging to resolve the interconnect bottleneck and improve performance of 2D ICs further. In 3D ICs, cells are placed in multiple dies, the dies are stacked vertically, and through-silicon vias (TSVs) are used to connect metal layers vertically as shown in Fig. 1. Since footprint area of 3D ICs becomes smaller than that of 2D ICs, the total wirelength becomes shorter than 2D ICs, so it is expected that the performance of 3D ICs is better than 2D ICs [4]. Via-first TSVs, however, are attached to landing pads in the bottommost and the topmost metal layers as shown in Fig. 1. These metal landing pads are usually very large (see Fig. 2), so they could result in significant metal density mismatch.

In this paper, we investigate the density of the metal 1 layer in 3D IC layouts and extend a 3D global placement algorithm to improve it. The extended algorithm improves the range of metal 1 density as well as the maximum metal 1 density gradient significantly compared to traditional wirelength-driven placement. In addition, we also investigate the impact of the landing size on metal 1 density metrics.

II. Motivation

In this section, we show the motivation of our work and briefly explain 3D IC design schemes.

[1]The range of metal density is defined as the difference between the maximum density and the minimum density.

[2]Metal density gradient is defined as the density difference between two adjacent density windows.

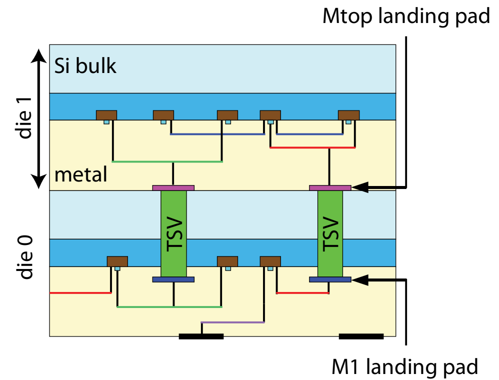

Fig. 1. A 3D IC designed in two dies using via-first TSVs and face-to-back die bonding.

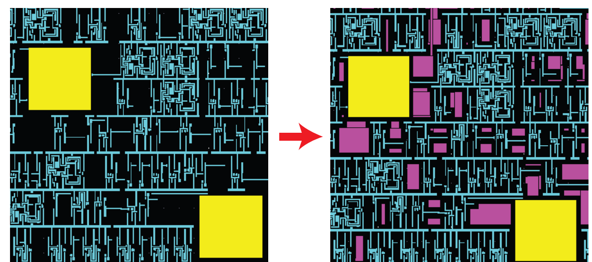

Fig. 2. Before (left) and after (right) filler insertion. Yellow squares denote TSVs, pink squares are fillers, and light blue squares are metal 1 wires.

A. Feature Density of 3D IC Layouts

To investigate the effect of landing pads on the density variation of the metal 1 layer, we conduct a preliminary experiment on a 2D layout whose area is $1.3mm \times 1.3mm$. In this experiment, we insert landing pads only in one window area ((0,0) to ($100\mu m$,$100\mu m$)), which we call the TSV window, and compare metal 1 density before and after fill insertion. Fig. 3 shows the result. When the number of landing pads is less than 30 to 50 in the TSV window, the maximum density window is different from the TSV window, so the density range over the entire layout can be controlled by traditional fill insertion. However, if the number of landing pads in the TSV window is greater than approximately 60, the maximum metal 1 density occurs in the TSV window and the density range increases monotonically as the number of landing pads increases. Therefore, it is necessary to keep the number of landing pads in one window small or spread landing pads out.

B. The Design of 3D ICs

The authors of [5] propose two 3D IC design schemes, namely TSV co-placement and TSV-site. In the TSV co-placement scheme, they place TSVs and cells simultaneously to find optimal locations of

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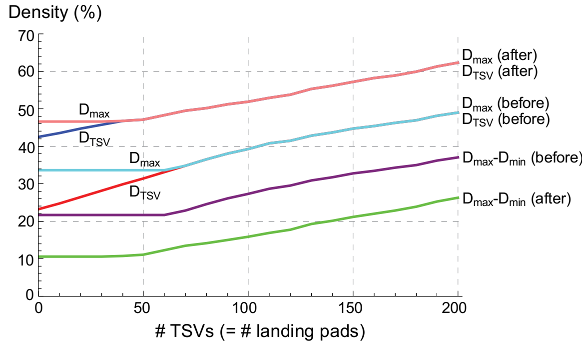

Fig. 3. Variation of the maximum density and the density range in the metal 1 layer when only one window contains landing pads ($4.14\mu m \times 4.14\mu m$). “before” (or “after”) denotes before (or after) fill insertion, $D_{\max}$ (or $D_{\min}$) denotes the maximum (or minimum) density, and D_{TSV} denotes the density of the window containing landing pads.

TSVs and cells. In the TSV-site scheme, on the other hand, they place TSVs uniformly on the entire layout area and then place cells. In this case, they need to assign 3D nets to TSVs to determine which 3D net uses which TSV. Since the solution set of the TSV co-placement scheme contains that of the TSV-site scheme, wirelength of the TSV co-placement scheme is in general shorter than that of the TSV-site scheme. However, it is expected that the TSV-site scheme will have better metal 1 density.

III. TSV Density-Driven 3D Global Placement

The 3D placement algorithm used in this work is based on the force-directed quadratic placement algorithm for 3D ICs [5], [6]. In this section, therefore, we review the force-directed quadratic 3D placement algorithm and explain how we extend it for the TSV density-driven 3D placement.

A. Force-Directed Quadratic 3D Global Placement

The basic principle of the force-directed quadratic *2D* global placement is to apply several forces to cells and move cells gradually until the cell occupancy of each global bin becomes less than a pre-determined number. When we apply forces, we try to minimize objective functions such as quadratic wirelength Γ.

The authors of [6] suggest three forces for the force-directed placement. The first force is *net force*, which pulls connected cells to minimize the wirelength of the net connecting the cells. The second force is *move force*, which spreads cells out to remove cell overlaps. The third force is *hold force*, which holds cells in low cell density regions at the current locations. The sum of these forces is set to zero to minimize the total wirelength while removing cell overlaps. This is mathematically expressed as follows:

$$\mathbf{f} = \mathbf{f}^{\text{net}} + \mathbf{f}^{\text{move}} + \mathbf{f}^{\text{hold}} = \mathbf{0}\ , \quad (1)$$

where $\mathbf{f}^{\text{net}}$, $\mathbf{f}^{\text{move}}$, and $\mathbf{f}^{\text{hold}}$ are net force, move force, and hold force, respectively.

The authors of [5] extend this algorithm to place cells in 3D. They first use multi-way partitioning to split cells into multiple partitions (multiple dies in 3D ICs). After partitioning, they place cells and TSVs with the same objective function as 2D placement. However, they compute all the forces in each die separately because cells in different dies do not overlap.

TABLE I

Benchmark Circuits. The number of TSVs is based on two-die implementation.

ckt	# gates	# nets	# TSVs	# TSVs / # nets
C1	29,706	29,979	1,035	0.0345
C2	77,234	77,378	675	0.0087
C3	88,401	89,149	1,045	0.0117
C4	103,711	103,946	424	0.0041
C5	109,181	109,415	1745	0.0159
C6	168,943	169,469	114	0.0007
C7	324,490	327,843	1559	0.0048
C8	444,555	483,563	3838	0.0079

TABLE II

Multi-pass metal 1 fill insertion parameters.

Parameter	Value
Max. metal density	75%
Max. length (or width) of a metal fill	$3.25\mu m$
Min. metal density	25%
Min. length (or width) of a metal fill	$0.065\mu m$
Preferred metal density	35%
Window size (width)	$100\mu m$
Window step size	$50\mu m$

B. TSV Density-Driven 3D Global Placement

Since closely-placed TSVs can cause serious density mismatch in the metal 1 layer, we apply another density force focusing on TSVs only, namely TSV density force. This force is similar as the move force that is computed by cell density. TSV density force is computed as follows. First, placement density considering only TSV density in each global placement bin is computed as follows:

$$D(b)\Big|_{z=d} = D^{\text{TSV}}(b)\Big|_{z=d} - D^{\text{chip}}(b)\Big|_{z=d}\ , \quad (2)$$

where $D^{\text{TSV}}(b)\big|_{z=d}$ is the TSV density in bin b of the d-th die and $D^{\text{chip}}(b)\big|_{z=d}$ is the total capacity of bin b of the d-th die. Then, we compute the placement potential Φ^{TSV} by Poisson equation:

$$\Delta\Phi^{\text{TSV}}(b)\Big|_{z=d} = -D(b)\Big|_{z=d} \quad (3)$$

The x-location of the i-th TSV in the next iteration is computed by the following equation:

$$x_i = x_i' - \frac{\partial}{\partial x}\Phi^{\text{TSV}}(b)\Big|_{(b'),z=d}\ , \quad (4)$$

where x_i is the target x-location, x_i' is the current x-location, and b' is the current bin in which the i-th TSV exists. y-location of the i-th TSV is computed in the similar way.

If we compute the TSV density force as above, the final force equation becomes as follows:

$$\mathbf{f} = \mathbf{f}^{\text{net}} + \mathbf{f}^{\text{move}} + \mathbf{f}^{\text{hold}} + \mathbf{f}^{\text{TSV}} = \mathbf{0}\ , \quad (5)$$

where $\mathbf{f}^{\text{TSV}}$ is the TSV density force.

For better understanding, we show three layouts of a circuit designed by the wirelength-driven TSV co-placement, the TSV density-driven co-placement, and the TSV-site placement in Fig. 4. The left figure shows the wirelength-driven placement and we observe that TSVs are placed non-uniformly. On the other hand, the middle figure shows the TSV density-driven placement and we find that TSVs are sparsely placed compared to the wirelength-driven placement. The right figure shows uniformly-placed TSVs in the TSV-site placement.

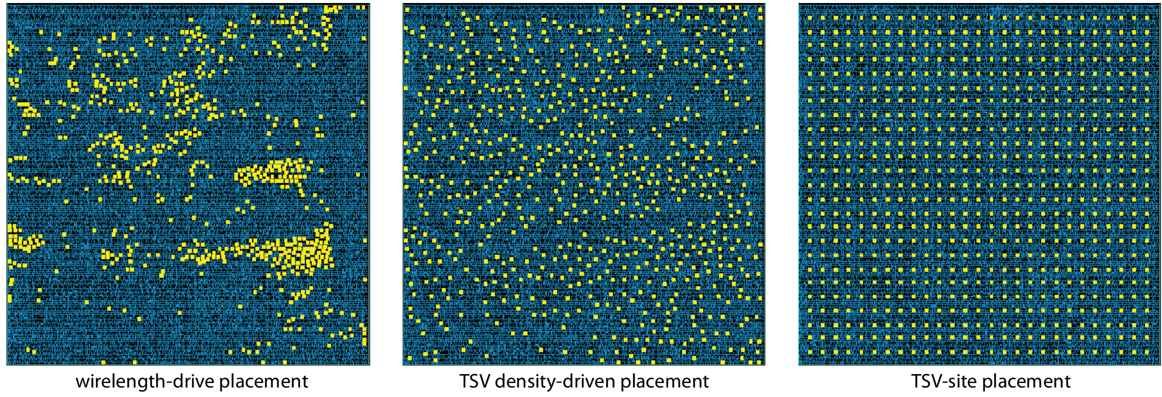

Fig. 4. Screen shots circuit C2. Dark rectangles are standard cells and light squares are metal 1 landing pads.

TABLE III

COMPARISON OF MINIMUM AND MAXIMUM METAL 1 LAYER DENSITIES IN **TWO-DIE** IMPLEMENTATION WITH $1\times$ TSV. "BEFORE (OR AFTER)" DENOTES BEFORE (OR AFTER) FILL INSERTION. DUE TO SPACE LIMIT, WE SHOW THE GEOMETRIC MEAN OF THE EIGHT BENCHMARK CIRCUIT RESULTS.

Die	Minimum density						Maximum density					
	WL-driven		TSV-site		TSV density-driven		WL-driven		TSV-site		TSV density-driven	
	before	after	before	after	before	after	before	after	before	after	before	after
die0	24.869%	35.165%	25.858%	37.884%	26.452%	33.445%	36.823%	44.700%	29.274%	42.891%	29.649%	42.238%
die1	20.167%	37.016%	19.761%	36.470%	20.061%	36.819%	36.470%	40.906%	21.904%	40.921%	22.104%	40.752%

TABLE IV

COMPARISON OF WIRELENGTH AND METAL 1 LAYER DENSITIES IN **TWO-DIE** IMPLEMENTATION WITH $1\times$ TSV. D DENOTES METAL 1 DENSITY OF A WINDOW. (NUMBERS IN PARENTHESES ARE WIRELENGTH RATIOS.)

Wirelength (mm)			Die	Range ($\Delta D = D_{\max} - D_{\min}$)			Maximum density gradient		
WL-driven	TSV-site	TSV density-driven		WL-driven	TSV-site	TSV density-driven	WL-driven	TSV-site	TSV density-driven
3.326	3.529	3.403	die0	9.197%	4.574%	4.982%	5.258%	2.400%	2.506%
(1.000)	(1.061)	(1.023)	die1	3.587%	4.102%	3.497%	2.064%	2.405%	1.832%

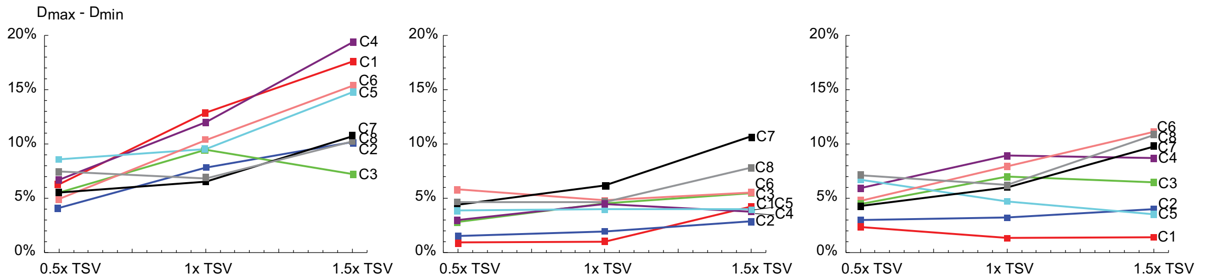

Fig. 5. ΔD of die0 of WL-driven placement (left), TSV-site placement (middle), and TSV density-driven placement (right)

IV. EXPERIMENTAL RESULTS

We use eight benchmark circuits obtained from IWLS 2005 benchmark suite [7] and OpenCores [8] in our experiments. These circuits are listed in Table I. We also use NCSU $45nm$ technology library [9]. The baseline TSV landing pad size ($1\times$ TSV) is $4.14\mu m \times 4.14\mu m$, and Table II shows some of our fill insertion parameters.

A. Comparison of the Metal 1 Layer Density

We first compare the minimum and the maximum metal 1 densities before and after fill insertion to show that the fill insertion tool satisfies the lower and the upper metal density limits and achieves the preferred density. Table III shows the geometric mean of the densities of the eight benchmark circuits. As the "after" columns show, the fill insertion tool satisfies the metal density limits for both die0 in which TSVs exist and die1 in which TSVs do not exist. Moreover, final metal densities are close to the preferred metal density. From this table, we observe that we can satisfy the lower and the upper metal 1 density limits after fill insertion even when large landing pads exist.

Next, we compare metal 1 densities of all the benchmark circuits designed in two dies with $1\times$ TSV. In this two-die implementation, *die0* contains TSVs as well as cells as shown in Fig. 1, but *die1* contains only cells. Table IV shows the results. Comparing the density range (ΔD), we observe that the WL-driven placement has the worst density range compared to the TSV density-driven placement or the TSV-site placement in die0. The geometric mean of ΔD of the WL-driven placement is about 9.197% whereas that of the TSV density-driven placement is 4.982% and that of the TSV-site placement 4.574%. Similarly, the maximum gradient, which is the maximum difference between densities of two adjacent windows, of the WL-driven placement is worse than the TSV density-driven or the TSV-

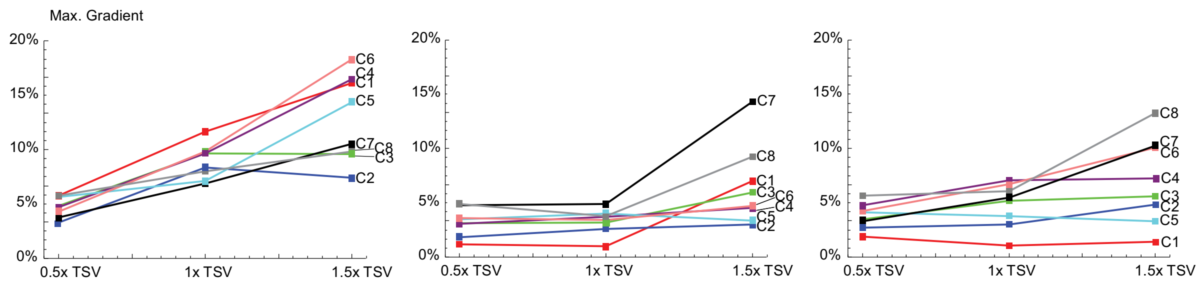

Fig. 6. Maximum density gradient of die0 of WL-driven placement (left), TSV-site placement (middle), and TSV density-driven placement (right)

site placement. The eometric mean of the maximum density gradient of the WL-driven placement is 5.258%, but that of the TSV density-driven placement is 2.506% and that of the TSV-site placement is 2.400% in die0. Therefore, we find that uniformly-placed or sparsely-placed TSVs improve metal 1 densities significantly. However, the metal 1 density in die1 shows different trends because die1 does not contain landing pads. As the table shows, the geometric mean of density range or the maximum density gradient of the WL-driven placement is similar to that of the TSV density-driven or the TSV-site placement.

B. Wirelength Comparison

In the WL-driven placement, we have the three basic forces – net force, hold force, and move force. However, we add one more force in the TSV density-driven placement and we pre-place TSVs uniformly in the TSV-site placement, so the wirelength of the TSV density-driven or the TSV-site placement is expected to be longer than that of the WL-driven placement. Table IV shows the wirelength comparison. The average wirelength of the WL-driven placement is $3.326mm$ while that of the TSV density-driven placement is $3.403mm$, which is 2.3% longer than the WL-driven placement. On the other hand, the average wirelength of the TSV-site placement is $3.529mm$, which is 6.1% longer than that of the WL-driven placement. Therefore, we observe that the TSV density-driven placement improves metal 1 density significantly (approximately $2\times$ better than the WL-driven placement with respect to both ΔD and the maximum gradient) with just 2.3% wirelength overhead. Moreover, wirelength overhead of the TSV density-driven placement remains between 1.2% and 3.7%, but the improvement in the metal density is $2\times$ to $9\times$. On the other hand, wirelength overhead of the TSV-site placement is between 1.0% and 13.4%, which is much worse than that of the TSV density-driven placement. As a result, we conclude that the TSV density-driven placement is comparable to the TSV-site placement with respect to the metal 1 density and comparable to the WL-driven placement with respect to the wirelength.

C. Impact of Landing Pad Size

Since the landing pad size affects the metal 1 density significantly, we also show the impact of landing pad size on the density metrics. Fig. 5 shows ΔD for all the circuits when the landing pad size is $0.5\times$ ($2.07 \times 2.07\mu m^2$), $1\times$ ($4.14 \times 4.14\mu m^2$), and $1.5\times$ ($6.21 \times 6.21\mu m^2$). In general, ΔD increases as the landing pad size goes up in the case of the WL-driven placement. However, ΔD decreases in some cases as the landing pad size increases as shown in the TSV density-driven or the TSV-site placement cases. Therefore, larger TSV landing pad size does not always lead to worse ΔD. This is mainly because fill insertion can increase the minimum density to decrease ΔD if TSVs are spread out sufficiently. Similarly, the maximum density gradient does not always increase as the landing pad size goes up as shown in Fig. 6.

V. Conclusions

In this paper, we investigate the density of the metal 1 layer in 3D IC layouts and propose a TSV density-driven 3D global placement algorithm to improve the metal 1 layer density in 3D IC layouts. In the algorithm, we add a new force acting only on TSVs so that we can spread TSVs without too much wirelength overhead. By applying the TSV density-driven 3D global placement algorithm, we achieve $1.86\times$ improvement in the range of the metal 1 density and $2.10\times$ improvement in the maximum metal 1 density gradient compared to the wirelength-driven placement. Wirelength overhead of our algorithm is 2.3%, which is almost negligible. On the other hand, wirelength overhead of the TSV-site placement is much larger than the TSV density-driven placement. Therefore, the TSV density-driven placement achieves short wirelength comparable to the wirelength-driven placement and small metal 1 density variation comparable to the TSV-site placement.

We also present the impact of landing pad size on the metal 1 density. As we observe in Section IV, the metal 1 density range and the maximum density gradient of the wirelength-driven placement become worse as the landing pad size increases. Those of the TSV density-driven placement also increase as the landing pad size increases, but this trend is observed only when there are few TSVs in the layouts. In summary, the TSV density-driven placement has better metal 1 density characteristics than the wirelength-driven placement with very small wirelength overhead.

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