Pre-Bond and Post-Bond Test and Signal Recovery Structure to Characterize and Repair TSV Defect Induced Signal Degradation in 3-D System

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***Abstract*— In this paper, we present a methodology for characterization and repair of signal degradation in through-silicon-vias (TSVs) in 3-D integrated circuits (ICs). The proposed structure can detect the signal degradation through TSVs due to resistive shorts in liner oxide and variations in resistance of TSV due to weak open and/or bonding resistance. For TSVs with moderate signal degradations, the proposed structure reconfigures itself as signal recovery circuit to maintain signal fidelity. This allows electrical repair of TSVs with moderate defects leading to better design yield and system functionality. This paper presents the design of the test and recovery structure and demonstrates their effectiveness through stand alone simulations as well as in a full-chip physical design of a 3-D IC.**

***Index Terms*— 3-D integrated circuit, signal integrity, test, through-silicon-via.**

I. Introduction

THE functionality of a 3-D integrated circuit (IC) strongly depends on the fidelity of signals through through-silicon-vias (TSVs) [1]–[2]. As the TSV process is not a perfect one, defects can be created while forming the TSVs before bonding (assuming a via-first process) or while bonding different dies together [3]–[12]. The defect can be created by short through the oxide surrounding the TSVs resulting in finite resistance between TSV and substrate. The open defects or ruptures can also be created during TSV growth [3]–[12]. The non-conformal growth of the insulator also creates defects or variation in TSV properties [3]–[12]. At the post-bond stage, the defects can be created due to variation in the resistance of the bonding material or misalignment. A short through the oxide creates a resistive path through the oxide to the surrounding substrate and hence ground (assuming the substrate is grounded, Fig. 1). Likewise the open defect, variation in bonding resistance, and TSV misalignment impact the resistance through a TSV. When the TSV is driven by a driver, the signal swing and/or slew at the receiver end can vary significantly due to short/open defects resulting in either complete or partial signal degradation. The complete degradation results in no signal propagation through TSVs and is caused by strong short/open. The weak short/open results in partial degradation i.e., signal can propagate through the TSV but with degraded amplitude/slew. Since maintaining the signal fidelity through TSVs is a primary requirement for 3-D system integration, it is imperative that characterization of the electrical impact of the TSV defects/variations is critical.

Testing and characterization of the TSVs have significant challenge, particularly before bonding (pre-bond-test) [3]–[12]. The TSVs are too small for test probe and one cannot afford to include a large number of probe pads for testing. The pre-bond test structures also need to satisfy additional requirements. First, the structures should be designed to be able to characterize TSV defects after bonding. Second, the test structures should be able to function as signal recovery circuits to recover the degraded signal at the receiver end of the TSV. This will allow electrical repair of the TSVs with weak defects to maintain system level signal fidelity and help to improve design yield. Third, distinguishing between weak and strong defects requires testing for the analog properties of TSVs. It is important that test structures should be able to create digital signatures of the analog nature of the defects. The digital signatures need to be stored on-chip and later read-out for test, characterization, and recovery. Finally, the power, performance, and area overhead associated with the built-in test structures need to be analyzed considering full-chip analysis of a 3-D IC.

The pre-bond test-structures for detecting resistive shorts and opens have received limited attention in recent literatures [9]–[12]. Tsai *et al*. has discussed detection of pin-holes defects in TSVs by using circuits to measure TSV resistance [9]. Chen *et al*. has proposed to measure the RC time constant of TSVs and compare that with the known values to determine the existence of faults [10]–[11]. However, to the best of our knowledge, there is no prior work that presents on-chip circuit that can simultaneously detect weak/strong defects in TSVs during pre-bond and post-bond test and if required, performs signal recovery under non-catastrophic failures in TSVs.

In this paper, we present an integrated on-line test and signal recovery structure and associated design/test methods to

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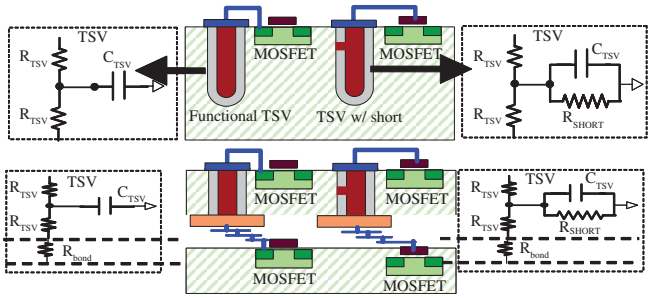


Fig. 1. Schematic illustration of TSV shorts at the pre-bond stage (top) and variation in the resistance at the post-bond stage (bottom).

simultaneously characterize TSV defects and maintain signal fidelity through TSVs. We present a low-overhead digital test structure based on scan flip-flops (FFs) that detects the resistive defects in TSVs and characterizes them as in one of the following groups: 1) bad TSVs with complete signal degradation; 2) repairable TSVs with moderate signal degradation and can be recovered with additional circuit; and 3) good TSVs with high signal quality. The test structure is designed to be able to characterize resistive shorts through oxide before bonding and resistance variation in the TSV path after bonding. The proposed test circuit reconfigures itself as a signal recovery circuit to repair TSVs with moderate pre-bond or post-bond defects and improve the fidelity of the signals passing through them. The efficiency and overhead of the proposed test structure is studied considering full-chip 3-D physical design of an example circuit.

The rest of this paper is as follows. Section II discusses the electrical effects of TSV defects, Section III presents the proposed test and signal-recovery structure, Section IV presents the simulation results, Section V presents the full-chip analysis of an example 3-D system, and Section VI concludes this paper.

II. Electrical Effects of TSV Defects

In this section we present the electrical impact of the TSV defects on the signal quality. Fig. 2(a) shows a typical scenario where a TSV with a short defect is driven by an inverter in one die and the signal is received by another inverter on the second die. Consider variation in the resistance of the short due to variation in the diameter of the short. The voltage at the receiver end can vary resulting in either complete or partial signal degradation. Based on the extent of the signal degradation, we partition the TSVs in three categories. If a low resistance short exists, V_{TSV} will be very low. We refer to this as un-repairable or *bad* TSVs. The TSVs for which V_{TSV} is very high (>90% V_{DD}) are considered to *good* or defect-free TSVs. We also define a third category of TSVs, referred to as *repairable* TSVs. The *repairable TSVs* correspond to the TSVs that have shorts with moderately high resistance such that signal degradation is within an acceptable limit (e.g., within 50% of V_{DD}). The receiver end of such TSVs makes logical transitions between '0' and '1' but with a reduced voltage swing. A lower voltage swing leads to higher noise susceptibility, short-circuit power, and delay at the receiving

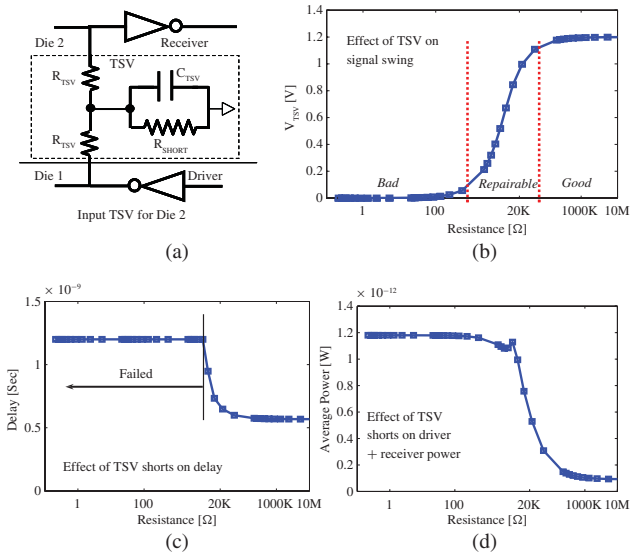


Fig. 2. Effect of TSV short (a) driver-receiver combination, (b) signal swing, (c) delay, and (d) driver & receiver power.

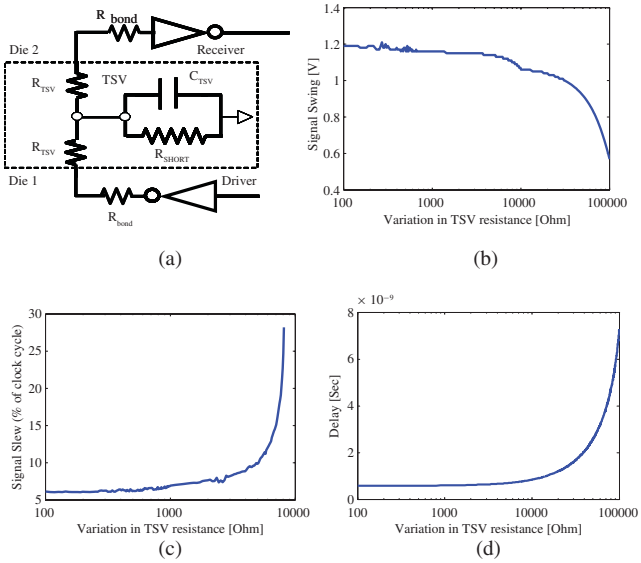
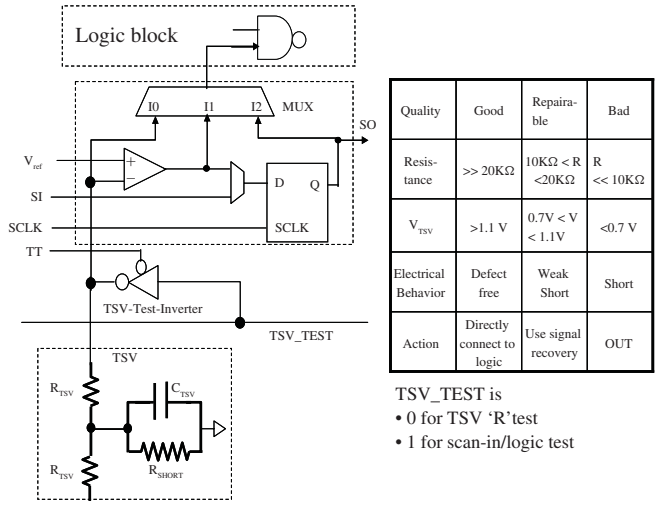


Fig. 3. Post-bond TSV resistance (a) driver-receiver, (b) effect on signal swing, (c) signal slew, and (d) signal delay.

gate as illustrated in Fig. 2. It can be observed that for very high resistance of the shorts (i.e., good TSVs), the signal swing is close to ideal [Fig. 2(b)]. As the resistance reduces the signal swing also gradually reduces [Fig. 2(b)] resulting in corresponding increase in delay through the TSV [Fig. 2(c)] and average power of the driver/receiver combination [Fig. 2(d)]. The TSVs with such intermediate resistances of the short belong to the *repairable* TSVs category. We refer to them as repairable because if the signal swing can be recovered at the receiver end, these TSVs will function correctly (although, possibly with a higher delay than the *good* ones). If the resistance is very low, the signal fails to make transition.

Fig. 3(a) shows a scenario where resistance variation can occur between TSV and receiver/driver due to weak open, misalignment, and bonding resistance. We collectively model



Quality	Good	Repairable	Bad
Resistance	>> 20KΩ	10KΩ < R <20KΩ	R << 10KΩ
V_{TSV}	>1.1 V	0.7V < V < 1.1V	<0.7 V
Electrical Behavior	Defect free	Weak Short	Short
Action	Directly connect to logic	Use signal recovery	OUT

TSV_TEST is
- 0 for TSV 'R'test
- 1 for scan-in/logic test

Fig. 4. Basic test structure and characterization policy.

the combined effect as variation in net TSV resistance. For small variation in this TSV resistance, the signal swing is close to ideal. As the variation increases, the signal swing through the TSV starts to reduce and eventually the TSV fails to function properly. Hence, variation in the TSV resistance degrades signal swing [Fig. 3(b)], impacts signal slew [Fig. 3(c)], and increases the delay of signal through TSV [Fig. 3(d)].

III. Test and Signal-Recovery Structure for TSV

In this section we discuss the proposed test and signal-recovery structure and its operating principle. The driver and the receiver across a TSV reside at two different tiers after bonding. Hence, during pre-bond test, our aim is to design a test circuit that can mimic the voltage degradation through the TSVs. But the test structure needs to perform this by using all devices in the same tier. The objective of the proposed test structure is to first place individual TSVs in one of three categories during the pre-bond test: *bad*, *repairable*, or *good*. If a *bad* TSV exists (assuming non redundant TSVs), the die is detected as a faulty one and not used during bonding thereby adding to yield degradation. However, for the repairable TSVs, the test structure reconfigures itself as a signal recovery circuit during post-bond normal operation. This reduces the overall yield degradation at the expense of marginal delay and/or power overhead. For the *good* TSVs, the test structure allows direct signal transfer from the driver to the receiver without signal recovery. After bonding, the test structure re-tests individual TSVs to capture the effect of variations in resistance of TSV. Note the test structure for repairable TSVs continues to operate in the recovery mode even after bonding. But even if a TSV is detected as defect-free during pre-bond test, if the variation in the resistance of that TSV is very high after bonding and causes signal degradation, the test structure for that TSV reconfigures itself to a signal recovery circuit.

A. Basic Structure and Operating Principle

1) Pre-Bond Test Mode for Input TSV: A TSV-test-inverter (TTI) is connected to each TSV (Fig. 4). During testing the input of the TTI is held low. This forms a resistor divider structure between the p-channel metal-oxide-semiconductor (PMOS) resistance of the TTI-inverter and the resistance of the TSV short. The resistances of the short (R_{short}) and the TTI determine the voltage at the TSV-TTI junction (V_{TSV}). Depending on the value of the R_{short}, the V_{TSV} will vary. This V_{TSV} is next compared against a reference voltage and sampled into a scan FF connected to the comparator. The reference voltage is selected such that it represents an "acceptable" signal quality (e.g., >50% of V_{DD}). The TSVs with low resistive shorts have V_{TSV} values less than the reference voltage while the defect-free TSVs have very high V_{TSV}. The output of the comparator connected to the TSV captures the extent of the short in that TSV in a digital '1/0' form. The values stored in the scan FFs are scanned out to locate the faulty TSVs at the end of the test. If such TSVs exist the die is categorized as a faulty one. The above test is performed again but with a higher reference voltage (∼90% of V_{DD}). The scan FFs which indicate faults with this high reference voltage corresponds to *repairable* TSVs.

2) Signal Recovery During Normal Operation (Input TSV): For the repairable TSVs, the test circuit reconfigures itself to connect the output of the comparator to the input of the logic gates (instead of directly using the TSVs) during normal operation. The comparator is designed such that during normal operation it functions as a level converter circuit and recovers the signal degradation. As for the input TSVs, the test circuit resides between TSV and the input logic gate.

3) Pre-Bond Testing and Signal Recovery for the Output TSV: The test structure for pre-bond testing of an output TSV is similar to that of an input TSV and uses the same test/reconfiguration circuit. The TTI is connected to the TSV and the V_{TSV} is sampled by the test circuit. The basic operating principle is also similar. The only difference is that instead of an output multiplexor (MUX), here we need to extend the input MUX to multiplex V_{TSV}, scan in (SI), and the logic output. The primary difference in this case is that the signal recovery needs to be performed in the second die [Fig. 5(a)]. This requires re-running the TSV test after bonding where the TTI drives the bonded TSV. The V_{TSV} developed at the receiver end in the second die is compared against the threshold to activate or deactivate the signal recovery.

4) Post-Bond Testing and Signal Recovery: Along with the short defects in the TSVs, the effective resistance of the TSV can also vary due to weak open, resistance of the bonding material, or misalignment during die-bonding. The proposed test structure is also used to characterize variations in the resistance of TSV and if required perform signal recovery [Fig. 5(b)]. Note if a TSV is detected as a repairable one in the pre-bond stage, it is automatically configured in the signal-recovery mode. Further, as such TSVs have moderate short, the voltage developed at the TSV end varies with a change in the resistance of the TSV. Hence, our test approach is to activate the TSVs from the driver layers and sample the TSV voltage at the receiver layer using the proposed test circuit. However, for good TSVs with very high resistive short, a variation in the resistance of TSVs is not reflected in the DC voltage change of the TSVs. This is because the TSV is connected to the gate

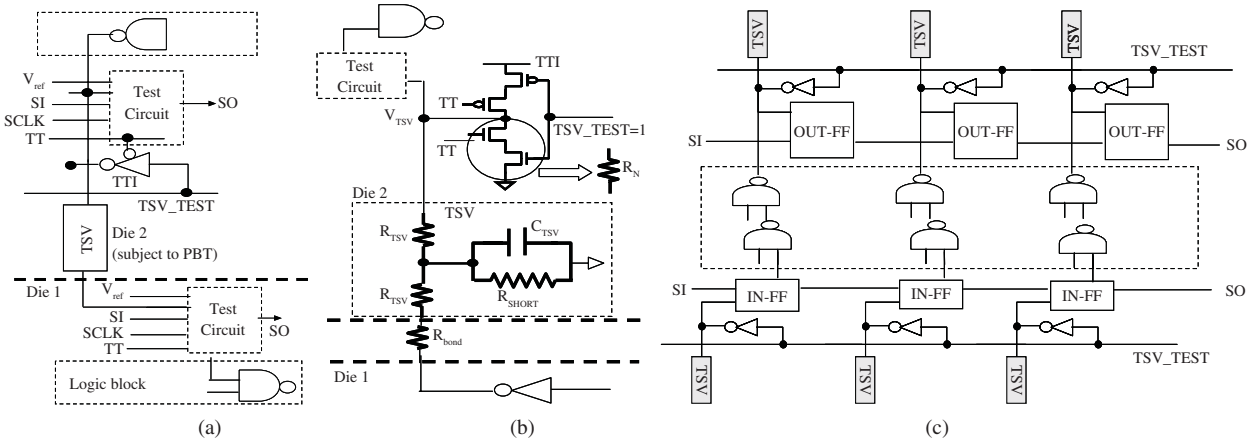


Fig. 5. Test structure for (a) pre-bond test of output TSV, (b) post-bond characterization, and (c) logic diagram of the overall test structure.

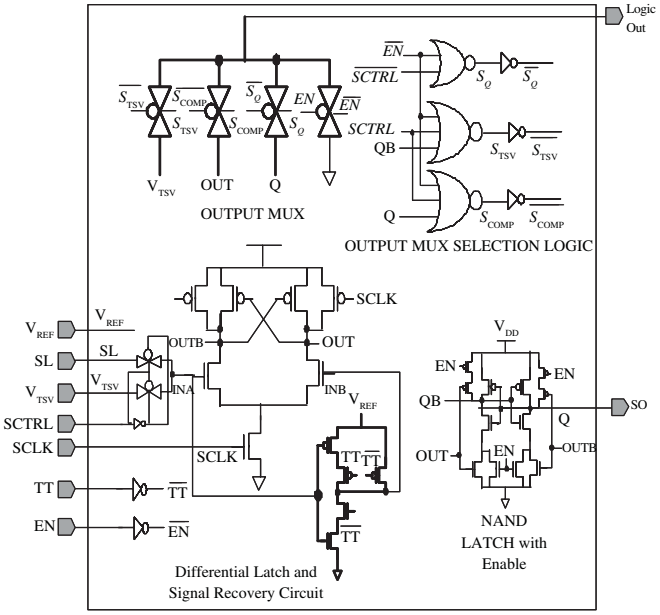


Fig. 6. Circuit schematic of the proposed test circuit.

of a device in the receiver end therefore there is no current path to ground. To enable the characterization of variation in the resistance of TSVs in such scenarios we propose to assign TSV_TEST = 1 for the TTI in the receiver tier. This activates the n-channel metal-oxide-semiconductor (NMOS) device in the TTI in the receiver end and creates a current path from the driver in die 1 to the ground. The NMOS is designed with long channel (or multiple NMOS in series) to ensure the voltage drop across the NMOS is very high if variation in the TSV resistance is very low. Otherwise V_{TSV} varies depending on the variation in the resistance. We sample the developed V_{TSV} into the test circuit to detect whether the variation in the resistance of TSVs is higher than a given limit. A high variation in resistance degrades the signal slew (for defect-free TSVs) and signal swing (for TSVs with short of moderate resistance) (see Section IV for simulation results). If for a TSV, a low V_{TSV} is developed during this test, we activate the signal recovery circuit to improve the signal swing and slew.

5) Integration with Scan Architecture for Pre-Bond Test: This paper primarily focuses on the TSV test. However, we would like to note that the scan FFs used in the TSV test can also perform as a scan chain for pre-bond logic test [Fig. 5(c)]. This enables one to perform pre-bond functional tests on the partial circuits in each die [6].

B. Detailed Design of the Test and Recovery Circuit

Fig. 6 shows the detail circuit schematic of the proposed test structure and Fig. 7 shows the control signals and the methodology for performing the test. We explain the operation considering the pre-bond test condition. Note the scan FFs used in the test structure do not function as a FF during regular operation. The heart of the proposed structure is a differential sense-amplifier-based FF. The FF is designed only with the PMOS latch [instead of a complementary metal-oxide-semiconductor (CMOS) based] to allow it to function as a level converter during regular operation. We multiplex the scan input and the TSV input. The select signal of this MUX, referred to as SCTRL in Fig. 6, controls whether the TSV input or the scan input is applied to the input of the differential latch. Since this MUX needs to transfer the TSV voltage during TSV test, we design this using a transmission gate-based MUX. The output of this MUX (referred to as IN_A in Fig. 6) forms the one input of the differential latch. The second input of the differential latch (referred to as IN_B in Fig. 6) is obtained by multiplexing the reference voltage (V_{ref}) and the inverse of IN_A. This is designed as a tri-state inverter-based MUX with V_{ref} as the supply voltage. During scan in or regular operation, the inverse of IN_A is connected to IN_B. During the TSV test, the signal TT is high which ensures IN_B is equal to V_{ref}. During scan in or signal recovery mode, TT is low which ensures the inverse of IN_A is applied to IN_B (Figs. 6 and 7).

While operating as a FF during TSV test and scan in/out mode, the enable signal (referred to as SCLK in Fig. 6) of the differential latch is the scan clock signal. However, for signal recovery, SCLK is held high so that the circuit behaves as a level converter. This can be achieved by multiplexing V_{DD} and the scan clock. The selection can be achieved using TT and SCTRL. Note the SCLK generation circuit is a global one shared by all test circuits.

Control Signal Values in Different Mode					
Mode	SCTRL	SCLK	TT	EN	Comment
TSV test	0	Scan CLK	1	0	EN = 0 ensures logic inputs does not switch during TSV test or scan in to save power. After scan in EN is raised to high to apply the logic vectors
Scan IN/Out	1	Scan CLK	0	0	
Recovery	0	V_{DD}	0	1	EN is initially '0' to load the correct states in the NAND latch, then raised to '1'to ensure (a) NAND latch stores the correct states and (b) TSV or comparator outputs correctly applied to logic

Output MUX selection Logic						
INPUT			MUX Control Signals			Comments
EN	SCTRL	Q	S_{TSV} (select TSV directly)	S_{COMP} (select recovered signal)	S_Q (select scan output)	• A TSV requires signal recovery if V_{TSV}< ~1.0V. This causes OUT = 0 and Q = 0 • If V_{TSV}> 1.0V, OUT = 1, Q = 1 and TSV can be directly connected to output. • If EN = 0, output is held at '0' to prevent unnecessary logic transitions or short-circuit power. • In the recovery mode the select signals are always available and hence, the evaluation of the select signal does come into the TSV delay path.
0	X	X	0	0	0	
1	1	X	0	0	1	
1	0	0	0	1	0	
1	0	1	1	0	0	

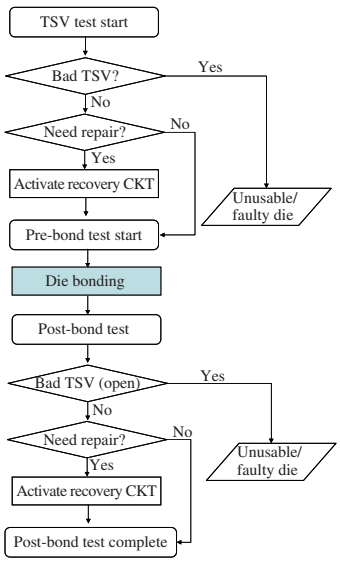


Fig. 7. Assignment of the control signals for the test circuit (left) and the overall test philosophy (right).

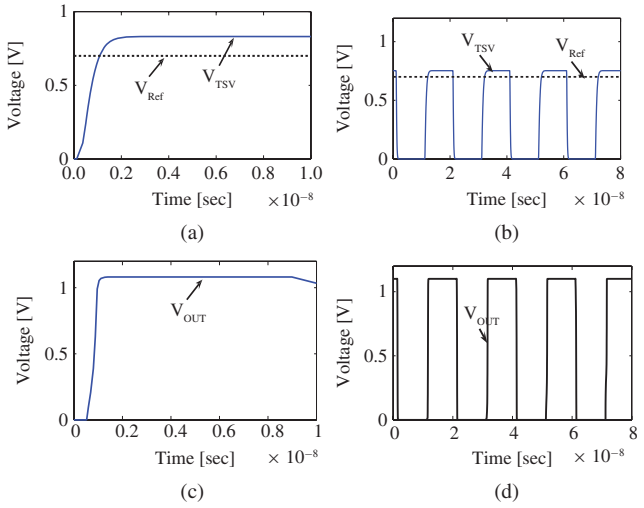


Fig. 8. Waveform of operation (a) detection input, (b) recovery input, (c) detection output, and (d) recovery output.

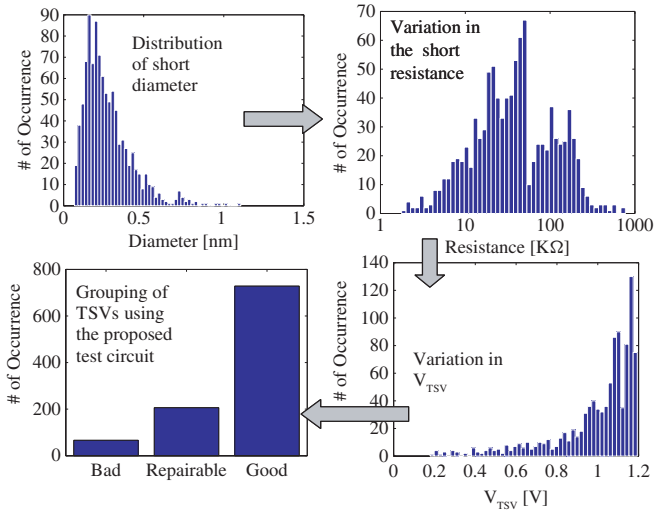


Fig. 9. Statistical simulation results showing the functionality at pre-bond test.

The output selection logic is designed to ensure that the logic input is equal to: 1) the output of the scan FF during pre-bond logic test; 2) the output of the comparator for TSVs requiring signal recovery in the operating mode; and 3) directly connected to the output of the TSVs for good TSVs in the operating mode. This can be achieved by multiplexing the three outputs. The control logic for the multiplexor is shown in Figs. 6 and 7. Note that the select signal that differentiates between scan mode and regular mode is shared by all test circuits. However, during operation one needs to differentiate between direct TSV connections and comparator connection which is a local signal. We achieve this by re-using the NAND latch connected to the sense-amplifier-based FF to store the local requirements of the TSVs (Fig. 7).

IV. Simulation Results

In this section, we present simulation results to verify the functionality of the proposed circuit.

A. Application to Pre-Bond TSV Tests and Signal Recovery

1) Verification of Functionality: Fig. 8 shows the waveform of operation of the proposed circuit demonstrating V_{TSV} detection and signal recovery. It can be observed that the proposed circuit can successfully detect the V_{TSV} value [Fig. 8(a) and (c)]. In the recovery mode, the proposed circuit can successfully recover the low voltage swing [Fig. 8(b) and (d)]. We next consider statistical simulation of variation in the diameter of the short. We consider a log-normal variation in the short diameter (Fig. 9). The resistance corresponding to different short diameters is computed considering copper TSV. As expected, the variation in the short diameter results in a variation in the resistance of TSV shorts. The resistance variation results in a variation in the voltage at the TTI-TSV connection (i.e., V_{TSV}). The proposed test structure successfully detects whether the shorts corresponds to a bad, repairable or good TSV.

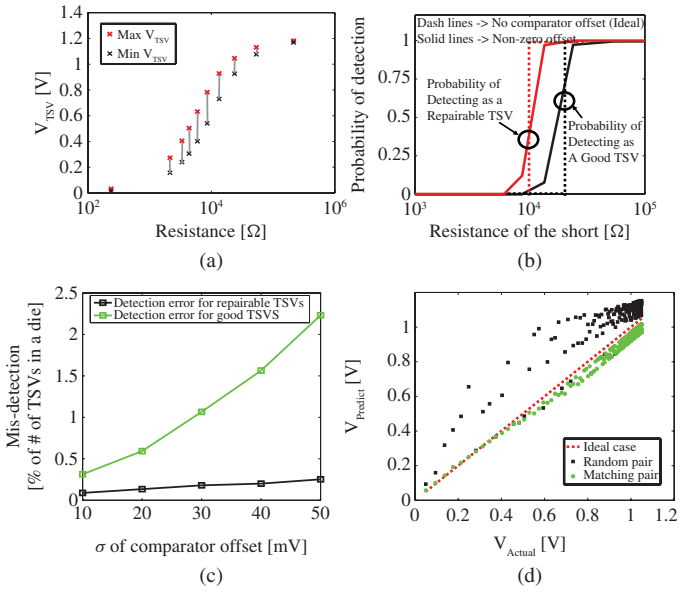


Fig. 10. Sources of detection inaccuracy obtained using Monte–Carlo simulations in 90 nm CMOS (a) VTSV variation, (b) detection error, (c) effect of offset variation, and (d) driver-TTI mismatch.

2) Factors Affecting Detection Accuracy:

a) Process variations: We first optimize the design to reduce the offset by proper device sizing. The SPICE Monte–Carlo simulation is performed considering the internal variability model for the IBM 90 nm technology [13]. The variability model simultaneously considers variations in all process parameters (such as L, W, and Vth, etc.). Due to the variation in the strength of the PMOS transistor in the TTI, the generated V_{TSV} for same short resistances can vary as shown in Fig. 10(a). This adds to the variation in the offset voltage of the differential latch due to device and output load mismatch. Considering these variations we compute the misdetection probability. We consider the random variations in the short diameters (hence, resistances) for TSVs. For each such TSV case, we perform 1000 Monte–Carlo simulations considering the random process variations and observed whether the TSV is detected as the good, repairable or bad. For each such TSV finally we compute the total probability of detecting it as good/repairable/bad and plot it against the short resistance. The detection probability should be a step function in the ideal case. However, due to finite offset there exists a misdetection probability but it is within an acceptable limit [Fig. 10(b)]. Next, we vary the standard deviation of the offset distribution and consider 1000 instances in a 3-D die with ∼1500 TSVs. For each such instance we randomly assign the TSV short diameter (and resistance) and perform the detection. The total numbers of TSVs that are incorrectly detected as repairable or good ones are computed for each die instance as a percentage of the total number of TSVs. The average of this value over the 1000 die instances is plotted in Fig. 10(c). It can be observed that the average percentage of misdetection error in detecting bad TSV as repairable or vice-versa is very low. This misdetection error is marginally higher for detecting good ones as repairable (or vice-versa).

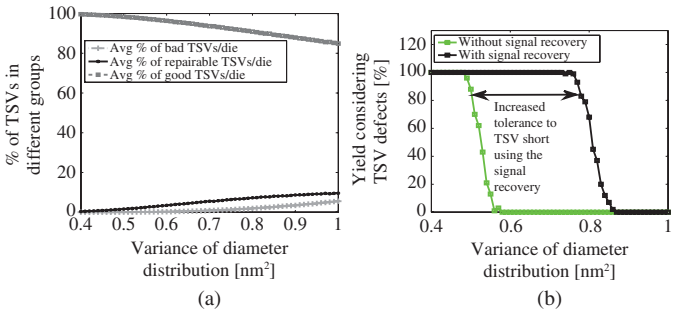


Fig. 11. (a) Detection of TSV groups and (b) effect of signal recovery on pre-bond yield.

b) Variation of the driver strength: In a real 3-D system, the drivers of each TSV are not identical. Hence, the extent of the signal degradation estimated with a fixed TTI (referred to as $V_{Predicted}$) may not exactly correlate with the actual signal degradation (referred to as V_{actual}). This is illustrated in Fig. 10(d) for different random driver sizes but fixed TTI (referred to as 'random pair'). This is obtained through multiple Monte–Carlo simulations considering random variations in short resistance and process parameters. However, the size of the drivers of each TSV is known after the design and full-chip placement/routing of the 3-D chip. We propose to use this information to match the size of the TTI for each TSV with the size of the actual driver of that TSV in the different dies (or same die for output TSVs). As expected, such a matched pair can significantly improve the correlation between the predicted and the actual signal degradation. The marginal difference can still exist because of the random process variations [as shown in Fig. 10(d)]. The above observation indicates that physical design aware synthesis of the TTI helps to improve the detection accuracy.

c) Signal recovery and TSV limited functional yield: We next study the effectiveness of the pre-bond TSV test and signal recovery on the yield enhancement (Fig. 11). We consider the offset distribution obtained from SPICE simulation. We generate 1000 random instances of a 3-D die with 1500 TSVs and different short resistances. The TSVs are grouped using the proposed circuit in bad/repairable/good groups and if required signal recovery circuit is activated. A die is considered faulty if there exists any TSVs with signal swing <1 V (with or without signal recovery). As expected, with an increase in the variance in the short diameter, the number of good TSVs reduces while that of repairable or bad TSVs increases in Fig. 11(a). This results in yield degradation. The use of signal recovery can improve the TSV yield and allow a circuit to function with less control in the TSV process as shown in Fig. 11(b).

B. Application to Post-Bond Tests and Signal Recovery

We next study the effectiveness of the proposed circuit in post-bond test and characterization of TSVs. After bonding the test structure is re-activated to detect V_{TSV}. For the post-bond test, the driving inverter is in one tier and V_{TSV} is sampled

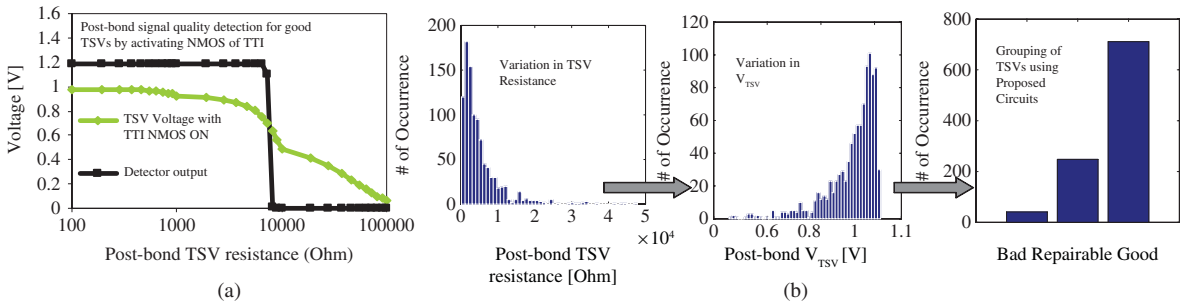


Fig. 12. Post-bond testing and recovery (a) detection with the test circuit and (b) statistical simulation results showing the functionality at post-bond test.

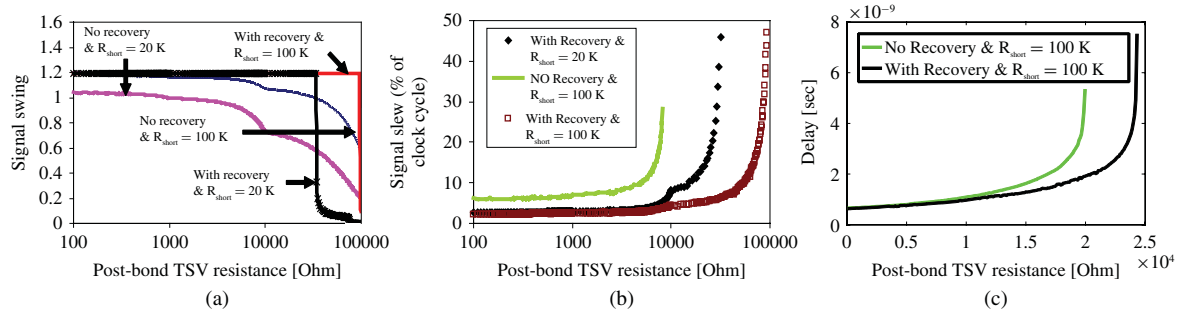


Fig. 13. Post-bond testing and recovery (a) effect on signal swing, (b) signal slew, and (c) delay.

by the test circuit of the other tier. If a particular TSV under test has appreciable R_{short} (i.e., a repairable TSV), the voltage level at the TSV output degrades naturally. For such TSVs signal recovery circuit is activated anyway based on the pre-bond test outcome. Detecting post-bond resistance variation is particularly challenging for the TSVs with no oxide short (i.e., "good" TSVs). Fig. 12(a) illustrates that the proposed circuit detects signal quality even for the good TSVs by activating NMOS of TTI. We observe that V_{TSV} reduces as the post-bond TSV resistance increases. We further perform statistical simulation to verify the functionality of the post-bond test [Fig. 12(b)]. Variation in post-bond TSV resistance results in variation V_{TSV}. Depending on the level of V_{TSV} proposed detection circuit successfully group TSVs as bad, repairable and good after bonding.

We now analyze the effectiveness of the signal recovery to correct against post-bond resistance variation. As shown in Fig. 13(a) and (b), the signal swing and the signal slew degrade significantly with an increase in the post-bond TSV resistance. We observe that the activation of the recovery circuit improves both the signal swing and the signal slew. Fig. 13(c) illustrates that a higher post-bond TSV resistance increases the signal delay. With recovery we can achieve a smaller delay compared to no recovery through TSV, particularly, for high post-bond TSV resistance. The delay improvement is primarily because of the reduction in signal slew as a higher signal slew increases the delay of the following logic gate. Our simulations have shown that when we bypass the signal recovery circuit for good TSVs, the slew at the input of the receiver degrades from ∼14% of clock high-time to ∼17% clock high-time. This is primarily due to the resistance of the transmission gate at the output MUX.

V. System Level Full-Chip Analysis

We analyze the overhead of the proposed test structure considering 3-D full-chip physical design with the 45 nm free PDK technology model [14] and cell libraries.

A. Target 3-D Structure and Design Flow

We use FFT256_8 design [15] to demonstrate our experiment on 3-D circuit. The target 3-D structure is shown in Fig. 14(a) where the two dies are stacked in a face-to-back fashion with via-first TSVs. The TSV structure is also shown in Fig. 14(a).

The 3-D physical design flow [16], [17] is shown in Fig. 15. First, a min-cut practitioner is used to partition the top level design into two dies. Each cut becomes a pin in each die, which corresponds to a TSV. Next, we place TSVs and standard cells sequentially. We convert the TSV pins to TSV standard cells which we define in the physical library. Then we place the TSV cells and standard cells together in the first die using the predefined pin locations as constraints. After placement, we change TSV standard cells back to TSV pins to do routing and optimization. For the second die, we get the TSV landing pad locations from the previous die. With these locations as constraints, we perform placement and routing. The following steps are the same as in the first die. After all the designs are done, we perform 3-D timing analysis. We generate the top-level Verilog file containing these two dies and a SPEF file for TSV parasitics. Primetime reads Verilog files and SPEF files in incremental modes, and generates a stitched SPEF file containing the RC information of both two dies and the TSVs. Then we perform timing analysis on the stitched files. Fig. 14(b) shows the die shot of the two layers.

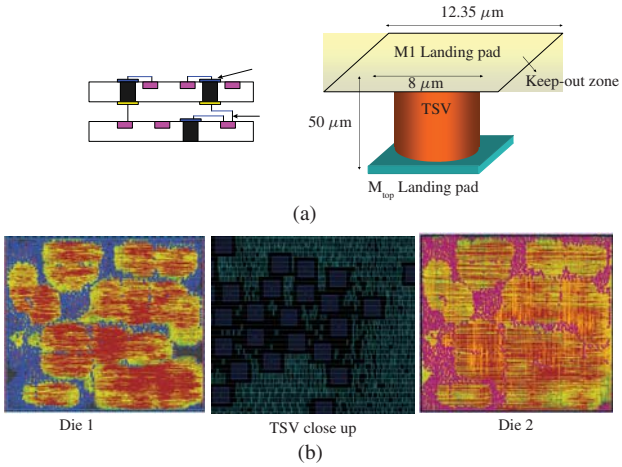


Fig. 14. 3-D system level analysis (a) target 3-D structure and TSV sizes and (b) full-chip layouts of the designed 3-D stack for FFT256_8 circuit.

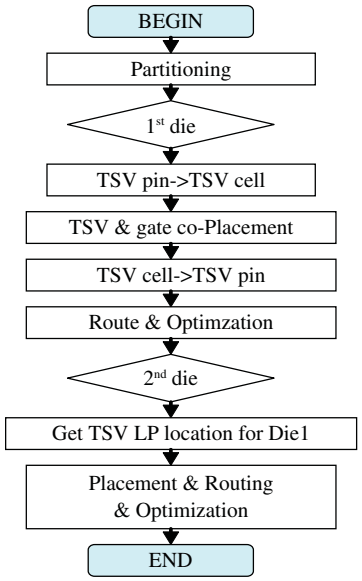


Fig. 15. 3-D design flow used in this paper.

Blue squares in die1 show the TSV M1 landing pads, and the pink squares in die2 show the TSV M6 landing pads. The total number of TSV is 1444. The area per die is 1.08 × 1.08 mm^2.

B. Delay and Power Impact of TSV Test Circuits

We consider the application of the proposed test circuit on the designed 3-D system. We first redesign the proposed test circuit in 45 nm PDK technology and verify its functionality. The physical area of the proposed design in the 45 nm technology is ∼21 μm^2. We add this additional cell to each TSV in our 3-D design flow to estimate the area overhead. For area overhead estimation, we have considered different partition options resulting in different number of TSVs for the entire 3-D chip. The area overhead was observed to be less than 4% of the total die area when TSV area is ∼20% of the die area [Fig. 16(a)].

Next we study the impact of the proposed test/signal recovery circuit on timing and power. SPICE simulation in the

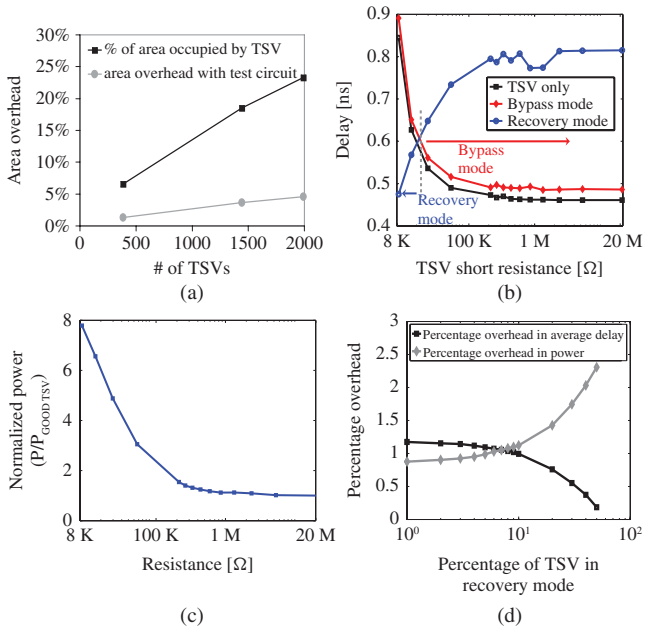


Fig. 16. Area and delay overhead of the proposed structure from system level analysis (a) area overhead, (b) delay overhead of the test circuit in different mode, (c) power overhead of the test circuit in different mode, and (d) tradeoff of delay and power overhead.

predictive 45 nm node is performed to estimate the delay and power of the driver, TSV, test circuit, and receiver combination considering presence/absence of signal recovery. We consider varying resistance of the oxide short to create good and repairable TSVs. It can be observed that with the proposed circuit delay increases marginally for very good TSVs. This is primarily due to the addition of the transmission gate in the signal path. But for the repairable TSVs in recovery mode, we observe a delay reduction through the entire driver–receiver combination due to improvement of the signal slew at the receiver input [Fig. 16(b)]. From a power perspective, the total power remains similar with or without the test-circuit for good TSVs [Fig. 16(c)]. However, for the repairable TSVs the total power increases due to the switching in the signal recovery circuit. A lower short resistance implies a smaller difference between V_{INA} (=V_{TSV}) and V_{INB}(=V_{ref}) in Fig. 6. This implies an increased switching time and hence, a larger short circuit power through the sense-amplifier. However, the power of the proposed design was observed to be less than a microwatt even in the recovery mode.

We next extend the timing/power analysis at the system level. After the timing analysis of the 3-D design is done, we add the timing degradation caused by the repairable TSVs and the test circuit. We assume that the random variations in TSV short resistances (similar to Fig. 9) and add the timing overhead of the proposed test circuit either in the recovery mode or in the bypass mode. Based on this assignment we compute the new delay for the paths that use TSVs. Each random case of across chip TSV resistance variation represents a 3-D chip. We vary the percentage of TSVs that are in the recovery mode from 1% to 50%, and assign different delay and power overhead values to all the 3-D timing paths

based on their working modes (i.e., recovery or bypass). Note the delay/power overhead is computed with respect to the design where the test and signal recovery circuit is not added to the TSVs. As shown in Fig. 16(d), the average delay overhead decreases as the number of TSVs in recovery mode increases. However, a higher number of TSVs in the recovery mode increases the power overhead. This is expected as the test circuit consumes more power in the recovery mode [Fig. 16(c)]. However, even with 50% of TSVs in the recovery mode, the chip level power overhead is marginal.

VI. Conclusion

In this paper, we have presented a test structure to detect the effect of TSV defects on the signal quality of a 3-D system. The proposed structure can be used during the pre-bond test to detect the resistive shorts through oxide liners. During the post-bond test, the structure can be used to characterize the effect of variation in the TSV resistance on signal quality. Depending on the detected signal quality, the proposed structure reconfigures itself to perform signal recovery. This allows improving the yield of 3-D system while maintaining the signal fidelity. The full-chip analysis shows that the signal quality enhancement can be achieved with only moderate overheads in chip area, power, and maximum delay. As the variability and defects in TSVs and bonding process are major challenges in the 3-D process flow, the proposed structure can help to improve the functional yield and signal fidelity in the next generation 3-D ICs.

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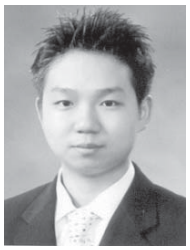

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