Full-Chip TSV-to-TSV Coupling Analysis and Optimization in 3D IC

Chang Liu[1], Taigon Song[1], Jonghyun Cho[2], Joohee Kim[2], Joungho Kim[2], and Sung Kyu Lim[1]
[1]School of Electrical and Computer Engineering, Georgia Institute of Technology, U.S.A.
[2]School of Electrical Engineering, Korea Advanced Institute of Science and Technology, Korea
{chang.liu,taigon.song,limsk}@gatech.edu

ABSTRACT

This paper studies TSV-to-TSV coupling in 3D ICs. A full-chip SI analysis flow is proposed based on the proposed coupling model. Analysis results show that TSVs cause significant coupling noise and timing problems despite that TSV count is much smaller compared with the gate count. Two approaches are proposed to alleviate TSV-to-TSV coupling, namely TSV shielding and buffer insertion. Analysis results show that both approaches are effective in reducing the TSV-caused-coupling and improving timing.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

General Terms

Design

Keywords

3D IC, TSV-to-TSV coupling

1. INTRODUCTION

Through-Silicon-Via (TSV) and 3D stacking technology are currently being actively evaluated as a potential solution to alleviate the interconnect delay problems in giga-scale circuits and systems [7]. Some works have been done to show that 3D ICs have advantages in total wire length [1] and timing performance [4] compared with 2D ICs.

However, signal integrity (SI) is another key challenge caused by the advance of nano-scale interconnect technologies because of the rising number of analog effects. Due to the big size of TSVs, it is highly possible that TSVs will introduce new coupling sources, which are bad to the circuit's SI performance. A big coupling noise between interconnections has two major impacts on the circuit performance. First, it increases the path delay due to Miller effect. When the aggressor and the victim signals switch in the opposite direction, the effective coupling capacitance between them doubles and thus degrades timing. Second, the coupling noise can result in a wrong logic function. For dynamic logic, the coupling noise causes charge-sharing, which may flip the signal unintentionally. For static logic, the coupling noise can change the state of the sequential element by flipping the cross-coupled inverter loop.

Several works have been done to illustrate the impact of TSVs on SI in 3D ICs [8, 6]. However, those studies only look at simple individual coupling cases in device level. To gain comprehensive understanding of SI issues in 3D ICs, we still need to answer the following two questions: (1) How much SI issues do the TSVs cause to the 3D IC design from a full-chip perspective? (2) If the impact of TSVs to the full-ship SI is non-negligible, how should we alleviate the TSV-caused coupling problem from a designer's perspective? This paper tries to answer these two questions.

The main contribution of this work includes the following: (1) We study the on-chip TSV-to-TSV coupling and present a compact circuit model for full-chip SI analysis. In addition, we for the first time observed that changing the distance between TSVs is inefficient in reducing TSV-to-TSV coupling level for low frequency signals (under a few GHz). (2) We, for the first time, perform full-chip 3D SI analysis using an accurate TSV-to-TSV coupling circuit model. Analysis results show that TSV-to-TSV coupling has a big impact on the full-chip coupling noise and timing performance. (3) We propose and compare two approaches for full-chip optimization to alleviate the TSV-caused coupling problem, namely, buffer insertion and TSV shielding.

2. TSV-INDUCED COUPLING MODEL

2.1 Coupling Sources Due to TSVs

TSVs introduce several new coupling sources to 3D ICs. The first coupling source is from the big TSV landing pad to the wires and devices. Considering the TSV landing pad is big (typically 25 μm^2) which occupies several standard cell rows, the metal wire running above or next to it will suffer from significant coupling capacitance. Fortunately, this coupling source can be analyzed by existing SI tools easily, because it is essentially a traditional wire coupling problem.

Another coupling source is TSV-to-device coupling. This coupling happens between the TSV and the S/D region of the MOSFET through the substrate. The coupling path is mainly on the silicon-bulk surface, which can be well controlled by substrate contact. Therefore, by adding sufficient substrate contact, the surface can be strongly tied to ground, thus alleviating TSV-to-device coupling.

The third coupling source is from TSV-to-TSV coupling. Different from TSV-to-device coupling, TSV-to-TSV coupling happens not only on the silicon-bulk surface, but also deep inside the substrate, because TSV is a via that goes through the entire substrate. Considering the height of the TSV (typically 50μm-100μm), simply adding substrate contact cannot guarantee to eliminate this coupling. Therefore, TSV-to-TSV coupling usually cannot be ignored. Moreover, TSV-to-TSV coupling scheme is totally different from the traditional wire coupling. In wire coupling case, two wires and the dielectric between them form a capacitor, through which the two wires are coupled. In contrast, TSV-to-TSV coupling is more complicated. Two TSVs are coupled through two liner layers and

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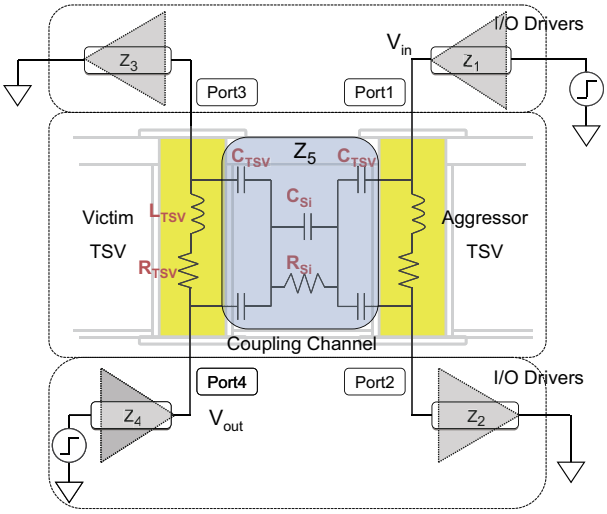

Figure 1: TSV-to-TSV coupling model

the silicon substrate, which cannot be treated as a single capacitor. Because of this difference, it is difficult for existing SI analysis tools to directly handle TSV-to-TSV coupling. Due to these reasons, we focus on the TSV-to-TSV coupling issues.

2.2 TSV-to-TSV Coupling Modeling

Recently, there have been several works presented to investigate TSV-to-TSV coupling from the device level. [8] studied a specific case, where 9 TSVs are placed as a 3×3 array. [6] gave an analytical model for the coupling capacitance between TSVs. However, these models ignore the TSV liner, which has big contributions to TSV coupling.

In this paper we propose a TSV-to-TSV coupling model for full-chip coupling analysis. Unlike vias in PCBs and packages, TSVs inside ICs are surrounded by a thin liner. In addition, silicon substrate is very lossy, and has not only resistive components, but also capacitive components. Therefore, the TSV-to-TSV structure must contain all components in the coupling path, including TSV copper, liner layer, silicon substrate and I/O drivers. Figure 1 shows an equivalent circuit model for the TSV-to-TSV coupling structure. A similar TSV modeling work [2] also considered these components. However, this model was devised to analyze signal transmission, and only considered 1 signal TSV with 2 ground TSV case.

In the modeling process, a TSV can be modeled by a resistor ($R_{\rm TSV}$) and an inductor ($L_{\rm TSV}$) in series, and the liner which surrounds TSV could be modeled as a capacitor ($C_{\rm TSV}$). Silicon substrate could be modeled by a resistor ($R_{\rm si}$) and a capacitor ($C_{\rm si}$) which is in parallel. We use the following equations to calculate the value of these components:

$$C_{\rm TSV} = \frac{1}{4}\frac{2\pi\epsilon_0\epsilon_{\rm r}}{\ln\frac{r_{\rm TSV}+t_{\rm ox}}{r_{\rm TSV}}} \cdot l_{\rm TSV} \quad (1)$$

$$C_{\rm si} = \frac{\pi\epsilon_0\epsilon_{\rm r}}{\ln\{\frac{d}{2r_{TSV}} + \sqrt{(\frac{d}{2r_{TSV}})^2 - 1}\}} \quad (2)$$

$$R_{\rm si} = \frac{\epsilon}{C_{\rm si}\sigma} \quad (3)$$

where $r_{\rm TSV}$ is the TSV radius, $l_{\rm TSV}$ is the TSV height, $t_{\rm ox}$ is the thickness of the liner, and d is the pitch between two TSVs.

This lumped circuit model is validated by a commercial 3D electromagnetic simulator (Ansoft HFSS) using S-parameter simulation. A simulation structure built for HFSS is shown in Figure 2(a).

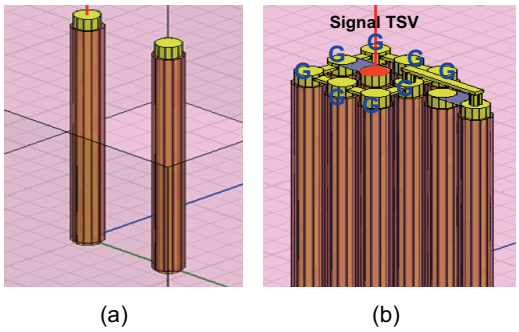

Figure 2: Coupling structure for HFSS simulation. (a) two signal TSVs, (b) one unshielded and one shielded signal TSV (= surrounded by 8 ground TSVs) shown in red

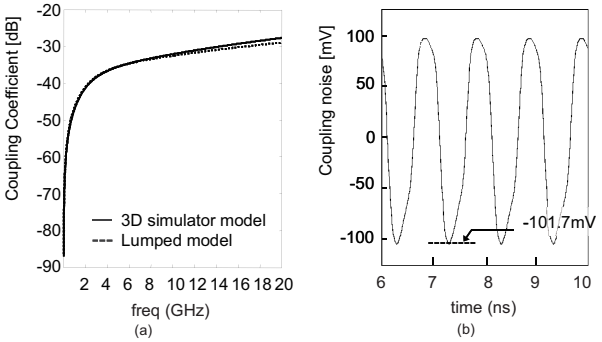

Figure 3: (a) S-parameter simulation for coupling coefficient. (b) Transient response for the victim TSV in a coupled TSV pair shown in Figure 2(a)

Figure 3(a) shows the S-parameter result comparison between the HFSS structure and the lumped model. We see the model is very accurate in the simulated frequency range. We use this lumped model to perform transient simulation and measure the coupling noise on the victim TSV. The simulation is performed using 45nm technology with 1.2V power supply. Simulation result shows that the peak-to-peak coupling noise can reach up to 200mV, which is non-negligible, as shown in Figure 3(b).

3. FULL-CHIP SI ANALYSIS

By studying the simple TSV coupling pair, we showed that TSV-to-TSV coupling is non-negligible in Section 2. However, compared with the standard cell count, the TSV count is much smaller in a realistic design. Therefore, whether TSV coupling will cause troubles in a real digital design will still be a question. In this section, we try to answer this question by performing full-chip SI analysis while considering TSV-related coupling. The TSV-related coupling we are dealing with in this paper is mainly TSV landing-pad related coupling and TSV-to-TSV coupling. The former can be handled by existing tools (CeltIC, Primetime, etc). We use the coupling model developed in Section 2 to help analyze TSV-to-TSV coupling.

3.1 Full Chip 3D SI Analysis Flow

Currently, existing SI analysis tools cannot well handle 3D circuits. There are two major reasons. First, 3D SI analysis tool must consider all nets and all TSVs in all the tiers simultaneously. This

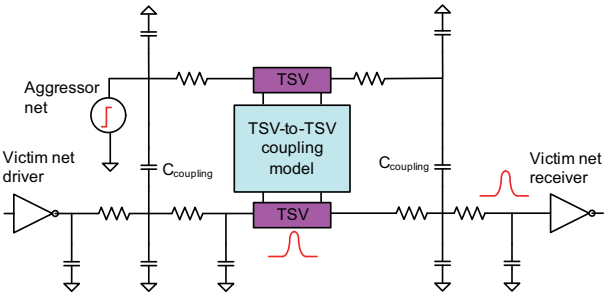

Figure 4: An example of a SPICE netlist for coupling noise analysis

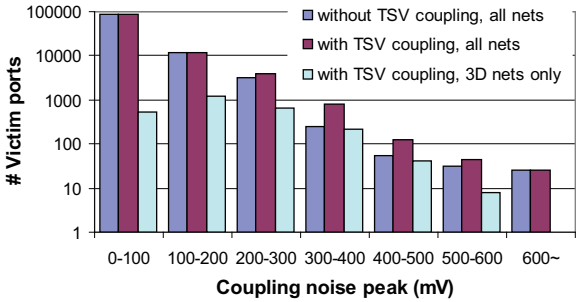

Figure 5: Glitch analysis results comparison

is because the total noise experienced by a 3D net may come from coupling within the same tier as well as neighboring tiers. Second, current SI analysis tools can only handle simple wire-to-wire capacitive coupling. As discussed in Section 2, TSV-to-TSV coupling consists of complicated coupling network, which cannot be handled by existing SI analysis tools.

To solve these two problems, we designed our 3D SI flow, which utilizes our own scripts in combination with the existing circuit simulation (= HSPICE) tools and timing analysis (= PrimeTime) tools. First, we use RC extraction tool to obtain the SPEF files containing the interconnect RC information for each die. Then a top-level verilog file and a top-level SPEF file are generated containing all the dies using our in-house tool. We also make a script to find out which TSVs interfere with each other based on their locations and record the TSV-to-TSV coupling information.

Once these files are ready, we use PrimeTime to read in verilog files and SPEF files in incremental mode, and generate a new stitched SPEF file containing the RC information of all the dies and the TSVs. Then we use our script to analyze the stitched SPEF file and generate the SPICE netlists for each individual net for coupling noise simulation. Note that each individual net contains the wire coupling information obtained from RC extraction. During SPICE netlist generation, the script also automatically plugs in the TSV-to-TSV coupling circuit model based on the TSV-coupling model in Section 2. Then the aggressor signal and victim driver model are also applied to the SPICE netlist. Using the generated SPICE netlists as shown in Figure 4, we perform SPICE simulation on each victim nets one by one, and record the peak noise at each port.

3.2 Design and Analysis Results

We use FIR32, which is a 32-bit FIR filter as a test circuit. The circuit has 35K gates and 548 TSVs. The design is a 2-die 3D IC based on 45nm technology. Our TSV is $4\mu m$ in diameter and $60\mu m$ in height. The TSV landing pad is $5 \times 5\mu m$, which occupies 3 standard-cell rows. Each TSV also has a $0.5\mu m$ keep-out zone, where no cells can be placed inside. We use our Cadence Encounter-based tool flow to generate 3D layouts [3]. The 3D timing optimization is performed using the timing-scaling method in [3]. In the following experiments, we use both original design and timing-optimized design for comparison.

After the designs are ready, we perform coupling noise analysis using the proposed flow. The analysis compares two cases with and without considering TSV-to-TSV coupling. Based on the analysis results, we have two major observations. First, TSV-to-TSV coupling increases the total coupling-noise. The total noise for the original design increases from 4518V to 4955V after considering TSV-to-TSV coupling. The total coupling noise on 3D nets is 471V, which is responsible for most of the total noise increase. Second, the contribution of TSV-to-TSV coupling is more on the high noise region. Figure 5 shows the coupling-noise distribution comparison. We also show the noise distribution only on 3D nets. We observe that after considering TSV-to-TSV coupling, the design has more victim ports with noise above 300mV. The average coupling noise on a 3D net is 170mV, which is 3 times more than that on the a 2D net (43mV). In summary, although the TSV count is much smaller than the gate count, it can still cause non-negligible coupling noise problem, especially in the high-noise region.

Besides coupling noise, TSV coupling also has significant contribution to timing degradation. We perform timing analysis on both original design and timing optimized design. The results show that due to TSV coupling, the longest-path-delay (LPD) almost doubles compared with the design without TSV-to-TSV coupling. A similar trend exists for the total negative slack (TNS). Table 1 summarizes the overall analysis results on the impact of TSV-to-TSV coupling.

4. TSV-TO-TSV COUPLING REDUCTION

After realizing that TSV-to-TSV coupling has significant contributions to the SI and timing performance degradation, we need to find solutions to reduce TSV coupling. We start from analyzing the coupling model in Figure 1. For simplification, we ignore the TSV resistance and inductance because they are very small. Using this simplified model, we derive the transfer function from V_{in} to V_{out} using Kirchhoff's law, as shown in Equation (4):

$$V_{out} = V_{\text{in}} \cdot \frac{Z_2 Z_3 Z_4}{Z_1 \cdot Z_A + Z_2 Z_3 Z_4 + Z_5 \cdot Z_B} \tag{4}$$

where

$$Z_A = Z_2 Z_3 + Z_2 Z_4 + Z_3 Z_4 + Z_3 Z_5 \tag{5}$$

$$Z_B = Z_1 Z_4 + Z_2 Z_3 + Z_2 Z_4 \tag{6}$$

$$Z_5 = Z_{C_{si}} // Z_{R_{\text{si}}} + 2 Z_{C_{\text{TSV}}} \tag{7}$$

Equation (4) shows that the coupling level between two TSVs depends on the coupling-channel impedance (Z_5), the termination condition (Z_2, Z_3, Z_4) and the driver condition (Z_1). In another words, to reduce the coupling level, we can either increase the channel impedance, decrease the port impedance at the victim net, or increase the impedance at the aggressor driving port. From a designer's perspective, possible methods include: (1) increase TSV distances (to increase Z_5), (2) shield the victim TSVs (to cutoff the coupling path and increase Z_5), (3) insert buffers at the victim net (to decrease Z_4), (4) decrease the driver size at the aggressor net. (to increase Z_1), and (5) increase the load at both victim and aggressor net (to decrease Z_3 and Z_2). Since option 4 and 5 have negative implications to timing performance, our focus is on the first three options.

4.1 Why TSV Spacing Is Inefficient

To solve the traditional wire coupling problem, the most intuitive way is to increase the distance between the coupled wires. However, for TSV-to-TSV coupling, increasing the TSV distance is not an effective method, which is completely different from wire

Table 1: Impact of TSV-to-TSV coupling on crosstalk and timing

	Original design w/o TSV coupling	Original design with TSV coupling	Timing-opt design w/o TSV coupling	Timing-opt design with TSV coupling
Footprint (μm^2)	402×402	402×402	402×402	402×402
Wirelength (μm)	7.506×10^5	7.506×10^5	7.516×10^5	7.516×10^5
Total coupling noise (V)	4518.75	4955.15	4230.74	4548.17
Longest path delay (ns)	13.09	22.79	5.54	9.24
Total negative slack (ns)	600.498	1175.14	335.076	836.88

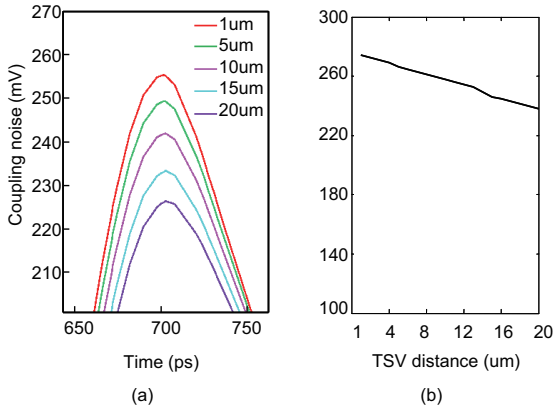

Figure 6: Glitch peak with different TSV distances. (a) shows the transient response of the victim TSV, (b) shows the relationship between coupling noise peak and TSV distance

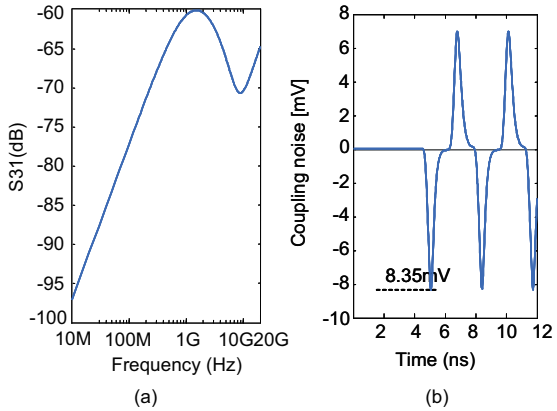

Figure 7: (a) S-parameter results of coupling coefficient (b) transient simulation for the coupling noise on the shielded TSV

coupling. This is because in low frequency region (under a few GHz), the coupling channel impedance Z_5 is mainly determined by C_{TSV}. Increasing the TSV distance has big impact on R_{si} and C_{si}, but has little impact on C_{TSV}. Therefore, the total coupling channel impedance Z_5 is not sensitive to the TSV distance. To verify this, we perform transient simulations to examine the coupling noise variation with different TSV distances. The signal frequency is 300MHz with 1.2V power supply. Figure 6(a) and (b) show the victim transient response with different TSV distances. When TSV distance varies from $1\mu m$ to 20 μm, the glitch noise only decreases from 255mV to 224 mV. Therefore, trying to reduce TSV coupling by increasing the TSV distance proves to be inefficient. Thus, we exclude TSV repositioning from the potential solutions.

4.2 TSV Shielding to Alleviate Coupling

Similar to the coaxial cable, we use ground TSVs to shield a sensitive signal TSV as shown in Figure 2(b). By doing this, the coupling path through the substrate is cutoff so that the coupling from other signal TSVs is minimized. To verify how effective the shielded structure is in term of coupling noise reduction, we create an HFSS structure, which consists of a shielded TSV and an aggressor TSV as shown in Figure 2(b), and perform S-parameter and transient simulations. The shielding structure we use contains 8 ground TSVs. We apply an aggressor signal to the aggressor TSV nearby. S-parameter simulation result in Figure 7(a) shows that the coupling level between the two signal TSVs is below -60dB. Transient simulation result in Figure 7(b) shows that the coupling noise is below 10mV, which agrees with the S-parameter simulation. Therefore, we conclude that with the proposed shielding structure, the coupling between the shielded TSV and neighboring signal TSV is negligible.

Based on this observation, we propose a design optimization flow utilizing shielded TSVs. This flow is performed after cell placement. The basic idea is to gradually replace TSVs which suffer from severe coupling with shielded TSVs. To perform this optimization flow, we need to define a new shielded TSV cell in the standard cell library. Since the shielded TSV cell is much larger than a regular TSV, we need to pay for a bigger footprint area.

In our flow, all the TSV pins are converted into TSV cells first. Using the coupling model in Figure 1, the TSVs are then sorted by the coupling-path impedance. As we discussed in the beginning of this section, the smaller the total impedance is, the bigger the coupling level is. Then, we generate a TSV list, which contains TSVs to be replaced with shielded TSV cells. To generate the list, we start from the TSV with highest coupling level and gradually choose the TSVs based on the coupling level order until we reach the coupling level threshold. After one TSV is chosen, we mark all its neighbors so that they will not be chosen. The reason why we skip the neighbors is that we do not want the shielded TSVs to gather together because it is likely to cause over compensation. After we obtain the TSV list, we recalculate the chip area based on the number of TSVs shielded and redo floorplanning. Then we replace the TSVs in the list with shielded TSVs and perform ECO placement to remove the overlaps. We perform this flow iteratively until total TSV coupling level is below the desired value.

Figure 8(b) shows the layout after TSV shielding. There are 118 TSV cells replaced with shielded TSV cells. As a result, the total chip area increases from $402 \times 402\mu m$ to $421 \times 421\mu m$. Based on this layout, we perform routing and perform full-chip noise analysis and timing analysis. Table 2 summarizes the analysis results. We see that TSV shielding reduces total coupling noise from 4955.15V to 3376.98V for the original design, and from 4548.17V to 3032.16V for the timing-optimized design. Note that this noise reduction is not only from the 3D nets, but also from the 2D nets because of the less congested routing resulted from the increased area. If we only look at the coupling noise on 3D nets, the total coupling noise decreases from 473.07V to 273.46V for the original design. Table 3 shows the noise distribution comparison for 3D nets between the original design and the TSV-shielded design. We see that compared with the original design, the noise distribu-

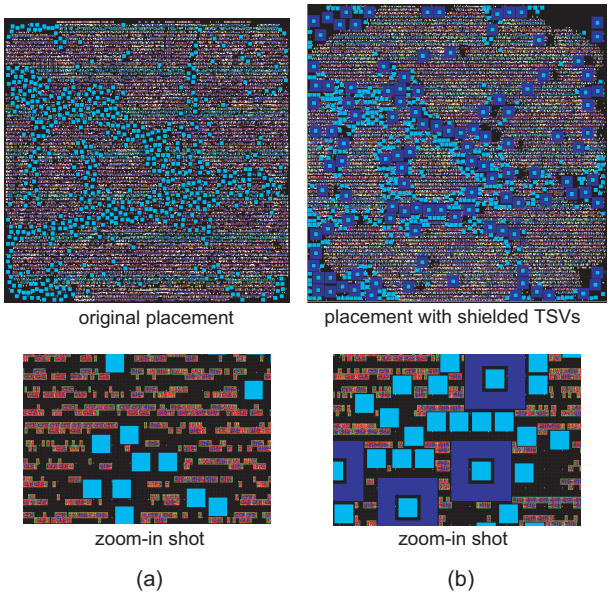

Figure 8: Various die shots using Virtuoso. Blue squares denote M1 TSV landing pads. (a) Original design (b) Design with shielded TSVs

Table 2: TSV shielding results. We report the area in μm^2, coupling noise in V, and delay/slack in ns.

	Original design	Original + shielding	Timing optimized	Timing + shielding
Area	402×402	421×421	402×402	421×421
Shielded-TSV count	0	118	0	118
Total noise	4955.15	3376.98	4548.17	3032.16
Total noise (3D nets)	471.091	273.46	329.967	226.525
Longest path delay	22.79	12.86	9.24	6.34
Total negative slack	1175.14	706.581	806.88	371.175

tion moves to the low-noise region. We observe that the same trend exists in the timing-optimized design.

Besides coupling noise reduction, the timing performance also improves. As shown in Table 2, the longest path delay reduces from 22.79 ns to 12.86 ns for the original design, and from 9.24 ns to 6.24 ns for the timing-optimized design. We observe the same trend on the total negative slack. Therefore, we conclude that TSV shielding is an effective way in alleviating TSV-caused crosstalk and timing problems. However, the cost we need to pay is the increased area.

4.3 Buffer Insertion to Alleviate Coupling

Another effective way to alleviate TSV-to-TSV coupling problem is buffer insertion. As discussed earlier, TSV-to-TSV coupling-caused glitch level is strongly sensitive to the port impedance. Buffer insertion before TSVs helps reduce the victim driving port impedance. To demonstrate the effectiveness of buffer insertion, we choose a 3D net, which is extracted from the SPEF file with the TSV coupling model in Figure 1 plugged in, and is originally driven by a 2X driver. We insert a 4X buffer before the TSV and perform SPICE simulation, as shown in Figure 9(a). Table 4 lists the coupling noise simulation results. We see that the coupling noise reduces by 70%, and the path delay also reduces by 65%.

Despite the fact that buffer insertion is effective in reducing TSV-to-TSV coupling noise, we still face the following question. Since timing optimization engine will insert a lot of buffers for timing

Table 3: Coupling noise peak (in mV) distribution. We report # of 3D victim net ports before and after TSV shielding.

Noise	0-100	100-200	200-300	300-400	400-500	500-600
Before	539	1254	659	210	41	8
After	1539	727	314	119	12	0

Table 4: Impact of buffer insertion on the 3D net. We report the glitch noise in V and delay in ns.

	Original net	Buffer near TSV	Buffer near driver
Noise @ receiver	0.4058	0.1207	0.1624
Noise @ TSV	0.4059	0.1207	0.1624
Delay	0.278	0.09701	0.09899

purpose, is it enough to only use timing optimization engines to solve the TSV-to-TSV coupling problems? Here, we give a negative answer because of the following two reasons. First, the timing engine cannot see the TSV-to-TSV coupling, and will not consider the TSV-to-TSV coupling-caused-delay in timing optimization. Second, even if the timing engine is able to consider TSV-to-TSV coupling for timing optimization, it is still not enough to solve coupling noise problem. This is because coupling-noise aware buffer insertion requires buffers to be inserted close to the TSV, while timing-aware engine does not necessarily insert buffers close to the TSV. This is because delay is not sensitive to the buffer locations in the 3D net, which is very different from the 2D net. In short, for a 3D net, coupling noise is very sensitive to buffer-to-TSV distance, while timing is not. To illustrate this, we use the circuit in Figure 9 to study the impact of buffer-to-TSV distance. In this experiment, we compare two cases where buffer is close to TSV and buffer is close to the original driver as shown in Figure 9 (a) and (b). We perform both glitch noise simulation and delay simulation on these two cases.

Table 4 shows the simulation results. We see that after we move the buffer from the driver end to the TSV end, the glitch at the receiver end reduces by 26%, while the delay decreases by 1.9%. This phenomenon is because of the resistive shielding effect [5]. A 3D net is a non-uniform net because of the TSV. If we model a TSV as a big capacitance, the resistive shielding effect from the wire will be applied to this capacitance. Therefore, the Elmore delay model is not effective. Our further experiment shows that a TSV has about 200um freedom to move between buffers without significantly changing delay.

Since timing-aware buffer insertion is not enough in reducing the TSV-to-TSV coupling noise, we propose an SI-aware buffering approach to co-optimize timing and SI. First, we perform coupling analysis for all the TSVs. Based on their coupling levels, we insert buffers with different sizes right before the TSVs. Then we perform timing optimization considering the TSV and its buffer as a single cell. One merit of this approach is that each TSV is shielded by the buffer so that we can use 2D optimization tool to optimize the design with proper timing constraints.

Figure 10 shows the buffers inserted in both dies associated with the TSV landing pads. Table 5 shows the crosstalk and timing analysis results for 4 designs: original design, original design with SI-aware buffer insertion, timing-optimized design and SI-timing co-optimized design. The results in Table 5 show that buffer insertion is very effective in reducing the coupling-noise for 3D nets. Using the buffer-before-timing approach, we obtained the best critical path delay number. Of course, we need to the pay for the cost of higher power consumption due to the inserted buffers.

4.4 Overall Comparison

Figure 11 presents an overall comparison between various optimization methods. We see that both buffer insertion and TSV-

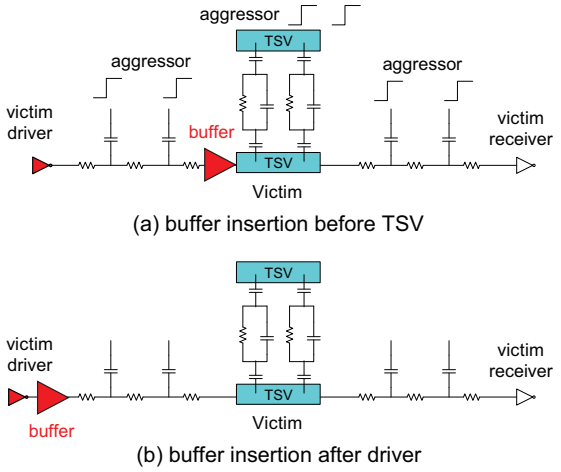

Figure 9: Coupling reduction with buffering

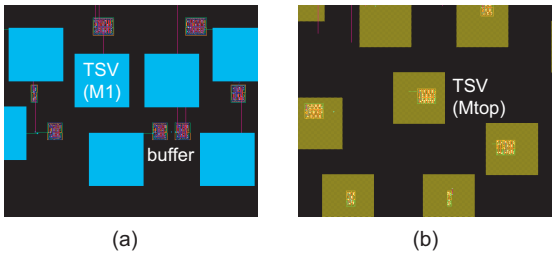

Figure 10: Buffers inserted in the layout of (a) top die (b) bottom die. Yellow squares are TSV landing pads on Mtop, which can overlap with buffers in the device layer of the bottom die.

shielding are effective in alleviating TSV-to-TSV coupling caused problems. However, for 3D-net noise reduction, buffer insertion is more effective. This is because we can afford to insert buffers before every TSVs for noise reduction, but we can only afford to choose some TSVs for shielding due to the increased area cost. If we shield every TSV in this design, the total area increases significantly, which is not affordable. On the other hand, TSV shielding has the advantage of lowering the total coupling noise. The 2D net noise also reduces due to the increased chip area. In terms of timing performance, buffer insertion works better than TSV-shielding. This is not only because of the shielded-TSV number constraints, but also because TSV-shielding results in longer wirelength due to the larger chip area. Finally, TSV-shielding achieves lower power consumption than buffer insertion. This is simply because adding more buffers will increase the power consumption significantly. Considering the larger chip area, TSV-shielding also has the advantage of a lower power density.

5. CONCLUSIONS

In this paper we studied the impact of TSV-to-TSV coupling issues in 3D ICs. Based on HFSS and SPICE simulations, we demonstrated that TSV-to-TSV coupling is more sensitive to terminal impedance than TSV distance. A compact TSV-to-TSV coupling model is developed for full-chip 3D signal integrity analysis. Using this model, a SPICE-based full-chip coupling analysis flow is developed. The 3D SI results show that TSV-to-TSV coupling has a big contribution to the total glitch noise and timing degradation. To alleviate TSV-to-TSV coupling, two approaches are proposed from a designer's perspective. Experimental results show that both TSV shielding and buffer insertion are helpful to improve

Table 5: Buffer insertion results. We report the coupling noise in V, and delay/slack in ns.

	original design	SI-aware buffering	timing-aware buffering	SI+timing buffering
Total buffer count	357	722	556	808
Total noise	4955.15	4513.11	4548.17	4301.6
Total noise (3D nets)	471.091	82.8308	329.967	73.0874
Longest path delay	22.79	6.98	9.24	5.64
Total negative slack	1175.14	469.625	806.88	431.712

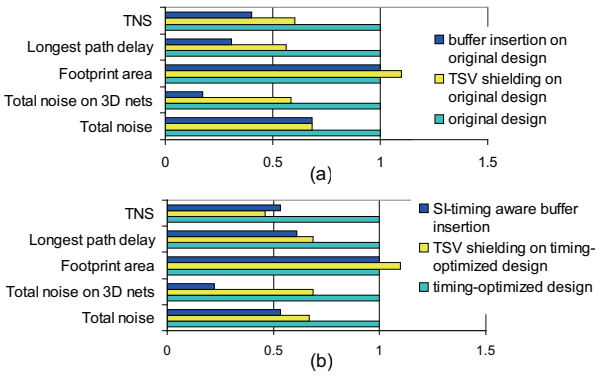

Figure 11: Design and TSV-coupling optimization summary of (a) original design (b) timing-optimized design

SI as well as timing performance. Future work will focus on developing more accurate TSV related coupling model, including TSV-to-device and TSV-to-wire coupling models. The impact of different TSV placement styles on full-chip SI will also be studied, including random placement, regular placement and TSV array.

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