A Study of TSV Variation Impact on Power Supply Noise

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***Abstract*—In this work, we study the through-silicon-via (TSV) RC variation impact on 3D power delivery network (PDN). First, we model TSV RC variation due to process variation. Then, we perform sign-off power supply noise analysis of 3D PDN in GDSII layouts which contain power/ground (P/G) TSV RC variation model. We explore the effect of TSV RC variation range, number of variation sources (P/G TSV count), number of C4 bumps and TSV size on the robustness of PDN under TSV RC variation. Our results show that TSV RC variations cause negligible influence on 3D PDN due to much smaller parasitic values of TSVs compared with that of entire PDN.**

I. Introduction

Power delivery is believed to be one of the biggest challenges in 3D stacked ICs. Even though there are many works on 3D power delivery network (PDN), there is no work on TSV RC variation impact on power supply noise in 3D PDN, to the best of our knowledge. Process variation has been critical issues of semiconductor fabrication process, which affects yield, performance, and power consumption. These process variations change the TSV parasitic characteristics, hence affect the quality of PDN. In this work, we explore the impact of TSV RC parasitic variation on the robustness of 3D PDN.

Our main contributions are as follows. First, we model TSV RC variation due to process variation. We perform both static (IR-drop) and dynamic noise (voltage droop) analysis on GDSII level 3D IC layouts with TSV RC variation model using existing 2D commercial sign-off level analysis tools. We explore the impact of number of variation sources (P/G TSV count), number of P/G bumps, and TSV RC variation range on the power supply noise. Also we investigate the impact of P/G TSV size and its variation on the 3D PDN quality.

II. TSV RC Variation

Process variations on TSVs are inevitable due to factors such as misalignment, TSV diameter/height and oxide thickness variation, wafer surface cleanliness and roughness. However, extreme misalignment, which causes a systematic variations and increases contact resistance, is highly unlikely in state-of-the-art wafer bonding processes [1]. Thus, TSV RC parasitic variation can be modeled as random effects. In this section, we model TSV RC variation based on TSV dimension variation using analytical models. We ignore TSV inductance since inductive voltage drop by TSV is comparable only for frequencies above several GHz [2], which is not the case for PDN.

A. R_{TSV} variation

The analytical expression of the dc resistance of TSV is given by

$$R_{TSV} = \frac{\rho l_{TSV}}{\pi r_{TSV}^2} \quad (1)$$

where ρ is the resistivity of conducting material, and r_{TSV} and l_{TSV} represent the radius and height of TSV, respectively. With Cu TSV conductor, the resistivity is 16.8 nΩ·m at 20°C. Also, we adopt a contact resistivity of 0.45 $\Omega \cdot \mu m^2$ from measured data based on Cu

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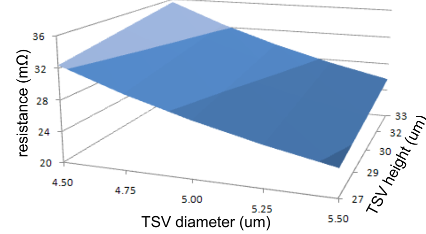

Fig. 1. TSV resistance vs. TSV diameter and height variation

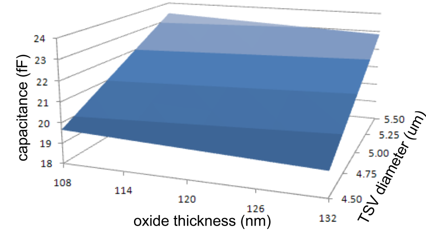

Fig. 2. TSV capacitance vs. TSV diameter and oxide thickness variation

direct bonding [3]. Thus, total TSV resistance is sum of TSV dc resistance and contact resistance.

We use a TSV with 5 μm diameter, 30 μm height, and 120 nm oxide thickness as a baseline TSV structure. Then, we vary both diameter and height by $\pm$10% of nominal values to model process variation. TSV diameter shows superlinear relationship with TSV resistance while TSV height has linear dependency shown in Figure 1. With fixed TSV height of 30 μm and $\pm$10% of TSV diameter variation, TSV resistance changes from -13.6% to +19.3% of the nominal TSV resistance.

B. C_{TSV} variation

The nature of the TSV C-V characteristics is similar to the planar MOS capacitor such that accumulation capacitance is the oxide capacitance given as [2]

$$C_{TSVacc} = C_{ox} = \frac{2\pi\epsilon_{ox} l_{TSV}}{ln(\frac{t_{ox}+r_{TSV}}{r_{TSV}})} \quad (2)$$

As the TSV bias increases, the depletion capacitance acts in series with the oxide capacitance, which is given by

$$C_{TSVdep} = \frac{2\pi\epsilon_{si} l_{TSV}}{ln(\frac{t_{ox}+r_{TSV}+d_{dep}}{t_{ox}+r_{TSV}})} \quad (3)$$

where t_{ox} is the TSV oxide thickness and d_{dep} is the depletion width in silicon substrate. We assume that substrate doping is $2\times10^{15}/cm^3$.

The effective TSV capacitance is the series combination of oxide and depletion capacitances given by

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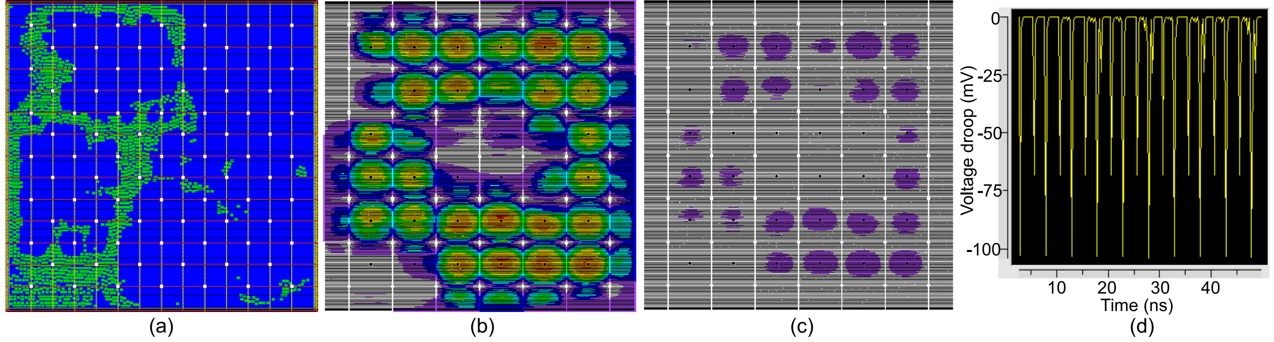

Fig. 3. Layout and power supply noise maps in the bottom die of ind1. (a) Layout. White rectangles are P/G TSVs and green rectangles are signal TSVs. (b) Dynamic noise map. Red color represents noisy spots. (c) Static noise map. (d) Transient voltage waveform of noisy region.

TABLE I
IMPACT OF TSV RC VARIATION RANGE.

TSV capacitance variation (unit: fF)	TSV resistance variation (unit: $m\Omega$)											
	$N(45.6,(0.1\times45.6)^2)$				$N(45.6,(0.2\times45.6)^2)$				$N(45.6,(0.3\times45.6)^2)$			
	worst static noise (mV)		worst dynamic noise (mV)		worst static noise (mV)		worst dynamic noise (mV)		worst static noise (mV)		worst dynamic noise (mV)	
	mean	% σ/m	mean	% σ/m	mean	% σ/m	mean	% σ/m	mean	% σ/m	mean	% σ/m
$N(35.5,(0.1\times35.5)^2)$	10.562	0	133.055	0.00014	10.562	0	133.055	0.00022	10.562	0	133.055	0.00030
$N(35.5,(0.2\times35.5)^2)$	10.562	0	133.055	0	10.562	0	133.055	0.00030	10.562	0	133.055	0.00024
$N(35.5,(0.3\times35.5)^2)$	10.562	0	133.055	0.00015	10.562	0	133.055	0.00022	10.562	0	133.055	0.00029

$$C_{TSV} = \frac{C_{ox}C_{TSVdep}}{C_{ox}+C_{TSVdep}} \tag{4}$$

Even though TSV height has direct impact on capacitance value, its percent deviation from the nominal value will be smaller compared with TSV diameter and oxide thickness. This is mainly because TSV height is several times larger than TSV diameter. Thus, we focus on the impact of TSV diameter and oxide thickness variation on TSV capacitance variation. We vary both TSV diameter and oxide thickness by by $\pm10\%$ of nominal values. Figure 2 shows that impact of oxide thickness variation on TSV capacitance is negligible. With fixed oxide thickness and $\pm10\%$ of TSV diameter variation, TSV capacitance changes from -8.6% to +8.6% of an original TSV capacitance.

III. 3D POWER SUPPLY NOISE ANALYSIS WITH TSV VARIATION

In this work, we build a sign-off level 3D power supply noise analysis flow using existing 2D commercial tools and our own scripts. First, we extract RC parasitics of P/G net (SPEF) of each die separately using StarRC. We also model the coupling capacitance between top metal wires and the substrate of an adjacent die by performing capacitance extraction on 3D structures using Q3D extractor and scale capacitance values for these top metal P/G wires in SPEF file accordingly which is not supported by 2D parasitic extraction tools. Then, we use our in-house tool to merge P/G nets from multiple dies to build a single PDN and insert P/G TSV parasitics, which follow given normal distribution, between adjacent dies.

We also modify design and interconnect technology files for an individual die to create a unified 3D design. Next, we generate pseudorandom input vectors which obey a given switching activity. With 3D design files and input vectors, we obtain current wave form of all signal nets in the 3D design using NanoSim. Once these files are ready, we use PrimeRail to perform both static and dynamic noise analysis of 3D PDN. Due to the limitation on the number of layers these tools can process, we restrict our simulations to two-die stacked 3D ICs. Figure 3 shows the layout and power supply noise maps from our analysis flow.

TABLE II
BENCHMARK CIRCUITS

circuit	# gates	area (μm^2)	# signal TSVs	# P/G TSVs	% area by P/G TSVs	% area by decap
ind1	355K	810^2	1632	85	0.91	5.32
ind2	1.16M	1850^2	14957	613	1.26	5.32
ind3	2.52M	2822^2	22413	1405	1.24	5.32

TABLE III
IMPACT OF NUMBER OF VARIATION SOURCES.

circuit	# P/G TSVs	TSV R $\sim N(45.6,(0.3\times45.6)^2)$ (unit: $m\Omega$) TSV C $\sim N(35.5,(0.3\times35.5)^2)$ (unit: fF)			
		worst static noise (mV)		worst dynamic noise (mV)	
		mean	% σ/m	mean	% σ/m
ind1	85	10.562	0	133.055	0.00029
ind2	613	8.794	0	104.435	0
ind3	1405	9.234	0	121.042	0.00031

IV. EXPERIMENTAL RESULTS

We use three industrial circuits for our analysis. All circuits are designed with 45 nm technology to two-die stacked 3D ICs, which are listed in Table II. We use top two metal layers to construct regularly distributed power grid for each 2D tier and insert P/G TSV at each grid node shown in Figure 3(a). We deploy decaps uniformly across the die with 0.5 fF/um^2 density and worst dynamic noise is reduced by 53 mV for the circuit ind1 in a deterministic simulation, for example. We assume that P/G TSVs are connected directly to C4 bumps. The power to power pitch of TSV, C4 bump, and grid is 100 μm in all our designs. To model C4 bump and package impedance, we use 5 $m\Omega$ resistance, 500 pH inductance, and a parallel 30 fF capacitance for each C4 bump. We generate current wave forms using 500 MHz clock frequency with a switching activity of 0.2 for input

TABLE IV

IMPACT OF NUMBER OF P/G C4 BUMPS.

# bumps	TSV R $\sim N(45.6, (0.3 \times 45.6)^2)$ (unit: $m\Omega$) TSV C $\sim N(35.5, (0.3 \times 35.5)^2)$ (unit: fF)			
	worst static noise (mV)		worst dynamic noise (mV)	
	mean	% σ/m	mean	% σ/m
21	25.948	0.058	242.897	0.070
42	12.630	0.029	133.864	0.001
85	10.56	0	133.05	0.0002

TABLE V

IMPACT OF TSV SIZE. ASPECT RATIO IS 10 FOR ALL TSVS

TSV diameter (μm)	area (μm^2)	# P/G TSVs	TSV RC $\sim N(m, (0.3m)^2)$			
			worst static noise (mV)		worst dynamic noise (mV)	
			mean	% σ/m	mean	% σ/m
2.5	1610^2	421	11.762	0.00177	166.166	0
5	1850^2	613	8.794	0	104.435	0
10	2430^2	1005	10.193	0.00094	203.645	0.00122

signals. We use a TSV with 5 μm diameter, 50 μm height, and 120 nm thick oxide, unless specified. Finally, we perform more than 400 Monte Carlo power supply noise simulations for every case.

A. Impact of TSV RC Variation Range

In this section, we investigate the impact of TSV RC variation range on power supply noise in 3D PDN. We generate TSV RC parasitics which follow the normal distribution with standard deviation of 10, 20, or 30 % of a nominal value. Table I shows that for both static and dynamic noise case, there are negligible variations from mean values for given RC variation range. This is because TSV RC parasitic is much smaller compared with parasitics from 2D P/G grid, decaps, and C4 bumps, hence TSV RC parasitic variation does not affect the quality of 3D PDN.

B. Impact of Number of Variation Sources

Since TSV RC variation range shows negligible effect on power supply noise, we explore the impact of the number of variation sources, i.e. P/G TSV count, to see if increasing number of variation sources worsen the robustness of PDN. We keep P/G TSV pitch, C4 bump pitch, and P/G grid density same for all circuits to study the impact of P/G TSV count only. Table III shows that the number of variation sources poses negligible effects on power supply noise. This is again parasitics of P/G TSVs are much smaller than those of 2D P/G grid.

C. Impact of Number of C4 Bumps

It is known that P/G C4 bump pitch is a critical factor for 3D PDN quality. In this section, we vary the number of C4 bumps with fixed P/G TSV count and location to explore the its impact on power supply noise variation. We use ind1 circuit for this experiment. Table IV shows that both mean and standard deviation of power supply noise increase with decreasing number of bumps. This is because P/G TSVs that are directly connected to bumps carry more current than others, hence more susceptible to TSV RC variation. However, power supply noise variation is still negligible with different number of C4 bumps.

D. Impact of TSV Size

So far, we used TSV diameter of 5 μm for all experiments. In this section, we investigate the impact of TSV size on power supply noise variation. We use TSV diameter of 2.5, 5, and 10 μm with an aspect ratio of 10. We also redesign the circuit ind2 with different TSV size, since TSV size can affect layout quality significantly. Table V shows that increasing TSV size expands footprint area significantly and accommodates more P/G TSVs if we keep P/G TSV pitch same. Even though mean values of both static and dynamic noise change due to TSV size, variation of power supply noise is still negligible.

TABLE VI

IMPACT OF TSV PARASITICS. ASPECT RATIO IS 10 FOR ALL TSVS

TSV diameter (μm)	TSV RC $\sim N(m, (0.3m)^2)$ (unit: $m\Omega$, fF)			
	worst static noise (mV)		worst dynamic noise (mV)	
	mean	% σ/m	mean	% σ/m
2.5	8.794	0.00162	104.435	0
5	8.794	0	104.435	0
10	8.794	0.00052	104.435	0.00013

TABLE VII

IMPACT OF PARASITICS OF NANO-SCALE TSVS

TSV diameter (μm)	TSV RC variation range	worst static noise (mV)		worst dynamic noise (mV)	
		mean	% σ/m	mean	% σ/m
1	$\sigma = 0.1m$	10.562	0	133.053	0
	$\sigma = 0.2m$	10.562	0	133.053	0
	$\sigma = 0.3m$	10.562	0	133.053	0
0.5	$\sigma = 0.1m$	14.706	0.08822	154.170	0.07671
	$\sigma = 0.2m$	14.705	0.11981	154.163	0.10521
	$\sigma = 0.3m$	14.701	0.17602	154.124	0.15435
0.1	$\sigma = 0.1m$	157.872	0.24234	847.569	0.22812
	$\sigma = 0.2m$	157.877	0.32161	847.942	0.31513
	$\sigma = 0.3m$	157.877	0.43053	847.568	0.42943

To further study the impact of P/G TSV parasitics of different TSV size, now we only vary P/G TSV parasitics with the same layout of the ind2. In this case, only P/G TSV RC values change while parasitics of 2D P/G grid remain same. Table VI shows that P/G TSV parasitic change does not affect both mean and standard deviation. This is because nominal values of these TSV RC parasitics are already small, i.e. 21∼86 $m\Omega$ and 10∼132 fF, hence the effect of different P/G TSV parasitics on the 3D PDN is not noticeable.

It is natural that fabrication technology will enable TSV to scale down to increase TSV density. However, smaller TSV size might cause more problems in PDN due to increased TSV resistance and its variation. To evaluate the impact of TSV RC parasitics of future nano-scale TSVs, we perform power supply noise analysis with the circuit ind1. We keep TSV height 15 μm for all cases. Table VII shows that variation of power supply noise is still small compared with mean values, even though the magnitude of standard deviation increases. More serious problem is high noise level itself in nano-scale TSVs, not the variation in power supply noise.

V. CONCLUSIONS

In this work, we explore the effect of TSV RC variation on the robustness of two-die stacked 3D PDN under TSV RC variation. Our results show that TSV RC variations cause negligible influence on both static and dynamic noise in 3D PDN due to much smaller RC parasitic values of TSVs compared with that of entire PDN. This indicates that building robust 3D PDN under nominal condition is important.

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