Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling

Dae Hyun Kim, *Student Member, IEEE*, Saibal Mukhopadhyay, *Member, IEEE*, and Sung Kyu Lim, *Senior Member, IEEE*

***Abstract*—In this paper, we present analytical models for fast estimation of coupling capacitance of square-shaped through-silicon vias (TSVs) in three-dimensional integrated circuits (3D ICs). Errors between our model and Synopsys Raphael simulation on regular TSV structures remain less than 6.03% while the computation time of our model for capacitance estimation is negligible. We also develop a simple capacitance estimation technique to extract TSV-to-TSV coupling capacitance in general layouts. Average errors between our model and Raphael simulation on random TSV structures is 5.06%–8.24%, and maximum errors remain less than 18.91% which is tolerable for fast capacitance estimation in computer-aided design area.**

***Index Terms*—Capacitance, through-silicon via (TSV), timing analysis, three-dimensional integrated circuits (3D IC).**

I. Introduction

DRIVEN by the need for performance improvement, a large number of universities and companies are actively researching 3D IC, which is expected to lead to shorter total wirelength, higher clock frequency, and lower power consumption than 2D IC [1]–[3]. In 3D IC, multiple dies are stacked, and vertical interconnections between dies are realized by through-silicon vias (TSVs). These TSVs play a central role in replacing long interconnects found in 2D ICs with short vertical interconnects. Shortened wires will result in low wire delay, thereby improving performance. In addition to performance improvement, it is also possible with 3D heterogeneous integration to stack disparate technologies to provide a 3D structure with heterogeneous functions including logic, memory, MEMS, antennas, display, RF, analog/digital, sensors, and power conversion and storage. Therefore, universities and companies have been actively developing TSV manufacturing and die-to-die bonding technologies [4]–[9]. Moreover, various works on utilizing TSVs for physical design have also been proposed recently [10], [11].

Manuscript received June 22, 2010; revised October 08, 2010; accepted November 08, 2010. Date of publication January 20, 2011; date of current version March 23, 2011. This research is based upon the work supported by the National Science Foundation under CAREER Grant CCF-0546382 and CCF-0917000; the SRC Interconnect Focus Center (IFC), and Intel Corporation. This work was recommended for publication by Associate Editor J. Kim upon evaluation of the reviewers comments.

The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA.

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Digital Object Identifier 10.1109/TCPMT.2010.2101910

The basic electrical characteristics of TSVs such as resistance, capacitance, and inductance have also been investigated in the literature to provide circuit designers with physical analysis and ranges of their values [12]–[16]. One of the results to notice is that TSV coupling capacitance is very big (tens of femto-farads) [13] so that it has huge impact on timing and interconnect power [17], [18]. Therefore, computer-aided design (CAD) tools are required to compute TSV coupling capacitance quickly but accurately during placement, routing, and optimization of timing and power in 3D ICs.

TSV-to-TSV (or TSV-to-wire) coupling capacitance is affected by TSV-to-TSV (or TSV-to-wire) distance, TSV and wire dimensions, the number of surrounding TSVs and wires, and their spatial distribution. It is therefore almost impossible to use lookup tables to compute TSV capacitance quickly because too many variables exist. In addition, it is also almost impossible to use field solvers for TSV capacitance computation during placement, routing, or optimization of timing and power because field solvers require nonnegligible amount of computation time.

In this paper, we present an accurate analytical model for the coupling capacitance among square-shaped TSVs and wires. In order to model layouts accurately, we consider various types of coupling and fringe capacitances while taking neighboring TSVs and wires into account. Our experiments show that errors between our model and Synopsys Raphael simulation remain less than 6.03% on regular TSV structures, and average errors on random TSV structures remain less than 5.06%–8.24% while our model requires a fraction of runtime for capacitance computation.

This paper is organized as follows. In Section II, we briefly discuss device structures in 3D ICs and review TSV coupling models. Section III shows basic formulas for capacitance computation. In Sections IV and V, we present our analytical models for fast estimation of TSV coupling capacitance. Capacitance estimation results on regular TSV structures and the impact of TSV capacitance on signal delay are presented in Section VI. We compare capacitances obtained from our model and Raphael simulation on random TSV structures in Section VII, and conclude in Section VIII.

II. Device Structure

A. TSV Formation and Die Bonding

Fig. 1 shows three types of die bonding and two types of TSVs. Under the via-first technology, devices and TSVs are fabricated first, metal layers are deposited, and then dies are bonded. Therefore, TSVs in via-first technology are surrounded

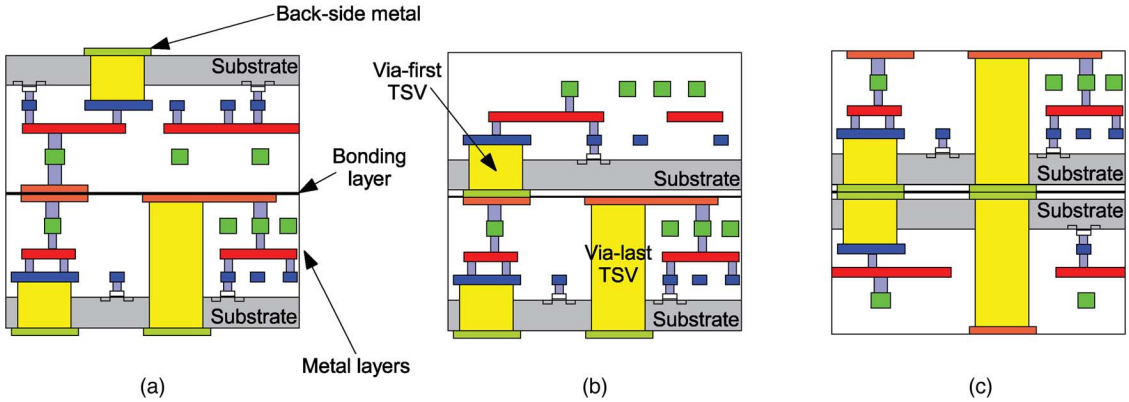

Fig. 1. Three types of die bonding (face-to-face, face-to-back, and back-to-back) and two types of TSVs (via-first and via-last). (a) Face-to-face. (b) Face-to-back. (c) Back-to-back.

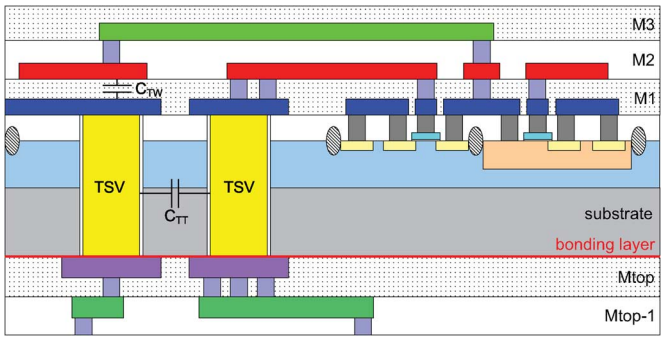

Fig. 2. Capacitive coupling in via-first TSV technology.

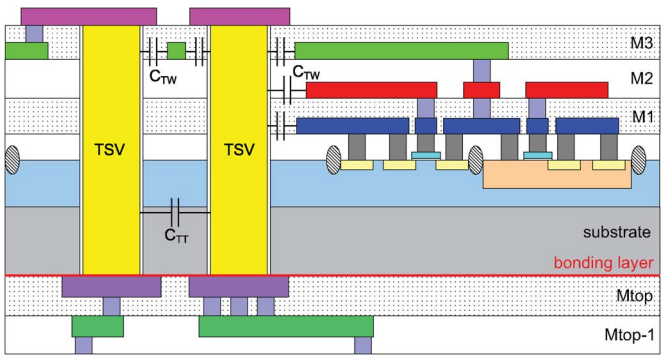

Fig. 3. Capacitive coupling in via-last TSV technology.

by other TSVs laterally and by wires vertically. In via-last technology, on the other hand, devices and metal layers are fabricated first, TSVs are fabricated through all the layers from the substrate to the topmost metal layer, and then dies are bonded. Therefore, TSVs in via-last technology are surrounded by other TSVs laterally and by wires laterally and vertically.

B. TSV Coupling Capacitance

TSV coupling capacitance consists mainly of two components as follows.

- Capacitive coupling (C_{TW} in Figs. 2 and 3) between a TSV and wires surrounding the TSV. These wires exist on the top or bottom of TSVs in via-first case as shown in Fig. 2. In case of via-last TSVs, there exists capacitive coupling between a TSV and neighboring wires in metal layers as shown in Fig. 3.
- Capacitive coupling (C_{TT} in Figs. 2 and 3) between two TSVs.

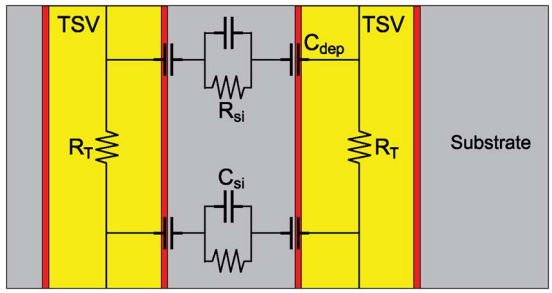

Fig. 4. TSV RC model.

To analyze physical phenomena between two TSVs in the substrate, we review previous models presented in the literature. Fig. 4 shows a TSV RC model presented in [15] and [19].[1] In the model, two TSVs are connected by a series connection of C_{dep}, a parallel connection of C_{si} and R_{si}, and C_{dep}. The impedance of the parallel connection of C_{si} and R_{si} is as follows:

$$Z_{\mathrm{si}} = \frac{R_{\mathrm{si}}}{1 + jwR_{\mathrm{si}}C_{\mathrm{si}}} \tag{1}$$

where C_{si} and R_{si} are capacitance and resistance of the silicon substrate respectively. If the substrate is pure silicon substrate or high-resistivity substrate (HRS) so that R_{si} is high, Z_{si} in (1) is determined primarily by C_{si}. In this case, we can simplify this model by removing R_{si}. The simplified model is shown in Fig. 5 which is our interest in this paper.[2]

In this simplified model, we also ignore the liner capacitance between a TSV and the silison substrate. The reason is because we assume that the liner is very thin so that the liner capacitance is very high compared to the TSV-to-TSV coupling capacitance, and we focus on high frequency ranges. If more accurate models

[1]We simplify the model by ignoring TSV inductance.

[2]If the substrate resistivity is low, we should not ignore substrate resistance in (1) but this case is beyond the scope of this paper.

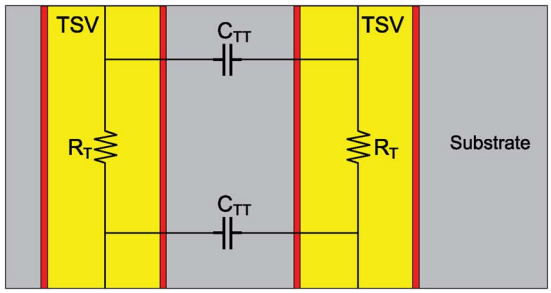

Fig. 5. Simplified TSV RC model.

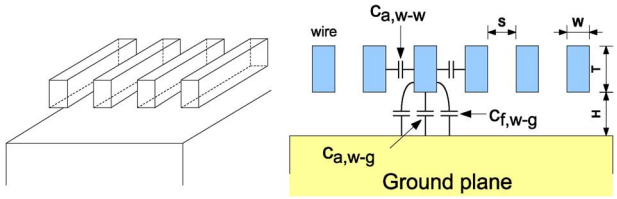

Fig. 6. Capacitance of multiple wires on ground plane.

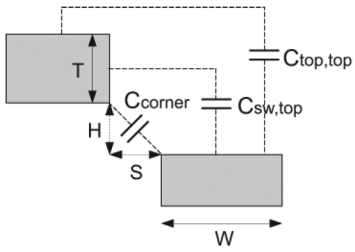

Fig. 7. Various fringe capacitances.

are required, we can compute and include the liner capacitance by capacitance formulas presented in [16].

III. Basic Formulas for Capacitance Computation

Our approach is to first figure out various capacitive components among TSVs and wires, and then derive analytical equations to compute each capacitance. In this section, we review existing capacitance formulas to handle various capacitive components between TSVs and wires.

A. Multiple Wires on Ground Plane

In 3D IC layouts, multiple wires go over a TSV which can be considered as a ground plane. Therefore, we first review capacitance formulas for multiple wires laid on a ground plane.

Fig. 6 shows the side view of wires and a ground plane, and [20] shows capacitance formulas for multiple wires on a ground plane as follows:

$$c_{\mathrm{a,w-g}} = \varepsilon_{\mathrm{di}} \cdot 1.15 \left(\frac{W}{H}\right) \tag{2}$$

$$c_{\mathrm{f,w-g}} = \varepsilon_{\mathrm{di}} \cdot 2.80 \left(\frac{T}{H}\right)^{0.222} \tag{3}$$

$$c_{\mathrm{w-g}} = c_{\mathrm{a,w-g}} + 2 \cdot c_{\mathrm{f,w-g}} \tag{4}$$

$$C_{\mathrm{w-g}} = L_{\mathrm{wire}} \cdot c_{\mathrm{wire}} \tag{5}$$

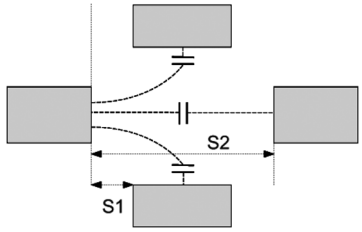

Fig. 8. Fringe capacitances when surrounding wires exist.

where W is the wire width, T is the wire thickness, H is the spacing between a wire and the ground plane, $c_{\mathrm{a,w-g}}$ is the area capacitance[3] per unit length between the bottom surface of the wire and the top surface of the ground plane, $c_{\mathrm{f,w-g}}$ is the fringe capacitance per unit length between a sidewall of the wire and the top surface of the ground plane, and $\varepsilon_{\mathrm{di}}$ is the dielectric constant of the dielectric material. $c_{\mathrm{w-g}}$, the coupling capacitance per unit length between a wire and the ground plane, is the sum of one area capacitance and two fringe capacitances as shown in Fig. 6. $C_{\mathrm{w-g}}$ is the final total coupling capacitance between a wire and the ground plane when multiple wires exist.

B. Fringe Capacitance

Formulas of fringe capacitances between two wires are presented in [21] and we repeat the geometry and formulas in Fig. 7 and

$$c_{\mathrm{sw,top}} = \frac{\varepsilon_{\mathrm{di}}}{\pi/2} \cdot \ln\left[\frac{H+\eta T+\sqrt{S^2+(\eta T)^2+2H\eta T}}{S+H}\right] \tag{6}$$

$$c_{\mathrm{top,top}} = \frac{\varepsilon_{\mathrm{di}} W\alpha\left(\ln\left[1+\frac{2W}{S}\right]+e^{\left(-\frac{S+T}{3S}\right)}\right)}{W\pi\alpha+(H+T)\left(\ln\left[1+\frac{2W}{S}\right]+e^{\left(-\frac{S+T}{3S}\right)}\right)} \tag{7}$$

$$c_{\mathrm{corner}} = \frac{\varepsilon_{\mathrm{di}}}{\pi}\sqrt{\frac{HS}{H^2+S^2}} \tag{8}$$

$$\eta = \exp\left[(W+S-\sqrt{S^2+T^2+2HT})/(\tau W)\right]$$

$$\alpha = \exp\left[-(H+T)/(S+W)\right] \tag{9}$$

$$\eta_0 = \exp\left[-\frac{\sqrt{S_1^2+\left(H+\frac{1}{2}T\right)^2}+S_1}{2S_2}+\frac{1}{5}\right] \tag{10}$$

where W is the metal width, T is the metal thickness, H is the vertical spacing, and S is the horizontal spacing. $c_{\mathrm{sw,top}}$ is the capacitance per unit length between the sidewall of the upper wire and the top surface of the lower wire. $c_{\mathrm{top,top}}$ is the capacitance per unit length between the top surfaces of the upper and lower wire. c_{corner} is the capacitance per unit length between the two corners. If there are surrounding wires as shown in Fig. 8, it is necessary to multiply $c_{\mathrm{sw,top}}$ by η_0 shown in (10) to account for new distribution of electric field [21].

[3]Area capacitance is the capacitance between two parallel plates.

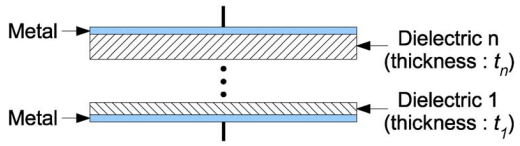

Fig. 9. Multiple dielectric materials in a parallel plate capacitor.

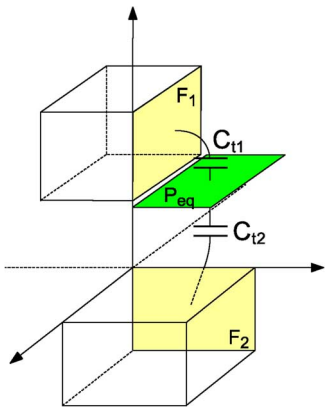

Fig. 10. Capacitance between two surfaces.

C. Multiple Dielectric Materials

When multiple dielectric materials exist between two parallel plates as shown in Fig. 9, its capacitance is computed by the following equation:

$$C = \varepsilon_0 \cdot \varepsilon_{\text{new}} \cdot \frac{S}{\sum_{i=1}^{n} t_i} \tag{11}$$

$$\varepsilon_{\text{new}} = \left(\sum_{i=1}^{n} t_i\right) \cdot \left(\sum_{j=1}^{n} \frac{t_j}{\varepsilon_{r,j}}\right)^{-1} \tag{12}$$

where ε_0 is the vacuum permittivity, ε_{new} is the relative permittivity of the parallel plate capacitor, S is the area of the parallel plate, n is the number of dielectric layers, t_i is the thickness of ith dielectric layer, and $\varepsilon_{r,j}$ is the dielectric constant of jth dielectric layer [22].

D. Capacitance Between Two Surfaces

$c_{\text{sw,top}}$ in (6) is valid when two wires are in the geometric relation shown in Fig. 7. If two surfaces are not in this geometric relation, however, we should not apply $c_{\text{sw,top}}$ directly to compute the coupling capacitance of the two surfaces. Fig. 10 shows an example where the geometric relation between the two surfaces F1 and F2 is different from the geometric relation in Fig. 7.

In this case, we use a simple approximation technique as follows. First, we find a flat equipotential plane between the two metal surfaces. Then we compute the coupling capacitance between a metal surface and the equipotential plane (C_{t1} and C_{t2} in the figure). Finally the coupling capacitance between the two metal surfaces is computed by the series connection of the two coupling capacitances. In Fig. 10, for example, we compute the coupling capacitance between two metal surfaces F_1 and F_2 by assuming the equipotential plane P_{eq} and computing C_{t1} and C_{t2} using $c_{\text{sw,top}}$. The final coupling capacitance between F_1 and F_2 is the capacitance of the series connection of C_{t1} and C_{t2}.

We generate several geometries, apply this technique, and compare results against Raphael simulation in order to validate this approximation technique. The error is around 10% but this is tolerable because absolute values of this kind of fringe capacitance are much smaller than TSV-to-TSV coupling capacitance or TSV-to-wire area capacitance.

IV. TSVs With Top and Bottom Neighbors

One of major challenges in the computation of TSV-related capacitances is in identifying different capacitive components. In this section, we identify all the capacitive components in a regular TSV structure in which a TSV is surrounded by eight other TSVs and top (and bottom) wires as shown in Fig. 11(a). Table I shows variables and constants used in this paper.

A. Modeling $C_{\text{top,1}}$

$C_{\text{top,1}}$ is the capacitance between the top surface of a TSV and the wires on top of the TSV as shown in Fig. 11(b). Table II shows the variable settings for $C_{\text{area,1}}$ and $C_{\text{fr,1}}$. $C_{\text{top,1}}$ is computed as follows:

$$\begin{aligned} C_{\text{area,1}} &= c_{\text{area,1}} \cdot W_{\text{TSV}} \\ C_{\text{fr,1}} &= c_{\text{fr,1}} \cdot W_{\text{TSV}} \\ C_{\text{top,1}} &= N_{\text{w}} \cdot (C_{\text{area,1}} + 2C_{\text{fr,1}}) \end{aligned} \tag{13}$$

where $C_{\text{area,1}}$ is the coupling capacitance between the bottom surface of the wires and the top surface of the TSV, $C_{\text{fr,1}}$ is the coupling capacitance between the sidewalls of wires and the top surface of the TSV. $c_{\text{area,1}}$ is computed by plugging W_{w}, S_{w}, and H_{w} into W, S, and H, respectively, in (2), and plugging $S_{\text{w}}/2$, 0,T_{w}, H_{w}, 0, and S_{w} into W, S, T, H, S_1, and S_2, respectively, in (6) and (10). Table II shows these substitution settings.

B. Modeling $C_{\text{top,2}}$

$C_{\text{top,2}}$ is the capacitance between a sidewall of the TSV and the outside wire pieces which are actually connected to wires on top of the TSV as shown in Fig. 11(c). $L_{\text{fr,1}}$ is determined empirically, and Table II shows the variable settings for $C_{\text{fr,2}}$ and $C_{\text{fr,3}}$. $C_{\text{top,2}}$ is computed as follows:

$$\begin{aligned} C_{\text{fr,2}} &= c_{\text{fr,2}} \cdot W_{\text{w}} \\ C_{\text{s1}} &= c_{\text{s1}} \cdot \frac{S_{\text{TSV}}}{2}, \quad C_{\text{s2}} = c_{\text{s2}} \cdot \frac{S_{\text{w}}}{2}, \quad C_{\text{fr,3}} = C_{\text{s1}} // C_{\text{s2}} \\ C_{\text{top,2}} &= N_{\text{w}} \cdot [C_{\text{fr,2}} + 2 \cdot C_{\text{fr,3}}] \end{aligned} \tag{14}$$

where $C_{\text{fr,2}}$ is the coupling capacitance between the bottom side of a wire and a sidewall of the TSV, and $C_{\text{fr,3}}$ is the coupling capacitance between sidewalls of wires and a sidewall of the TSV.

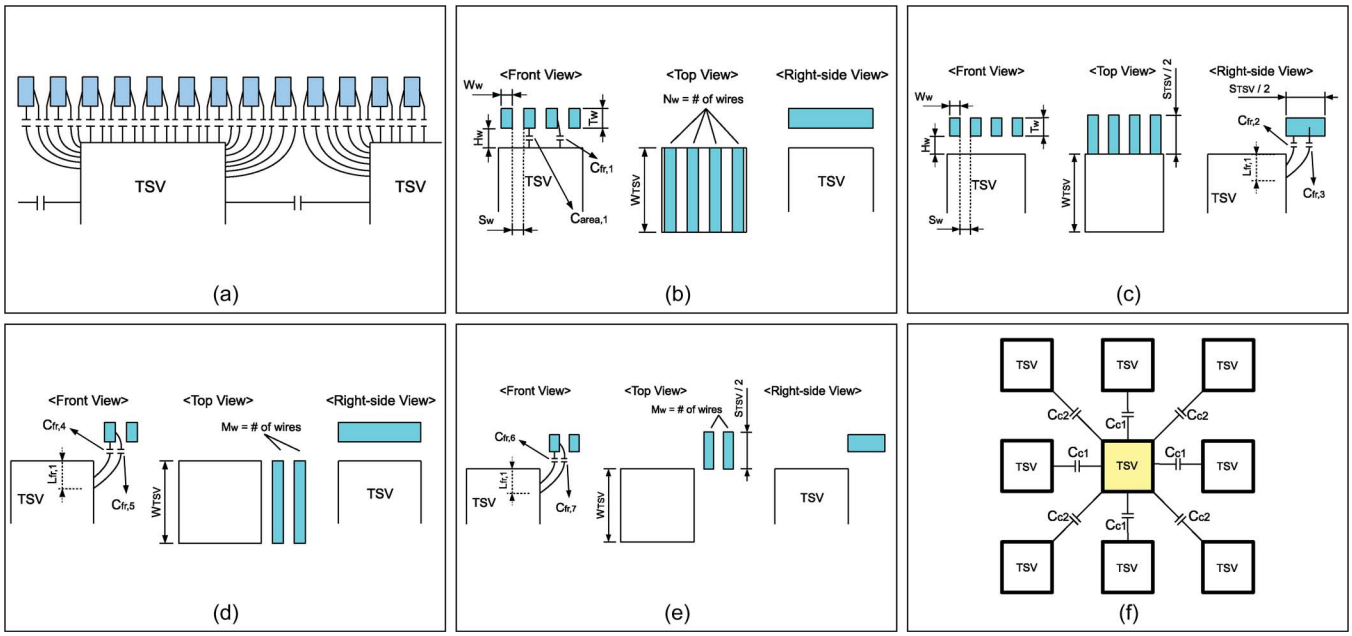

Fig. 11. Capacitive components of TSVs with top and bottom neighboring wires.

TABLE I
VARIABLES AND CONSTANTS USED IN CAPACITANCE EXTRACTION

W_{TSV}	TSV width (assuming TSVs are square-shaped)
H_{TSV}	TSV height (length in z-direction)
S_{TSV}	spacing between two TSVs
W_{w}	metal wire width
S_{w}	spacing between two parallel metal wires
T_{w}	metal wire thickness
H_{w}	spacing in z-direction between two adjacent metal layers
N_{w}	the number of wires on top (or bottom) of a TSV ($=\frac{W_{\mathrm{TSV}}}{W_{\mathrm{w}}+S_{\mathrm{w}}}$)
M_{w}	a half the number of wires between two TSVs ($=\frac{S_{\mathrm{TSV}}}{2(W_{\mathrm{w}}+S_{\mathrm{w}})}$)
$L_{\mathrm{fr},1}$	effective length affecting fringe capacitance of a TSV ($=0.4\cdot\frac{S_{\mathrm{TSV}}}{2}$) (see Fig. 11 (c), (d), (e))
$L_{\mathrm{fr},2}$	effective length affecting fringe capacitance of a TSV ($=0.4\cdot\frac{S_{\mathrm{TSV}}-2\cdot S_{\min}}{2}$) (see Fig. 12 (d), (e))
$S_{\min}$	minimum spacing between a metal wire and a TSV (see Fig. 12 (d), (e))
M'_{w}	$=\frac{S_{\mathrm{TSV}}-2\cdot S_{\min}}{2(W_{\mathrm{w}}+S_{\mathrm{w}})}$ (see Fig. 12 (e))
H_{INT}	height of interconnect layers between TSVs (see Fig. 12 (a))
W_{mis}	$=W_{\mathrm{TSV}}\cdot$ misalignment ratio. (see Fig. 12 (f))

C. Modeling $C_{\mathrm{side},1}$

$C_{\mathrm{side},1}$ is the capacitance between a sidewall of the TSV and side wires as shown in Fig. 11(d). Table II shows the variable settings for $C_{\mathrm{side},1}$. $C_{\mathrm{side},1}$ is computed as follows:

$$\begin{aligned} C_{\mathrm{fr},4}(m) &= c_{\mathrm{fr},4}(m)\cdot W_{\mathrm{TSV}} \\ C_{\mathrm{fr},5}(m) &= c_{\mathrm{fr},5}(m)\cdot W_{\mathrm{TSV}} \\ C_{\mathrm{side},1} &= \sum_{m=1}^{M_{\mathrm{w}}}\left(C_{\mathrm{fr},4}(m)+2\cdot C_{\mathrm{fr},5}(m)\right) \end{aligned} \tag{15}$$

where $C_{\mathrm{r},4}(m)$ is the coupling capacitance between the bottom side of the mth wire and the facing wall of the TSV, and $C_{\mathrm{fr},5}(m)$ is the coupling capacitance between the sidewalls of the mth wire and the facing wall of the TSV.

D. Modeling $C_{\mathrm{side},2}$

$C_{\mathrm{side},2}$ is the capacitance between a sidewall of the TSV and side wires in nonoverlapped regions as shown in Fig. 11(e). Table II shows the variable settings for $C_{\mathrm{side},2}$. $C_{\mathrm{side},2}$ is computed as follows:

$$\begin{aligned} C_{\mathrm{s3}} &= c_{\mathrm{s3}}\cdot W_{\mathrm{w}}, \quad C_{\mathrm{s4}}(m) = c_{\mathrm{s4}}(m)\cdot\frac{S_{\mathrm{TSV}}}{2} \\ C_{\mathrm{fr},6}(m) &= C_{\mathrm{s3}}//C_{\mathrm{s4}(m)} \\ C_{\mathrm{s5}} &= c_{\mathrm{s5}}\cdot\frac{S_{\mathrm{TSV}}}{2}, \quad C_{\mathrm{s6}} = c_{\mathrm{s6}}\cdot S_{\mathrm{w}} \\ C_{\mathrm{s7}}(m) &= c_{\mathrm{s7}}(m)\cdot\frac{S_{\mathrm{TSV}}}{2} \\ C_{\mathrm{fr},7}(m) &= C_{\mathrm{s5}}//C_{\mathrm{s6}}//C_{\mathrm{s7}}(m) \\ C_{\mathrm{side},2} &= \sum_{m=1}^{M_{\mathrm{w}}}\left[C_{\mathrm{fr},6}(m)+2\cdot C_{\mathrm{fr},7}(m)\right] \end{aligned} \tag{16}$$

where $C_{\mathrm{fr},6}(m)$ is the coupling capacitance between the bottom side of the mth wire and the facing sidewall of the TSV, and $C_{\mathrm{fr},7}(m)$ is the coupling capacitance between sidewalls of the mth wire and the facing sidewall of the TSV.

E. Modeling C_{TT}

As mentioned in Section II, there exists capacitive coupling between two adjacent TSVs. This coupling capacitance C_{TT} between two TSVs consists of two components. The first component is the coupling capacitance [C_{c1} in Fig. 11(f)] between the sidewalls of the TSVs, and the second component is the coupling capacitance (C_{c2} in Fig. 11(f)) between the corners of the TSVs. C_{c1} is computed as follows:

$$C_{\mathrm{c1}} = \varepsilon_{\mathrm{di}}\frac{(H_{\mathrm{TSV}}-2\cdot L_{\mathrm{fr},1})\cdot W_{\mathrm{TSV}}}{S_{\mathrm{TSV}}} \tag{17}$$

c_{corner} in (8) which will be used for the computation of C_{c2} is dependent on S/H. If H and S are constants, c_{corner} also

TABLE II
VARIABLE SETTINGS. C.F. MEANS "CAPACITANCE FUNCTION." SERIES MEANS THE COMPONENTS ARE CONNECTED IN SERIES (E.G., $c_{\mathrm{fr},3}$ IS COMPUTED BY THE SERIES CONNECTION OF $c_{\mathrm{s}1}$ AND $c_{\mathrm{s}2}$)

		Series	C.F.	W	S	T	H	S_1	S_2
$C_{\mathrm{top},1}$	$c_{\mathrm{area},1}$		$c_{\mathrm{a,w-g}}$	W_{w}	-	-	H_{w}	-	-
	$c_{\mathrm{fr},1}$		$c_{\mathrm{f,w-g}}$	-	-	T_{w}	H_{w}	-	-
$C_{\mathrm{top},2}$	$c_{\mathrm{fr},2}$		$c_{\mathrm{sw,top}}$	$L_{\mathrm{fr},1}$	H_{w}	$\frac{S_{\mathrm{TSV}}}{2}$	0	-	-
	$c_{\mathrm{fr},3}$	$c_{\mathrm{s}1}$	$c_{\mathrm{sw,top}}$	$\frac{S_{\mathrm{w}}}{2}$	0	T_{w}	$\frac{H_{\mathrm{w}}}{2}$	0	S_{w}
		$c_{\mathrm{s}2}$	$c_{\mathrm{sw,top}}$	$L_{\mathrm{fr},1}$	$\frac{H_{\mathrm{w}}}{2}$	$\frac{S_{\mathrm{TSV}}}{2}$	0	-	-
$C_{\mathrm{side},1}$	$c_{\mathrm{fr},4}(m)$		$c_{\mathrm{sw,top}}$	$\frac{L_{\mathrm{fr},1}}{2\cdot M_{\mathrm{w}}}$	$H_{\mathrm{w}}+(2m-1)\frac{L_{\mathrm{fr},1}}{2\cdot M_{\mathrm{w}}}$	W_{w}	$m\cdot S_{\mathrm{w}}+(m-1)W_{\mathrm{w}}$	-	-
	$c_{\mathrm{fr},5}(m)$		$c_{\mathrm{top,top}}$	$\frac{L_{\mathrm{fr},1}}{4\cdot M_{\mathrm{w}}}$	$H_{\mathrm{w}}+m\frac{L_{\mathrm{fr},1}}{M_{\mathrm{w}}}$	W_{w}	$m\cdot S_{\mathrm{w}}+(m-1)W_{\mathrm{w}}$	-	-
$C_{\mathrm{side},2}$	$c_{\mathrm{fr},6}(m)$	$c_{\mathrm{s}3}$	$c_{\mathrm{sw,top}}$	$\frac{S_{\mathrm{TSV}}}{2}$	H_{w}	$\frac{S_{\mathrm{TSV}}}{2}$	0	-	-
		$c_{\mathrm{s}4}(m)$	$c_{\mathrm{sw,top}}$	$\frac{L_{\mathrm{fr},1}}{2\cdot M_{\mathrm{w}}}$	$S_{\mathrm{w}}+(2m-1)\frac{L_{\mathrm{fr},1}}{2\cdot M_{\mathrm{w}}}$	W_{w}	$m\cdot S_{\mathrm{w}}+(m-1)W_{\mathrm{w}}$	-	-
	$c_{\mathrm{fr},7}(m)$	$c_{\mathrm{s}5}$	$c_{\mathrm{sw,top}}$	$\frac{S_{\mathrm{w}}}{2}$	0	T_{w}	H_{w}	0	S_{w}
		$c_{\mathrm{s}6}$	$c_{\mathrm{sw,top}}$	$\frac{S_{\mathrm{TSV}}}{2}$	H_{w}	$\frac{S_{\mathrm{TSV}}}{2}$	0	-	-
		$c_{\mathrm{s}7}$	$c_{\mathrm{sw,top}}$	$\frac{L_{\mathrm{fr},1}}{2\cdot M_{\mathrm{w}}}$	$S_{\mathrm{w}}+(2m-1)\frac{L_{\mathrm{fr},1}}{2\cdot M_{\mathrm{w}}}$	S_{w}	$m\cdot S_{\mathrm{w}}+(m-1)W_{\mathrm{w}}$	-	-
$C_{\mathrm{side},3}$	$c_{\mathrm{area},2}$		$c_{\mathrm{a,w-g}}$	W_{w}	-	-	S_{min}	-	-
	$c_{\mathrm{sw},1}$		$c_{\mathrm{sw,top}}$	$\frac{S_{\mathrm{w}}}{2}$	0	$\frac{S_{\mathrm{w}}}{2}$	S_{min}	0	S_{w}
	$c_{\mathrm{sw},2}$		$c_{\mathrm{sw,top}}$	$\frac{H_{\mathrm{w}}}{2}$	0	W_{w}	S_{min}	0	H_{w}
$C_{\mathrm{side},4}$	$c_{\mathrm{area},3}$		$c_{\mathrm{a,w-g}}$	T_{w}	-	-	S_{min}	-	-
	$c_{\mathrm{sw},3}$		$c_{\mathrm{sw,top}}$	$\frac{H_{\mathrm{w}}}{2}$	0	W_{w}	S_{min}	0	H_{w}
$C_{\mathrm{side},5}$	$c_{\mathrm{sw},4}$		$c_{\mathrm{sw,top}}$	$L_{\mathrm{fr},2}$	0	$\frac{S_{\mathrm{TSV}}-2S_{\mathrm{min}}}{2}$	S_{min}	-	-
$C_{\mathrm{side},6}$	$c_{\mathrm{sw},5}(m)$		$c_{\mathrm{sw,top}}$	$\frac{L_{\mathrm{fr},2}}{2M'_{\mathrm{w}}}$	$\frac{(2m-1)L_{\mathrm{fr},2}}{2M'_{\mathrm{w}}}$	W_{w}	$S_{\mathrm{min}}+(m-1)W_{\mathrm{w}}+(m-1)S_{\mathrm{w}}$	-	-
	$c_{\mathrm{sw},6}(m)$		$c_{\mathrm{top,top}}$	$\frac{L_{\mathrm{fr},2}}{4M'_{\mathrm{w}}}$	$m\frac{L_{\mathrm{fr},2}}{M'_{\mathrm{w}}}$	W_{w}	$S_{\mathrm{min}}+m\cdot W_{\mathrm{w}}+(m-1)S_{\mathrm{w}}$	-	-
C_{m2}			$c_{\mathrm{sw,top}}$	W_{mis}	S_{TSV}-W_{mis}	W_{mis}	0	-	-

becomes a constant. In our case, however, the width, height, and spacing of TSVs vary in a wide range. Therefore, we find a proportional constant K_{corner} empirically and compute C_{c2} as follows:

$$C_{\mathrm{c2}} = \frac{\varepsilon_{\mathrm{di}}}{\pi\sqrt{2}} \cdot H_{\mathrm{TSV}} \cdot K_{\mathrm{corner}} \tag{18}$$

$$K_{\mathrm{corner}} = \frac{1}{2} \cdot \frac{H_{\mathrm{TSV}}}{S_{\mathrm{TSV}}} \quad \left(\text{if} \quad \frac{H_{\mathrm{TSV}}}{S_{\mathrm{TSV}}} \leq 4.0\right)$$
$$= 2.0 \quad \left(\text{if} \quad \frac{H_{\mathrm{TSV}}}{S_{\mathrm{TSV}}} \geq 4.0\right). \tag{19}$$

Lastly, C_{TT} is computed by the following equation:

$$C_{\mathrm{TT}} = 4(C_{\mathrm{c1}} + C_{\mathrm{c2}}). \tag{20}$$

F. Impact of TSV Liner

It is required to consider multiple dielectric materials when we compute TSV-to-wire fringe capacitance or TSV-to-TSV coupling capacitance because there exist multiple dielectric materials between two conductors. In this case, we use the capacitance formula shown in (12) to take multiple dielectrics into account. In our simulation, we neglect the impact of TSV liner because we assume that TSV liner is very thin (approximately 0.1 μm) compared to TSV-to-wire or TSV-to-TSV distance, thus $\varepsilon_{\mathrm{new}}$ in (12) is dominated mainly by ILD and substrate. If TSV liner thickness is not negligible, however, we need to use (12) and should consider multiple dielectric materials.

G. Metal Wires Connected to TSVs

If a metal wire on top of a TSV is connected to the TSV in Fig. 11(a), we need to subtract the coupling capacitance between the wire and the TSV from the TSV capacitance. In this case, however, we also need to add wire-to-wire coupling capacitances ($c_{\mathrm{a,w-w}}$) shown in Fig. 6 to the TSV capacitance. The wire-to-wire coupling capacitance is computed by the following formula [20]:

$$c_{\mathrm{a,w-w}} = \varepsilon_{\mathrm{di}} \cdot \left(0.03\left(\frac{W}{H}\right) + 0.83\left(\frac{T}{H}\right) - 0.07\left(\frac{T}{H}\right)^{0.222}\right)\left(\frac{S}{H}\right)^{-1.34} \tag{21}$$

where W is the wire width, T is the wire thickness, H is the spacing between a wire and the ground plane, and S is the spacing between two adjacent wires.

V. TSVs WITH TOP, BOTTOM, AND SIDE NEIGHBORS

Fig. 12(a) shows capacitance components when a TSV is surrounded by neighboring wires vertically and laterally. We again assume a regular TSV structure in which one TSV is surrounded by eight neighboring TSVs and metal wires go over and between the TSVs.

A. Modeling $C_{\mathrm{side},3}$

$C_{\mathrm{side},3}$ consists of three components $C_{\mathrm{area},2}$, $C_{\mathrm{sw},1}$, and $C_{\mathrm{sw},2}$ as shown in Fig. 12(b). Table II shows the variable settings for these three components. $C_{\mathrm{side},3}$ is computed as follows:

$$C_{\mathrm{area},2} = c_{\mathrm{area},2} \cdot T_{\mathrm{w}}$$
$$C_{\mathrm{sw},1} = c_{\mathrm{sw},1} \cdot T_{\mathrm{w}}, \quad C_{\mathrm{sw},2} = c_{\mathrm{sw},2} \cdot W_{\mathrm{w}}$$
$$C_{\mathrm{side},3} = N_{\mathrm{w}} \cdot (C_{\mathrm{area},2} + 2 \cdot C_{\mathrm{sw},1} + 2 \cdot C_{\mathrm{sw},2}) \tag{22}$$

where $C_{\mathrm{area},2}$ is the coupling capacitance between facing sidewalls of a wire and the TSV, and $C_{\mathrm{sw},1}$ and $C_{\mathrm{sw},2}$ are the cou-

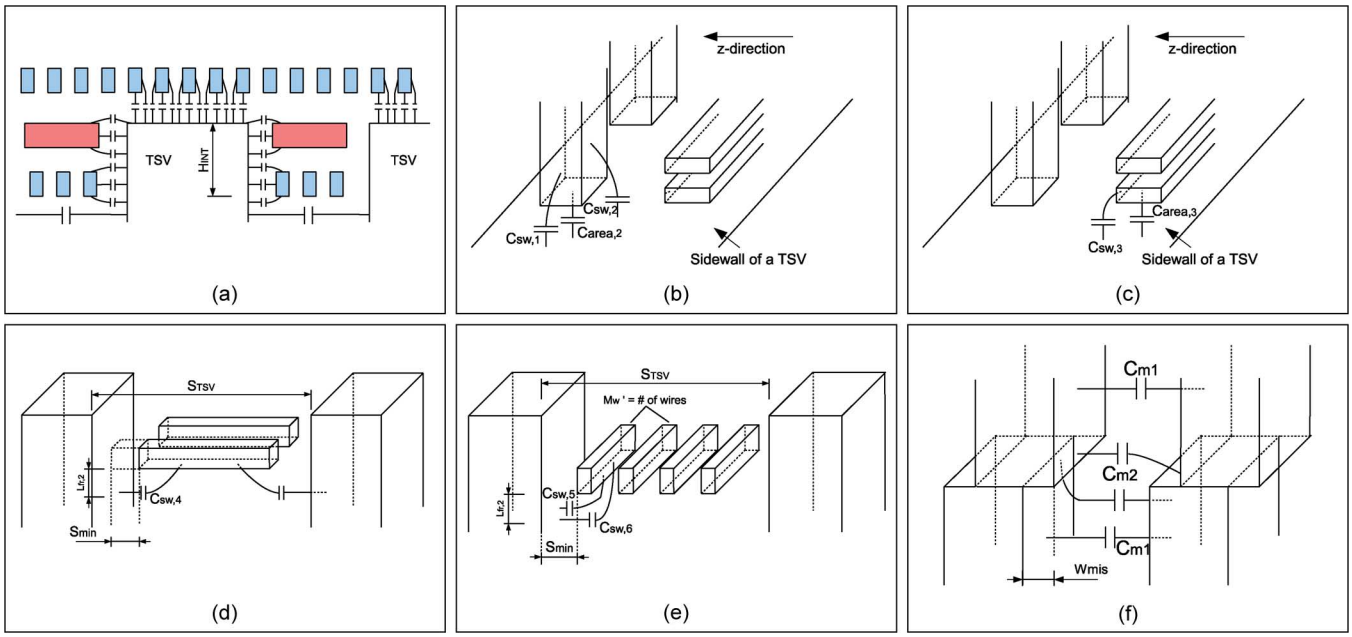

Fig. 12. Capacitive components of TSVs with top, bottom, and side neighboring wires.

pling capacitances between a sidewall of a wire and the facing sidewall of the TSV.

B. Modeling $C_{\text{side},4}$

$C_{\text{side},4}$ consists of two components $C_{\text{area},3}$ and $C_{\text{sw},3}$ as shown in Fig. 12(c). Table II shows the variable setting for these two components. $C_{\text{side},4}$ is computed as follows:

$$\begin{aligned} C_{\text{area},3} &= c_{\text{area},3} \cdot W_{\text{TSV}} \\ C_{\text{sw},3} &= c_{\text{sw},3} \cdot W_{\text{TSV}} \\ C_{\text{side},4} &= C_{\text{area},3} + 2 \cdot C_{\text{sw},3} \end{aligned} \tag{23}$$

where $C_{\text{area},3}$ is the coupling capacitance between a sidewall of a wire and the facing sidewall of the TSV, and $C_{\text{sw},3}$ is the coupling capacitance between the top surface of a wire and the facing sidewall of the TSV.

C. Modeling C_{bm}

M1 layer has no additional metal layers below it, so we compute the coupling capacitance C_{bm} between an M1 wire and a sidewall of a TSV as follows:

$$\begin{aligned} C_{\text{sw},4} &= c_{\text{sw},4} \cdot W_{\text{w}} \\ C_{\text{side},5} &= N_{\text{w}} \cdot C_{\text{sw},4} \\ C_{\text{sw},5}(m) &= c_{\text{sw},5}(m) \cdot W_{\text{TSV}} \\ C_{\text{sw},6}(m) &= c_{\text{sw},6}(m) \cdot W_{\text{TSV}} \end{aligned} \tag{24}$$

$$C_{\text{side},6} = \sum_{m=1}^{M'_{\text{w}}} (C_{\text{side},5} + 2 \cdot C_{\text{side},6}) \tag{25}$$

$$C_{\text{bm}} = 2 \cdot (C_{\text{side},5} + C_{\text{side},6}) \tag{26}$$

where $C_{\text{sw},4}$ and $C_{\text{sw},5}(m)$ are the coupling capacitances between the bottom side of wires and the facing sidewall of the TSV, and $C_{\text{sw},6}(m)$ is the coupling capacitance between a sidewall of the mth wire and the facing sidewall of the TSV as shown in Fig. 12(d) and (e). We determine $L_{\text{fr},2}$ empirically.

D. Modeling C_{TT}

Lastly, we compute the C_{TT} as follows:

$$\begin{aligned} C_{\text{c3}} &= \varepsilon_{\text{di}} \frac{(H_{\text{TSV}} - 2 \cdot H_{\text{INT}} - 2 \cdot L_{\text{fr},2}) W_{\text{TSV}}}{S_{\text{TSV}}} \\ C_{\text{c4}} &= \frac{\varepsilon_{\text{di}}}{\pi\sqrt{2}} \cdot H_{\text{TSV}} \cdot K_{\text{corner}} \\ C_{\text{TT}} &= 4(C_{\text{c3}} + C_{\text{c4}}) \end{aligned} \tag{27}$$

where C_{c3} is the coupling capacitance between two TSVs placed in parallel, and C_{c4} is the coupling capacitance between two TSVs placed diagonally.

E. Modeling of Misalignment

Misalignment between TSVs occurs due to imperfectness of die aligning [23]. Therefore we also show TSV capacitance modeling under misalignment. Fig. 12(f) shows our model for misalignment. In this model, we assume that the capacitance near the bonding layer is not affected by surrounding wires of TSVs for simplification.

In Fig. 12(f), C_{m1} is computed by the area capacitance equation, and C_{m2} is computed by Table II and the following equation:

$$C_{\text{m2}} = c_{\text{m2}} \cdot W_{\text{TSV}} \tag{28}$$

where c_{m2} is the coupling capacitance between the top surface of a TSV and the facing sidewall of its neighboring TSV.

VI. TSV Capacitance Extraction and Simulation

We use SUN UltraSPARC-II 400 MHz machine with 4 GB main memory for Synopsys Raphael simulation [24]. Wire width is 0.2 μm, wire thickness is 0.36 μm, wire-to-wire

TABLE III
COMPARISON OF CAPACITANCES FOR TSVS WITH WIRES ABOVE AND BELOW THE TSVS UNDER PERFECT TSV-TO-TSV ALIGNMENT. COMPUTATION TIME OF OUR MODEL IS NEGLIGIBLE FOR ALL THE CASES

TSV dimension (μm)			TSV capacitance (fF)			Breakdown of capacitive components						Raphael runtime (minutes)
						Raphael			Our model			
Width	Spacing	Height	Raphael	Our model	Error	C_{TT}	C_{top}	C_{side}	C_{TT}	C_{top}	C_{side}	
5	5	5	8.868	9.389	5.88%	14.86%	53.3%	31.84%	15.72%	56.21%	28.07%	3
		20	18.336	19.102	4.18%	57.04%	26.12%	16.84%	58.57%	27.63%	13.8%	3
		50	37.033	37.129	0.26%	78.69%	12.94%	8.37%	78.69%	14.21%	7.10%	4
		100	68.227	67.174	−1.54%	88.36%	7.04%	4.60%	88.22%	7.86%	3.92%	4
	10	20	15.706	15.939	1.48%	29.17%	32.01%	38.82%	32.5%	39.07%	28.43%	6
		50	27.984	29.615	5.83%	60.15%	17.97%	21.88%	63.67%	21.02%	15.31%	6
		100	48.437	49.301	1.78%	76.97%	10.39%	12.64%	78.18%	12.63%	9.19%	7
10	10	10	26.079	27.210	4.34%	7.45%	62.55%	30.01%	10.85%	65.32%	23.83%	15
		20	32.645	32.752	0.33%	22.91%	50.59%	26.50%	25.94%	54.26%	19.80%	16
		50	51.392	52.644	2.44%	50.84%	32.19%	16.97%	53.92%	33.76%	12.32%	16
		100	82.570	82.689	0.14%	69.40%	20.03%	10.57%	70.66%	21.49%	7.85%	19
20	20	20	81.140	82.352	1.49%	3.59%	72.54%	23.86%	7.17%	74.16%	18.67%	20
		50	101.040	99.679	−1.35%	19.41%	58.98%	21.61%	23.31%	61.27%	15.42%	23
		100	132.188	133.222	0.78%	38.48%	45.06%	16.46%	42.62%	45.84%	11.54%	24
50	25	50	403.026	385.697	−4.30%	7.22%	80.77%	12.01%	9.80%	81.88%	8.32%	60
		100	454.968	441.124	−3.04%	17.82%	71.54%	10.64%	21.14%	71.59%	7.27%	64
		200	558.915	542.651	−2.91%	33.11%	58.23%	8.66%	35.89%	58.20%	5.91%	110
	50	50	398.710	386.463	−3.07%	1.41%	83.21%	15.37%	3.82%	84.60%	11.58%	120

TABLE IV
COMPARISON OF CAPACITANCES FOR TSVS WITH WIRES ABOVE, BELOW, AND IN THE SIDE OF THE TSVS UNDER PERFECT TSV-TO-TSV ALIGNMENT. COMPUTATION TIME OF OUR MODEL IS NEGLIGIBLE FOR ALL THE CASES

TSV dimension (μm)				TSV capacitance (fF)			Breakdown of capacitive components						Raphael runtime (minutes)
							Raphael			Our model			
Width	Spacing	Height	S_{min}	Raphael	Our model	Error	C_{TT}	C_{top}	C_{inter}	C_{TT}	C_{top}	C_{inter}	
5	5	5	0.5	8.055	8.572	6.03%	0.46%	40.28%	59.26%	0.13%	43.52%	56.35%	120
		20	1.0	16.280	15.570	−4.36%	50.92%	21.92%	27.16%	48.59%	20.11%	31.30%	120
		50	2.0	33.751	35.115	4.04%	81.32%	11.76%	6.92%	80.63%	10.72%	8.65%	120
		100	2.0	64.799	67.581	4.29%	90.27%	6.13%	3.60%	93.98%	5.23%	0.79%	143
10	5	10	1.0	24.174	24.981	3.23%	15.75%	52.61%	31.64%	16.41%	50.48%	33.11%	300

spacing is 0.2 μm, and wire-to-TSV spacing is 0.3 μm. Liner thickness is 0.1 μm.

A. TSVs With Top and Bottom Neighbors

Our Raphael simulation structure consists of nine TSVs forming a 3 × 3 array and wires above and below the TSVs, as shown in Fig. 11(f) and (a). We compute the capacitance of the center TSV assuming all other TSVs and wires are grounded. Table III shows capacitances for various TSV dimensions.

We observe that the relative difference between Raphael and our modeling is less than 5.88% for all the cases and the average error is 2.51% which is very small. We also show the breakdown of capacitive components to show that our model for each capacitance component is accurate. In the table, C_{TT} is the TSV-to-TSV coupling capacitance, C_{top} is the coupling capacitance between a TSV and wire pieces right above the $\mathrm{TSV}(= C_{\mathrm{top},1} + C_{\mathrm{top},2})$, and C_{side} is the coupling capacitance between a TSV and wire pieces outside the top surface of the $\mathrm{TSV}(= C_{\mathrm{side},1} + C_{\mathrm{side},2})$. The difference between Raphael simulation and our model is again very small, which shows that our model is highly accurate. Moreover, the result shows that C_{top} and C_{side} are not negligible when TSV is relatively short compared to the TSV width. Therefore we need to consider TSV-to-wire capacitance for the computation of TSV capacitance. Raphael runtime is much higher but the computation time of our model is negligible.

B. TSVs With Top, Bottom, and Side Neighbors

Our Raphael simulation structure consists of nine TSVs forming a 3 × 3 array and wires above, below, and in the side of the TSVs as shown in Fig. 11(f) and Fig. 12(a). We compute the capacitance values of the center TSV assuming all other TSVs and wires are grounded. Table IV shows that the difference between Raphael simulation and our model is less than 6.03% for all cases and the average error is 4.39% which is acceptable for fast estimation of TSV capacitances. The breakdown of capacitive components also shows that our model is highly accurate in computing individual capacitive components as well. In Table IV, C_{inter} is the sum of $C_{\mathrm{side},3}$, $C_{\mathrm{side},4}$, and C_{bm}. Since there are many more wires in this simulation structure than the case shown in Section VI-A, Raphael runtime is excessively high. Moreover, we could not run Raphael simulation on more complicated structures due to huge memory requirement (more than 6–8 GB).

C. TSV Under Misalignment

Our Raphael simulation structure contains nine TSVs on a 3 × 3 array and another nine TSVs on top of those with misalignment. The simulated values are the capacitances of the center TSV. Table V shows the comparison. The result shows that the capacitance change due to misalignment is not significant if the misalignment ratio is less than 20%. The relative difference between Raphael simulation and our model is less than 3.59% for

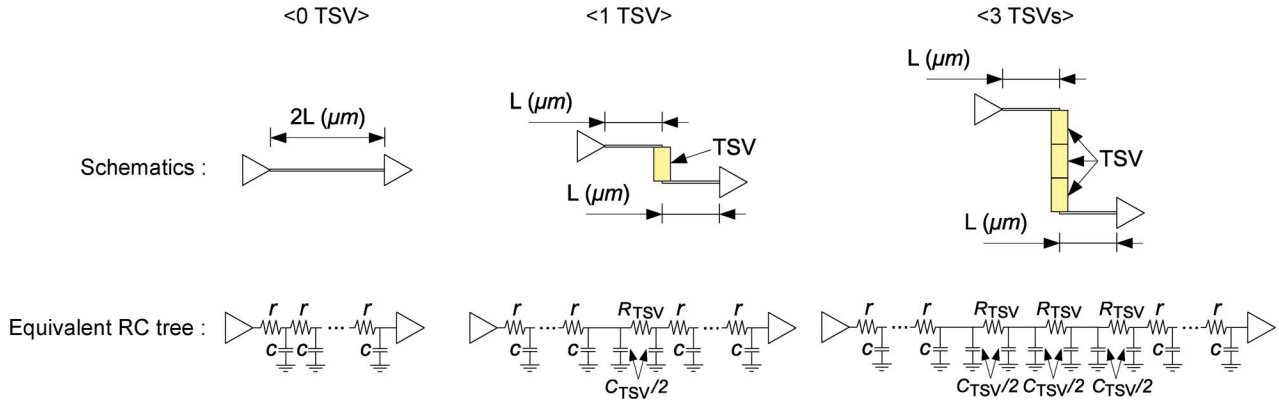

Fig. 13. Schematics for the delay simulation in Table VII. C_{TSV} is the total capacitance (the sum of TSV-to-wire coupling capacitances and TSV-to-TSV coupling capacitances) of a TSV.

TABLE V
TSV CAPACITANCE UNDER MISALIGNMENT. M_{TSV} IS THE MISALIGNMENT RATIO. CAPACITANCE VALUES ARE REPORTED IN fF. THE DIMENSION OF WIDTH, SPACING, AND HEIGHT IS μm

Width	Spacing	Height	M_{TSV}	Raphael	Our model	Error
5	5	5	0%	6.412	6.475	0.98%
			5%	6.269	6.449	2.87%
			10%	6.348	6.438	1.42%
			20%	6.504	6.469	−0.54%
		50	0%	64.117	64.753	0.99%
			5%	62.485	64.726	3.59%
			10%	62.642	64.716	3.31%
			20%	63.061	64.747	2.67%
20	20	20	0%	25.647	25.901	0.99%
			5%	25.078	25.795	2.86%
			10%	25.393	25.752	1.41%
			20%	26.017	25.876	−0.54%
		50	0%	64.117	64.753	0.99%
			5%	62.581	64.646	3.30%
			10%	62.898	64.604	2.71%
			20%	63.709	64.728	1.60%
50	50	100	0%	128.234	129.506	0.99%
			5%	125.201	129.239	3.23%
			10%	125.914	129.133	2.56%
			20%	128.303	129.443	0.89%

TABLE VI
COMPARISON BETWEEN TSV CAPACITANCE AND WIRE CAPACITANCE. WE REPORT THE RATIO OF TSV CAPACITANCE TO WIRE CAPACITANCE. WIRE WIDTH IS 0.2 μm, WIRE THICKNESS IS 0.36 μm, HORIZONTAL WIRE SPACING IS 0.2 μm, AND VERTICAL WIRE SPACING IS 0.3 μm. L IS THE WIRELENGTH

TSV dimensions	$L(\mu m)$	TSV height		
		$20\mu m$	$50\mu m$	$100\mu m$
width : $5\mu m$ spacing : $5\mu m$	50	4.37	8.50	15.38
	300	0.73	1.42	2.56
	1000	0.22	0.43	0.77
	2000	0.11	0.21	0.38
	5000	0.04	0.09	0.15
width : $20\mu m$ spacing : $20\mu m$	50	18.85	22.82	30.50
	300	3.14	3.80	5.08
	1000	0.94	1.14	1.52
	2000	0.47	0.57	0.76
	5000	0.19	0.23	0.30

all the cases. If a rough approximation for misalignment is sufficient, we do not need to consider C_{m2}. However, including C_{m2} results in more accurate capacitance values.

TABLE VII
DELAY OF 3D INTERCONNECTS. SCHEMATICS FOR THIS SIMULATION ARE SHOWN IN FIG. 13. WE SCALE ALL THE DELAY VALUES TO THE BOLDFACE CASE

		TSV dimensions					
		$w = 5\mu m$ $s = 5\mu m$ $h = 20\mu m$		$w = 10\mu m$ $s = 10\mu m$ $h = 100\mu m$		$w = 20\mu m$ $s = 20\mu m$ $h = 50\mu m$	
$L(\mu m)$	0 TSV	1 TSV	3 TSVs	1 TSV	3 TSVs	1 TSV	3 TSVs
50	0.32	**1.00**	2.06	2.83	7.86	3.35	9.41
300	1.65	2.23	3.39	4.17	9.20	4.68	10.75
1000	5.39	5.98	7.14	7.92	12.97	8.44	14.53
2000	10.78	11.37	12.54	13.32	18.40	13.84	19.97
5000	27.31	27.91	29.10	29.90	35.06	30.42	36.65

D. Impact of TSV Capacitance on Delay

In this experiment, we study the impact of TSV capacitance on delay because TSV capacitance is not negligible. Table VI shows ratios of TSV capacitance to wire capacitance. When the wirelength (L) is short (up to 100 μm), TSV capacitance is much bigger than wire capacitance. For instance, the capacitance of a TSV whose width is 5 μm, spacing is 5 μm, and height is 50 μm is 8.5× bigger than the capacitance of a wire whose length is 50 μm. Similarly, TSV capacitance is 22.82× bigger than wire capacitance when the TSV width is 20 μm, TSV-to-TSV spacing is 20 μm, the TSV height is 50 μm, and the wirelength is 50 μm. As the wirelength goes up, on the other hand, wire capacitance becomes much bigger than TSV capacitance.

Next, we show the impact of TSVs on 3D interconnect delay. In our SPICE simulation, a signal goes through a wire, one TSV (or three TSVs), and then another wire whose length is same as that of the first wire as shown in Fig. 13. Table VII shows the delay values for various TSV dimensions. When the wirelength is short, the number of TSVs in the interconnect (1 versus 3 TSVs) affects the delay significantly. For instance, the delay of "3 TSVs" case is 2.06× to 2.81× bigger than "1 TSV" case when L is 50 μm. However, the impact of TSVs decreases as the wirelength increases because long wires have larger parasitic capacitance than TSVs so that wire capacitance becomes dominant in long wires.

TABLE VIII
TSV-TO-TSV COUPLING CAPACITANCE VERSUS TSV MOS CAPACITANCE. THESE NUMBERS DO NOT INCLUDE TSV-TO-WIRE CAPACITANCE. w IS TSV WIDTH, h IS TSV HEIGHT, AND s IS TSV-TO-TSV SPACING

TSV dimensions (in μm)			MOS cap. (fF)	Coupling cap. (fF)
w	h	s		
5	20	5	27.5	13.4
		10		8.78
	50	5	68.8	32.2
		10		21.2
10	50	10	74.3	32.2
		20		21.1
	100	10	148.5	63.6
		20		41.6

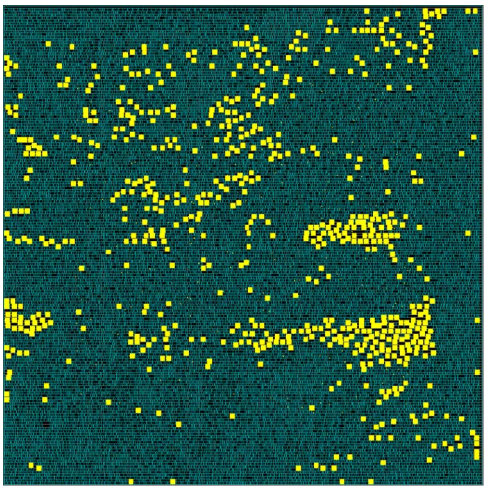

Fig. 14. An example layout of a 3D IC designed by 3D IC design methodology presented in [3]. We use via-first TSVs and stack two dies with face-to-back bonding. Bright rectangles are TSV landing pads (TSVs exist inside landing pads), and dark rectangles are standard cells.

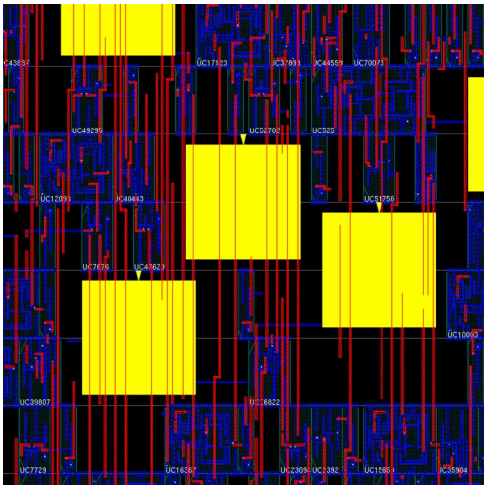

Fig. 15. Zoom-in shot of Fig. 14. Bright big rectangles are TSV landing pads (TSVs exist inside landing pads), and thin vertical lines above TSVs are metal wires.

E. Comparison Between TSV Coupling and MOS Capacitance

In previous works such as [13], [16], TSV MOS capacitance is used for TSV capacitance. Therefore, we compare TSV coupling capacitance and TSV MOS capacitance in this section. Table VIII compares the TSV-to-TSV coupling capacitance with TSV MOS capacitance computed by capacitance equations presented in [16].[4] We observe in the table that the coupling capacitance is smaller than MOS capacitance. For example, when the TSV width is 10 μm and the TSV height is 50 μm, MOS capacitance is 74.3 fF but the coupling capacitance is 21.1 fF when the TSV-to-TSV spacing is 20 μm. The results indicate that using MOS capacitance is not accurate because it does not take TSV-to-TSV capacitive coupling into account.

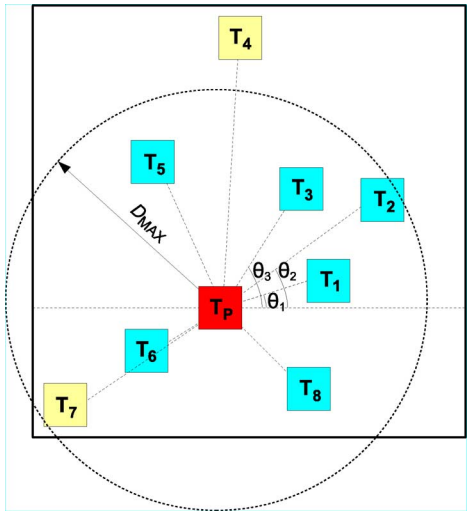

Fig. 16. A general layout where TSVs are placed irregularly. We compute the capacitance of $\mathrm{T_P}$.

VII. ANALYZING MORE GENERAL LAYOUTS

In previous sections, we focused on two regular TSV structures, where a given TSV is surrounded by eight neighboring TSVs and full of wires above, below, and in the side of the TSVs. In real layouts, however, this kind of regular TSV arrangement rarely happens unless we use highly regular TSV placement as presented in [3]. Fig. 14 shows an example layout in which there are 152 K cells and 428 TSVs, and Fig. 15 shows a zoom-in shot of Fig. 14. We observe that regular TSV structures do not occur in this layout. Rather, it is required to handle more general layouts. In this section, therefore, we present a methodology for the analysis of general layouts and compare the results against Raphael simulation.

A. Methodology for General Layout Analysis

In this section, we show our algorithm for computation of TSV capacitance in general layouts where TSVs are placed irregularly.

1) Sorting TSVs: The first step used to compute TSV capacitance is sorting TSVs as follows. We draw a horizontal line (l_0) passing through the center of $\mathrm{T_P}$ and a line (l_n) connecting the centers of $\mathrm{T_P}$ and T_n as shown in Fig. 16. The TSVs are sorted in the ascending order of the angle between l_0 and l_n, denoted by θ_n. The range of θ_n is greater than or equal to 0 (rad) and less than 2π (rad).

[4]We do not include TSV-to-wire coupling capacitance here.

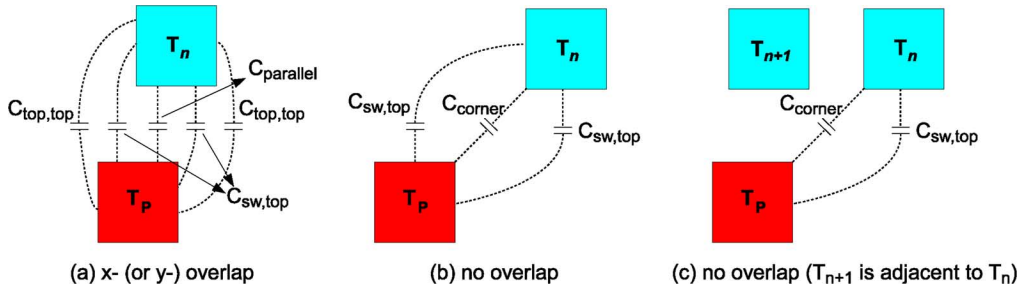

Fig. 17. Capacitance computation for a pair of TSVs. If there exists an x- or y-overlap, we apply $C_{\rm parallel}$, $C_{\rm sw,top}$, and $C_{\rm top,top}$ as shown in (a). If there is no overlap, we apply $C_{\rm corner}$ and $C_{\rm sw,top}$ as shown in (b) and (c).

2) Extracting Meaningful TSVs: After sorting TSVs, meaningful TSVs for the given target TSV, $\mathrm{T_P}$, are extracted. A meaningful TSV is a TSV, T_n, satisfying the following two conditions.

- **Distance condition**: The distance from $\mathrm{T_P}$ to T_n is less than a distance $D_{\rm MAX}$ predetermined empirically. For instance, the area capacitance between the facing sidewalls of two TSVs at a distance of d is approximately 1 fF, we set $D_{\rm MAX}$ to be d.
- **Visibility condition**: T_n is visible from $\mathrm{T_P}$. T_n is said to be visible from $\mathrm{T_P}$ if the following inequality is satisfied:

$$|\theta_m - \theta_{m+1}| \geq \theta_{\rm MIN} \tag{29}$$

where m is the TSV index, and $\theta_{\rm MIN}$ is the predetermined angle (0.1π in our simulations). If two adjacent TSVs in the sorted TSV list violate the visibility condition, the TSV having shorter distance from $\mathrm{T_P}$ is set to be a meaningful TSV and the other TSV is eliminated from the list. The sorted TSV list is circular. For instance, the angular difference between T_8 and T_1 in Fig. 16 is computed to determine if one of them is a meaningful TSV or not.

TSVs that do not satisfy the distance condition are excluded during capacitance computation. The reason is that the coupling capacitance between $\mathrm{T_P}$ and T_n becomes too small if they are separated by a large distance. For instance, T_4 in Fig. 16 is excluded due to violation of the distance condition.

TSVs that do not satisfy the visibility condition are also excluded during capacitance computation. They are excluded because electric field diverging from $\mathrm{T_P}$ does not reach T_n if another TSV exists in between $\mathrm{T_P}$ and T_n. For instance, T_7 in Fig. 16 is excluded because $|\theta_6 - \theta_7|$ is less than $\theta_{\rm MIN}$ and T_7 is farther away from $\mathrm{T_P}$ than T_6.

3) Capacitance Computation for Meaningful TSVs: After extracting the list of meaningful TSVs, we compute the capacitance of $\mathrm{T_P}$ by summing the coupling capacitance between $\mathrm{T_P}$ and each meaningful TSV, T_n. The computation step is as follows.

If there is an overlap in x- or y-coordinates of $\mathrm{T_P}$ and T_n as shown in Fig. 17(a), we apply the parallel capacitance equation for the overlapped region. For nonoverlapped regions, we apply $C_{\rm sw,top}$ and $C_{\rm top,top}$.

On the other hand, if there is no overlap in x- or y-coordinates of $\mathrm{T_P}$ and T_n as shown in Fig. 17(b), we apply $C_{\rm corner}$ and $C_{\rm sw,top}$. When we apply $C_{\rm sw,top}$, we also compare the relative position of T_n and T_{n+1} (or T_{n-1}) as shown in Fig. 17(c). If T_{n+1} (or T_{n-1}) blocks the path of the electrical field diverging from $\mathrm{T_P}$ to a sidewall of T_n, we do not apply $C_{\rm sw,top}$ for the sidewall of T_n.

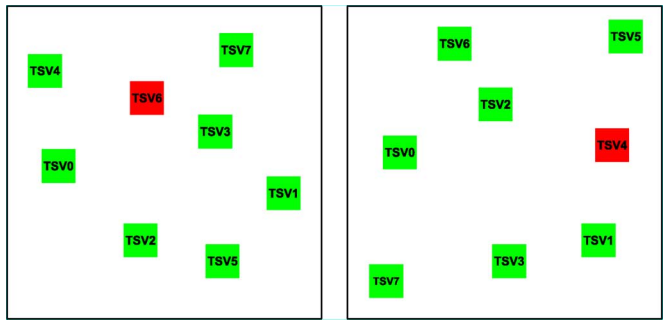

Fig. 18. Two general (= nonregular) example layouts. The total number of TSVs is eight. The electric potential of one of them (= red regular) is set to $\mathrm{V_{DD}}$, while that of all others are set to 0.

B. Simulation Results

We first distribute TSVs in a fixed-size window as shown in Fig. 18. Then we choose one TSV out of the TSVs and set the potential of the TSV to be $\mathrm{V_{DD}}$ while setting the potential of all other TSVs to be zero. For a randomly-generated layout, 1) we run our capacitance estimation program and obtain the capacitance of the red TSV, 2) we convert the structure into Raphael input format, run Raphael, and obtain the capacitance of the red TSV, and 3) we compare those two values.

Fig. 18 shows two example layouts. Each square represents a TSV, and the electric potential of green squares is set to zero while that of red square is set to $\mathrm{V_{DD}}$.

Table IX shows the average relative errors between Raphael simulation and our model on random structures. For each simulation set (e.g. 5 μm width and minimum spacing, 50 μm height, and total six TSVs in the layout), we generate 20 random structures, compute errors for each structure, and obtain average and maximum errors out of 20 errors. In all the cases, the errors are less than 18.91% and the average error ranges between 8.18% and 11.86%, which is acceptable for fast estimation for quick full-chip timing analysis and layout optimization. The runtime of Raphael simulation is negligible when there are few objects and the layout boundary is small. However, it takes several seconds to compute coupling capacitances when there are more than ten objects and the layout boundary is large. Since this is the extraction runtime for one TSV, the actual runtime becomes

TABLE IX
CAPACITANCE EXTRACTION ON GENERAL LAYOUTS

TSV dimensions (μm)			# TSVs	Average error (%)	Max. error (%)
Width	Min. spacing	Height			
5	5	50	6	8.79	16.15
			8	10.20	15.59
			10	8.48	14.92
			12	11.86	15.79
		100	6	9.70	15.78
			8	10.49	16.94
			10	11.20	15.03
			12	8.53	14.82
10	10	50	6	10.68	16.15
			8	9.36	14.55
			10	11.44	17.18
			12	11.22	18.91
		100	6	10.10	17.06
			8	9.07	14.62
			10	10.08	15.48
			12	8.18	14.79

N times longer when there exist N TSVs. On the other hand, our capacitance estimation is extremely fast. This clearly shows the effectiveness of our model for the fast estimation of TSV coupling capacitance.

VIII. CONCLUSION

In this paper, we analyze various parasitic coupling capacitive components of through-silicon vias (TSVs). Our model considers coupling with surrounding wires in lateral and vertical directions as well as neighboring TSVs. The error between our model and Synopsys Raphael simulation on the two regular structures remains less than 6.03%, and the average error on more general structures is around 11.86%. However, our analytical model requires a fraction of Raphael simulation runtime to compute the coupling capacitances. Therefore our quick but relatively accurate analytical model will be helpful for CAD applications such as full-chip timing analysis and layout optimization in 3D ICs.

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Dae Hyun Kim (S'08) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2002, and the M.S. degree in electrical and computer engineering, in 2007, from Georgia Institute of Technology, Atlanta, where she is currently working toward the Ph.D. degree in the School of Electrical and Computer Engineering.

His research interests are physical design algorithms for 3D ICs including design methodology, placement, routing, and design for manufacturability.

Saibal Mukhopadhyay (S'00–M'07) received the B.E. degree in electronics and telecommunication engineering from Jadavpur University, Calcutta, India, in 2000, and the Ph.D. degree in electrical and computer engineering from Purdue University, West Lafayette, IN, in 2006.

He is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, as an Assistant Professor. Prior to joining Georgia Tech, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, as a Research Staff Member. His research interests include low-power variation tolerant VLSI circuits and systems, embedded systems, and 3D integration. He has (co)-authored over 90 papers in refereed journals and conferences.

Dr. Mukhopadhyay was a recipient of the IBM Faculty Partnership Award for 2009 and 2010, SRC Inventor Recognition Award in 2009, SRC Technical Excellence Award in 2005, IBM PhD Fellowship Award for 2004–2005, the Best in Session Award at 2005 SRC TECNCON, Best Paper Awards at 2003 IEEE Nano and 2004 International Conference on Computer Design.

Sung Kyu Lim (S'94–M'00–SM'05) received the B.S., M.S., and Ph.D. degrees from the Computer Science Department, University of California, Los Angeles (UCLA), in 1994, 1997, and 2000, respectively.

From 2000 to 2001, he was a Post-Doctoral Scholar at UCLA, and a Senior Engineer at Aplus Design Technologies, Inc. He joined the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, in 2001, where he is currently an Associate Professor. His research focus is on the physical design automation for 3D ICs, 3D System-in-Packages, microarchitectural physical planning, and field-programmable analog arrays. He is the author of *Practical Problems in VLSI Physical Design Automation* (Springer, 2008).

Dr. Lim received the Design Automation Conference (DAC) Graduate Scholarship in 2003 and the National Science Foundation Faculty Early Career Development (CAREER) Award in 2006. He was on the Advisory Board of the ACM Special Interest Group on Design Automation (SIGDA) during 2003–2008 and received the ACM SIGDA Distinguished Service Award in 2008. He is currently an Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS (TVLSI) and served as a Guest Editor for the ACM Transactions on Design Automation of Electronic Systems (TODAES). He has served the Technical Program Committee of several ACM and IEEE conferences on electronic design automation.