A Study of Signal Integrity Issues in Through-Silicon-Via-based 3D ICs

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***Abstract*— In this paper, we study the signal integrity issues of through-silicon-via (TSV)-based 3D IC layouts. Unlike the most existing work, our study reports the coupling noise among all nets and all TSVs used in a real processor design implemented in 3D. Our RTL-to-GDSII design flow consists of commercial tools, enhanced with various add-ons to handle TSV and 3D stacking. Using this tool flow, we generate GDSII-level layouts of 3D implementation and perform sign-off-level signal integrity analysis. Based on our 2D vs 3D GDSII comparisons, we found that the overall noise-level of 3D is worse than 2D, but 3D designs have the advantage of significantly reducing the total number of the nosiest nets.**

I. Introduction

Through-Silicon-Via (TSV) and 3D stacking technology are currently being actively evaluated as a potential solution to alleviate the interconnect delay problems in giga-scale circuits and systems [1]. However, signal integrity (SI) is another key challenge caused by the advance nano-scale interconnect technologies due to the rising number of analog effects. Through-Silicon-Vias (TSVs) are a non-negligible source of coupling noise that deteriorates the SI of 3D IC layouts, but there is little work on the SI analysis and optimization for TSV-based 3D IC designs, especially at the circuit and system-level.

The impact of TSVs on the signal integrity of 3D IC layout is mainly threefolds. First, TSV landing pads can cause routing congestion problem, which worsen SI performance in the 3D design. A via-first TSV has two large landing pads (LPs) in the first and top metal layers, as shown in Fig. 1(a). These LPs directly take up the routing space from the Mtop and M1 layers (see Fig. 2(a)), making routing in these two layers more challenging. Moreover, TSVs themselves occupy space in the device layers, thereby becoming obstacles for standard cell placement. A poor TSV and/or gate placement is more likely to cause routing congestion. In addition, an LP occupies several standard-cell rows if the TSVs are larger than the gates. In this case, the power stripe routing has to be done in metal layers other than M1, say M3, to avoid shorting with TSV LPs (see Fig. 2(b)). This in turn affects the routing in M3 more challenging.

Second, coupling capacitance caused by TSVs is harmful to SI. Fig. 1(a) shows the possible coupling capacitance between LPs and wires. Experimental results show that the coupling capacitance from the adjacent or overlap wires to the TSV LP is about 1 to $1.2fF$ with a $7\mu m \times 7\mu m$ TSV LP size using 130nm process. Fig. 1(b) illustrates the TSV-to-TSV couplings. The modeling of TSV-to-TSV coupling is not easy because the modeling of the substrate and its ground tap is a complicated problem.

Third, despite the potential SI disadvantages of 3D ICs discussed above, 3D ICs have the advantage of shorter total wirelength compared to 2D ICs [1]. Shorter wirelength helps improve SI performance mainly because the chance of having two long wires running in parallel for a long distance is low if the overall wirelength is reduced. However, wirelength is significantly affected during the physical design steps, i.e., partitioning, placement, and routing. Thus, the SI quality of the final 3D layout with TSVs strongly depends on the quality of these 3D physical design tools.

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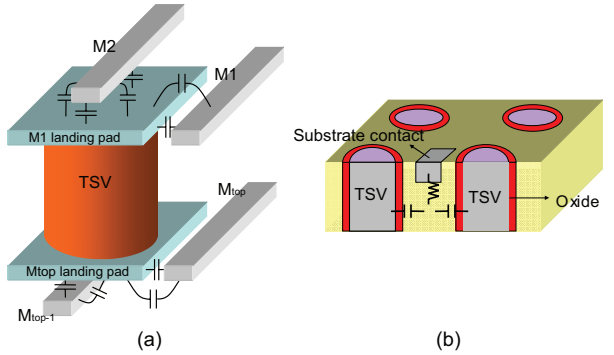

Fig. 1. Coupling between (a) TSV landing pads and wires, (b) TSVs and TSVs

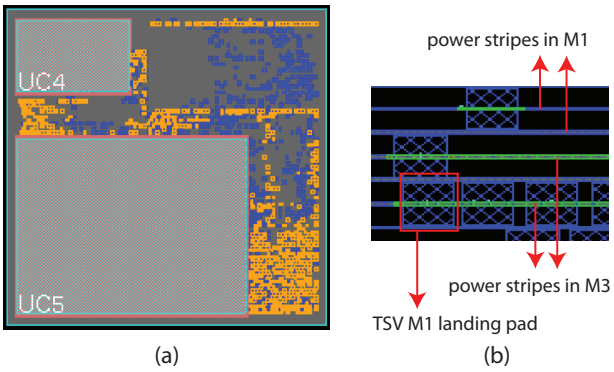

Fig. 2. (a) M6 and M1 routing area taken by TSV landing pads, where the orange and blue regions respectively denote Mtop and M1 landing pads, (b) power stripes used in M1 and M3 due to TSV landing pads

The goal of this paper is to demonstrate how serious the signal integrity problem in TSV-based 3D ICs is compared with 2D counterparts. Unlike the most existing work, our study reports the coupling noise among all nets and all TSVs used in a real processor design implemented in 3D. Our analysis is based on the GDSII-level layouts of 3D ICs and sign-off-level signal integrity analysis.

II. 3D and 2D Designs for LEON3 Processor

We use LEON3 processor to demonstrate our 3D design and SI analysis flow. The LEON3 processor is a 32-bit processor compliant with the SPARC V8 architecture. The design is in $130nm$ process

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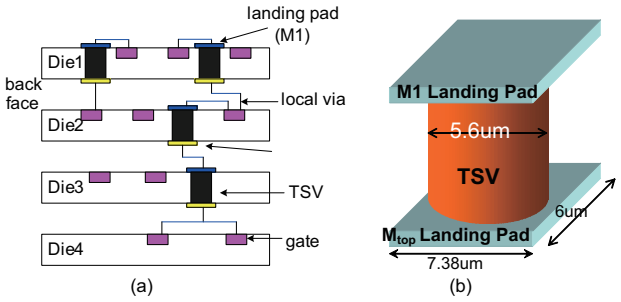

Fig. 3. (a) Side view of 3D stack used in our 3D implementation of LEON3 processor, (b) TSV dimensions used in our experiment

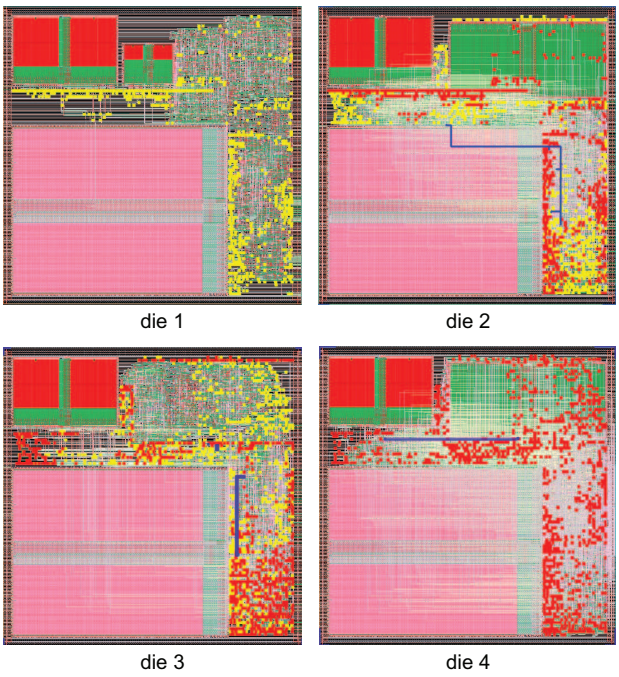

Fig. 4. GDSII layout of LEON3 4-die 3D design used in our signal integrity analysis. Two of the nosiest 3D nets are shown in blue.

with 6 metal layers. The target 3D stacking is shown in Fig. 3(a), where all the 4 dies are stacked in face-to-back fashion with via-first TSVs. As shown in Fig. 3(b), the TSV landing pad on M6 or M1 occupies two standard cell rows each. The diameter of a TSV is $5.6\mu m$.

The GDSII layout of the four dies is shown in Fig. 4. Our RTL-to-GDSII design flow [2] consists of commercial tools, enhanced with various add-ons to handle TSV and 3D stacking. Using this tool flow, we generate GDSII-level layouts of 2D and 3D implementation of LEON3 processor and perform sign-off-level signal integrity analysis. The footprint of a single tier is $750\times750\mu m$. TSV landing pads on M1 and M6 are shown in yellow and red colors, respectively. For comparison, we also designed two other layouts. The first is a 2D design of LEON3 with footprint of $1500 \times 1500\mu m$, which is set so that the total silicon area between the 3D and 2D designs are the same. The second one is a 4-die 3D design with larger $900 \times 900\mu m$ footprint. We refer to these two 3D designs as "3D-small" and "3D-large".

The total wirelength of the 3D-small, 3D-large, and 2D designs are $1,579,680\mu m$, $1,467,300\mu m$ and $1,478,330\mu m$ respectively.

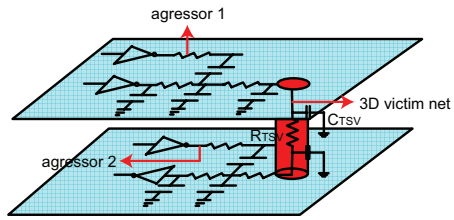

Fig. 5. Illustration of a 3D victim net and SPEF file stitching

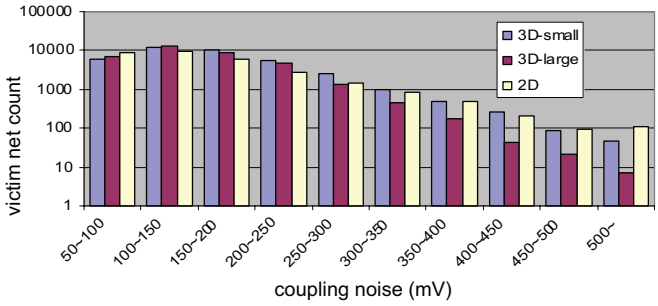

Fig. 6. Coupling noise comparison among the 3 designs: 2D, 3D-small, and 3D–large

On one hand, the longer 3D-small wirelength reveals that our 3D design tool does not fully utilize the benefit from 3D in terms of wirelength. On the other hand, we also see that the wirelength of the 3D-large design is slighly better than the 2D design, and noticeably better than the 3D-small design. This fact shows that that with more routing resource available, it is much easier for 3D design tools to take advantage of TSV-based short interconnect to reduce the overall wirelength.

III. 3D SI Analysis Methodology

3D SI analysis must consider all nets and all TSVs in all 4 tiers simultaneously, because the total noise experience by a 3D net may come from coupling within the same tier as well as neighboring tiers. Fig. 5 shows a 3D net whose aggressors come from both tiers. Currently, there is no commercial tool available for 3D IC signal integrity analysis. Therefore, we designed our 3D SI flow, which utilizes our own scripts in combination with the existing commercial SI (= CeltIC) and timing analysis (= PrimeTime) tools.

First, we use RC extraction tool to obtain the SPEF files containing the interconnect RC information for each die. Note that existing RC extraction tools are able to handle the coupling parasitics between TSV LPs and wires. We also use our in-house tool to generate a SPEF file for TSV parasitic modeling. In this design, we assume the substrate is strongly tied to ground so that TSV-to-TSV coupling is eliminated. Therefore, a π-model is used to model TSV parasitics, as shown in red in Fig. 5. In our experiement, we use $C_{TSV} = 12.5fF$ and $R_{TSV} = 1\Omega$. Next, we use our in-house tool to generate the top level verilog file which contains all four tiers.

Once these files are ready, we use PrimeTime to read in verilog files and SPEF files in incremental mode, and generate a new stitched SPEF file containing the RC information of all the 4 dies and the TSVs. With this stitched SPEF file, we use CeltIC to perform signal integrity analysis. The blue lines in Fig. 4 show two of the nosiest victim 3D net in 3D-small design. The first starts in die2 and ends in die3 with the noise amplitude of $646mV$. The other starts in die3 and ends in die4 with the noise amplitude of $496mV$.

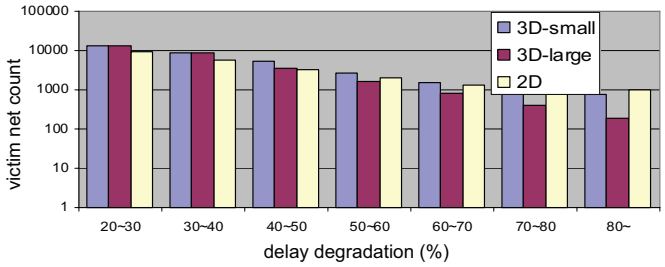

Fig. 7. Delay degradation comparison among the 3 designs: 2D, 3D-small, and 3D–large

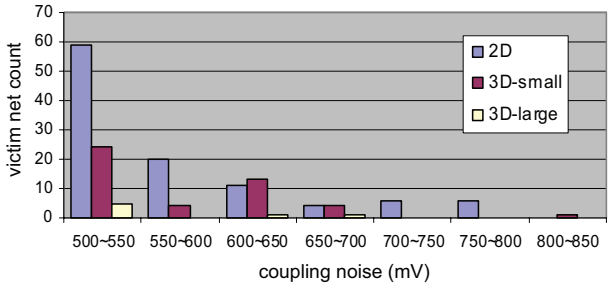

Fig. 8. Coupling noise comparison on the noisiest nets

IV. Experimental Results

A. Overall Noise Comparison

The SI problem manifests itself in two ways, namely glitch and delay degradation [3]. These two types of problems have strong correlation between each other. For comparison, we record the number of nets with glitch greater than 50mV, and delay degradation greater than 20% in all 3 designs. The comparison on glitch noise and delay degradation is shown in Fig. 6 and Fig. 7, where the delay degradation is evaluated by the percentage of the initial delay.

We observe that SI in the 3D-small design is worse than in 2D. The total noise of the 3D-small design is 6225V, which is 35% higher than that of 2D design, whose total noise is 4603V. This shows that if the total silicon area is the same, 3D design suffers more from coupling noise than its 2D counterpart, mainly due to the additional coupling caused by the TSVs. In addition, the wires in 3D-small design are routed in a smaller footprint compared with 2D, which causes more wire-to-wire coupling.

On the other hand, we observe that the SI result in 3D-large design is better than 3D-small design. The total noise of 3D-large is 5336V, which is still 15% higher than the 2D design, but 18% lower than the 3D-small design. The main reason for this SI improvement in 3D-large compared with 3D-small is simply the larger footprint and thus less routing congestion, which helps reduce TSV-to-wire, TSV-to-TSV, and wire-to-wire coupling. We also observe that the overall trend among the 3 designs are similar between the glitch noise and delay degradation metrics.

B. Noise Comparison for Noisy Nets

From Fig. 6 and 7, we observe an interesting fact that in the region above 250mV, the 3D-large glitch result is even better than the 2D design. The same is true in the region above 50% for the delay degradation result. These results show that 3D is capable of reducing the number of the noisiest nets.

To further investigate this, we zoom in the "high noise" region in Fig. 6 and 7. Fig. 8 and 9 show the total count of victim nets with

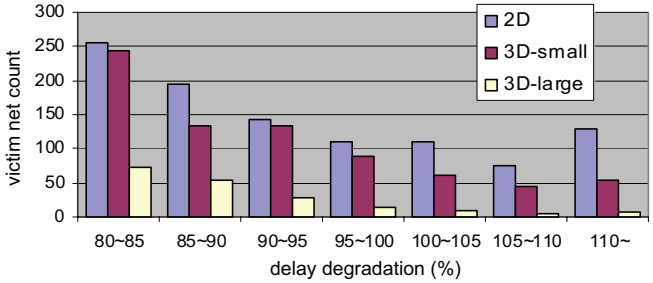

Fig. 9. Delay degradation comparison on the nosiest nets

TABLE I
Summary of the SI analysis

	2D	3D-small	3D-large
Footprint (μm)	1500×1500	750×750	900×900
Silicon Area (mm^2)	2.25	2.25	3.24
Wirelength (μm)	1,478,330	1,579,680	1,467,300
Total noise (V), nets $>$ 50mV	4603	6225	5336
Total noise (V), nets $>$ 500mV	61	25	4

glitch noise bigger than 500mV and with delay degradation bigger than 80%, respectively. Interestingly, these figures show that both 3D-large and 3D-small outperform 2D design in terms of both glitches and delay degradation. This supports the point that 3D is effective in reducing the number of nosiest nets. The main reason is that the total number of long wires in 3D is smaller than 2D due to the short vertical connections made with TSVs, which in turn causes coupling noise on noisy nets to decrease. In addition, based on the comparison between 3D-small and 3D-large, we observe that larger footprint is still beneficial to 3D designs in terms of signal integrity.

Table I summarizes the SI results of the three designs. We see that, although the total noise is worse in 3D designs compared with 2D, the number of noisy nets (= more troublesome nets) is significantly reduced in 3D designs. We also observe that the proper footprint area is crucial for 3D designs to alleviate the SI problem and reduce the total wirelength.

V. Conclusions

In this paper, we presented a signal integrity study for 3D ICs based on GDSII layouts of commercial processor design. A method to perform sign-off 3D SI analysis is proposed. Analysis results show that the overall SI is worse in 3D design compared with 2D when using the same silicon chip area. However, by increasing the footprint area, the signal integrity problem is improved significantly. In addition, we observed that 3D is effective in reducing the number of nosiest nets. The main reason is that the total number of long wires in 3D is smaller than 2D due to the short vertical connections made with TSVs, which in turn causes coupling noise on noisy nets to decrease.

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