Automatic Layout Generation of RF Embedded Passive Designs

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Abstract

In this paper we propose a methodology for automatic layout generation of embedded passive RF circuits. Physical layout generation of such designs is challenging since the response of a given layout is tightly coupled with the response of the individual components and the effect of interconnect parasitics. Our approach is to make use of circuit models to represent and optimize a given layout and use non-linear optimization at various stages to obtain the desired goals. Full-wave EM simulations is completely out of the design loop, so our methodology significantly reduces the design time for RF embedded passive circuits.

I. Introduction

Embedded passive is an emerging technology that has a potential for increased reliability, improved electrical performance, size shrinkage and reduced cost [1]. Using this technology, surface-mount passive components used in systems are integrated into packaging substrate via multiple layers. However, the design of circuits with embedded passives is non-trivial due to the electromagnetic interactions that cause parasitics, leading to non-ideal frequency behavior. In this paper we target RF embedded passive filter designs using liquid crystalline polymer (LCP) substrate. Layout generation for such designs is not an easy task. The desired response of a given layout is tightly coupled with the response of each of the individual components and the effect of parasitics due to interconnects between them. The manual design cycle for generation of such layouts can be extremely time-consuming. A minor change in the layout may cause a drastic change in the frequency response. A conventional design flow tries to optimize circuit performance at the layout level at the premium cost of time-consuming EM iterations (using a full-wave EM simulation tool like SONNET) for entire layouts.

Our goal is to develop a tool that quickly generates and optimizes RF embedded passive circuits in LCP substrate automatically. An early work [2] targets primarily CMOS technology, not packaging substrate such as LCP or LTCC. They do not describe a way of estimating parasitics for more than 2-pin nets. Such an approach would not work for RF embedded passive circuit since knowing the exact nature of interconnect parasitics is critical. Sommer et al. [3] presented a layout synthesis algorithm for embedded passive components such as capacitor, resistor and inductor. But, they did not discuss how to use them to construct an entire circuit. Mukherjee et al. [1] discuss another technique for automating the design of passive components. They also suggest how to analyze an entire embedded passive circuit, but their approach is limited to optimizing a given layout instead of constructing one.

Our contribution is a design methodology that automates the design process of LCP-based embedded passive designs from its circuit model to the layout. We make use of circuit models to represent and optimize a given layout and use non-linear optimization at various stages of the methodology to obtain the desired goals. Full-wave EM simulations is completely out of the design loop. Thus, our methodology significantly reduces the design time for RF embedded passive circuits. In addition, we provide the designer with an initial layout solution that closely matches the desired response. Since it is easier to tweak a given good solution to meet the desired goals rather than starting from scratch, our design flow can help reduce design times significantly.

II. Preliminaries

A. Problem Formulation

We assume that the following are given: (i) a netlist of the given RF circuit consisting of a set of passive components (we restrict ourselves to inductors and capacitors for RF filter designs) and nets, (ii) initial value of the components, (iii) a set of design goals such as center/resonent frequency, bandwidth, insertion loss, etc, (iv) a parameterized library that consists of inductors, capacitors, interconnects, and coupling models. The goal of *Embedded Passive Physical Design* is to automatically generate a layout of the given circuit (= placement and routing of the components) such that the performance objectives are achieved and the area of the layout is minimized. Our target packaging substrate consists of two metal layers separated by a LCP layer for component placement (= minimum required to place a capacitor) and routing [1].

B. Design Flow

Our approach is to optimize the component placement using Simulated Annealing and component routing using parasitic-aware maze-routing. We perform non-linear optimization at various steps of the layout generation process to meet the desired performance objectives while minimizing the area of the layout. Our method consists of the following steps:

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- Step 1: component shapes are chosen from the library based on their initial values.
- Step 2: these components are resized during our pre-layout optimization step by ADS (Advanced Design System by Agilent), a circuit-level simulator and optimizer. This is necessary to consider the effects of various component parasitics such as vias connecting to ground, wire connection from the core to boundary, etc. The geometric shapes change slightly during this step.
- Step 3: we perform placement and routing using the optimized components. Component coupling and wire parasitics are introduced during this step. The objectives during this step include layout area, wirelength, and routability. We save K_1-best layouts based on these objectives.
- Step 4: for each of the K_1-best layouts, we derive the circuit model and evaluate using ADS. The goal is to select K_2-best layouts that achieve the responses that are closest to our goals. The circuit model of the components and their coupling are extracted from the placement, whereas the wire and via parasitics are derived from the routing.
- Step 5: for each of the K_2-best layouts, we perform non-linear circuit optimization again using ADS on the entire layout. The components and wires are again re-sized during this step so that the overall circuit response best meets our goals.
- Step 6: The white space introduced during the post-layout optimization step is removed during our layout compaction step. The goal is to preserve the circuit response while optimizing the layout area. The component placement and routing change slightly during this step.

In case the final compacted layout passes our final circuit-level verification, we perform a full-wave EM simulation using SONNET for final verification. If not, we repeat the entire process starting from placement and routing (or even component selection and optimization). Our final solution can be used for further manual touch-up if necessary.

III. Pre-layout Optimization

The objective of our pre-layout optimization is to find optimized component dimensions which meet the desired circuit objectives while considering intra-component parasitics. The circuit elements in each component are grouped into two categories, namely, dominating elements, and parasitic elements. The dominating element values reflect the main inductance or the capacitance value of a given component. During initial selection, the components were selected based on their dominating element values. Due to the effect of parasitics in each component, the initial selection does not always meet the desired circuit response. The goal of our pre-layout optimization is to find new components (possibly with new dimensions) such that they meet the desired circuit responses while considering both the dominating and parasitic elements. In addition to intra-component parasitics, additional parasitics such as vias connecting to ground, core-to-boundary elongation are also modeled. Due to these changes in the circuit model, the overall shape of the component after the optimization may change. Note that the optimization is applied not to individual components but to the circuit model of the *entire* design. Since the optimization is performed before placement and routing, the effect of interconnect parasitic and component coupling are not considered in this case. Note that our post-layout optimization step does consider these layout-based parasitics.

To optimize a given unplaced/unrouted circuit, we use Agilent's Advanced Design System (ADS) engine to perform non-linear optimization. The basic idea is that during the optimization process, the parasitic element values of all components are fixed while the dominating element values are changing. The optimization process finds the optimal values of dominating elements. For every component with new dominating element value, we replace it using our library. Since the new component has different dominating value, the parasitics are also different in this new component. We then repeat the overall process until the response of the overall design meets our goal or the change in the response is minimal. More specifically, we first fix the parasitic element values and makes the dominating element values as variables for the optimization engine. Next we find the maximum and minimum value for dominating elements of each component based on the available values in library. The optimization engine is then called. Next we update the current solution based on the values (both dominating and parasitic elements) obtained from the optimization engine. The above process is repeated while the maximum change in dominating element values is below a threshold or the maximum number of iterations is reached.

IV. Placement and Routing

The main objective of our placement and routing step is to find good candidate layouts which are optimized for area, wirelength, and routability. From a given candidate placement solution, we actually perform routing to accurately decide whether the given placement is routable. Since the routing resource is restricted to two metal layers, and the wires and vias add significant parasitics to the overall design, wirelength and routing completion are very important goals. In addition, the area objective also play an important role in determining the overall wirelength as well as coupling among the components.

The ultimate goal in our embedded passive layout is to meet the desired goals in terms of frequency responses, which can be judged by a circuit simulator such as ADS or EM simulator such as SONNET. However, layout optimization using these tools is extremely time-consuming if not impossible. Thus, we sample "good initial layouts" that are optimized in terms of area, wirelength, and routability, and then choose the best one out of these using ADS as the verification engine. As discussed in Section II-B, we save the K_1-best layouts based on area, wirelength, and routability objectives. For each of the K_1-best layouts, we derive the circuit model and evaluate using ADS. The goal is to select K_2-best layouts that achieve the responses

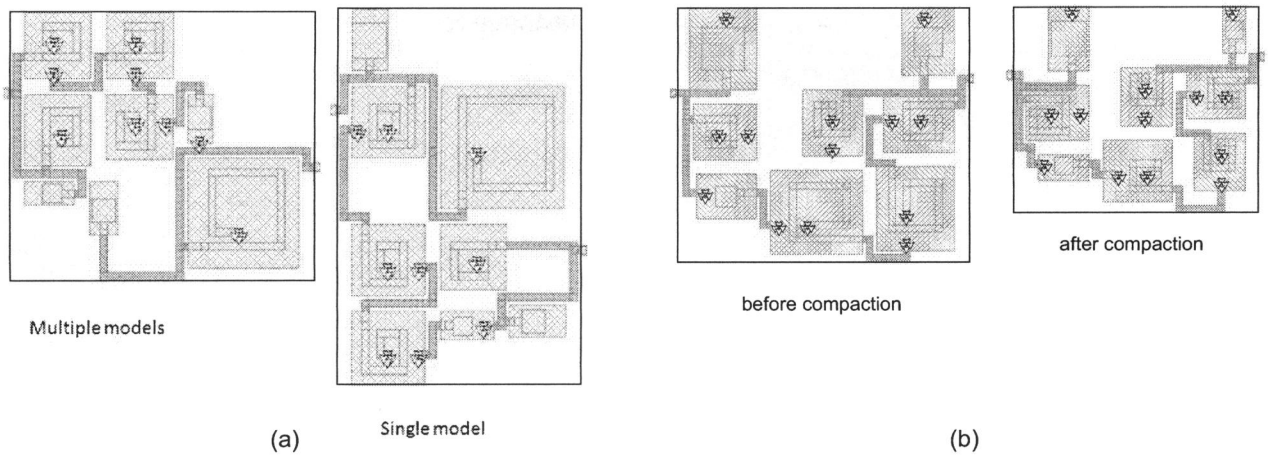

Fig. 1. (a) impact of multiple shape and pin location consideration, (b) impact of post-layout resizing and compaction. Both techniques reduce the overall layout area significantly. The frequency responses were almost identical.

that are closest to our goal. Lastly, for each of the K_2-best layouts, we perform non-linear circuit optimization again using ADS for the entire layout. The components and wires are again re-sized during this step so that the overall circuit response best meets our goals. The layout that closely matches our goal and is the smallest becomes our final solution.

The dimensions of each component is obtained from our library based on their optimized dominating/parasitic element values. The placement is obtained and optimized using the well-known Sequence Pair [4] combine with Simulated Annealing. Routing is performed on each candidate placement solution, which is based on the well-known maze routing [5]. The main objective of this phase is to route all nets and reduce the overall wirelength. The nets are routed in the order of their decreasing weights, where the weight of a net is equal to the number of pins in the net. This method focuses on hard-to-route nets first.

Given a target inductance/capacitance value, there may exist multiple layout geometries that correspond to the required inductance/capacitance values. Efficient use of these various possible geometries may help reduce both area and wirelength of the overall layout. Given a capacitance value cap_j with A_j as its area, there may exist multiple rectangular shapes with the same area and same capacitance values. In case of inductors, the actual inductance value is dependent not only on the overall rectangular shape but on other parameters such as the number of turns, total wirelength, spacing between the turns, etc. Thus for a given inductance value, there may exist several possible inductor layouts which can meet the required specifications. In addition to the basic shapes of the capacitors and inductors, the location of the pins along the boundary may play an important role in terms of wire parasitics. In some cases, having pins on the same boundary of a capacitor or inductor is more beneficial to the overall layout than having them on the opposite side.

In order to optimize our layouts while considering components with different shapes and pin locations, we modify our simulated annealing engine as follows. During the simulated annealing process we keep a list of component layouts which corresponds to the required inductance and capacitance value. We add two new types of perturbation moves called *swap_shape* and *swap_pin*. In case of *swap_shape* we choose a new dimension for the selected component, whereas in case of *swap_pin* we choose a new component having pins in different locations. During the annealing process *swap_shape* is given higher priority at higher annealing temperature, whereas *swap_pin* is given higher priority during lower annealing temperature. Figure 1(a) shows an illustration of the impact of multiple shape and pin location consideration.

V. Post-layout Optimization

The goal of the place and route phase was to minimize the parasitic effects of interconnect so as to produce candidate solutions which may be close to the desired circuit response. However, we note that the layout obtained from the placement and routing stage does not usually meet the desired. This occurs because of the considerable amount of (i) component parasitics, (ii) parasitics added due to interconnects and vias, and (iii) coupling among components and interconnects. The idea of post-layout optimization is to choose new components and their layouts such that the desired goals are achieved considering the parasitic effect of interconnects. This process usually introduces changes in the overall layout, and we attempt to keep the change small so that the overall structure and quality of the layout are preserved.

We perform post-layout optimization by using circuit models to represent the entire layout and then optimize it using ADS to obtain new component values which meet the desired goals. Since the initial layout is given, this circuit model not only includes the individual component-level models but also the interconnect wires, vias, and coupling information among wires and components. Such a circuit representation is not highly accurate but shows high fidelity and matches the response of a given layout closely. The use of circuit models is necessary since using a full wave EM-solver to optimize a given layout can be prohibitively time-consuming.

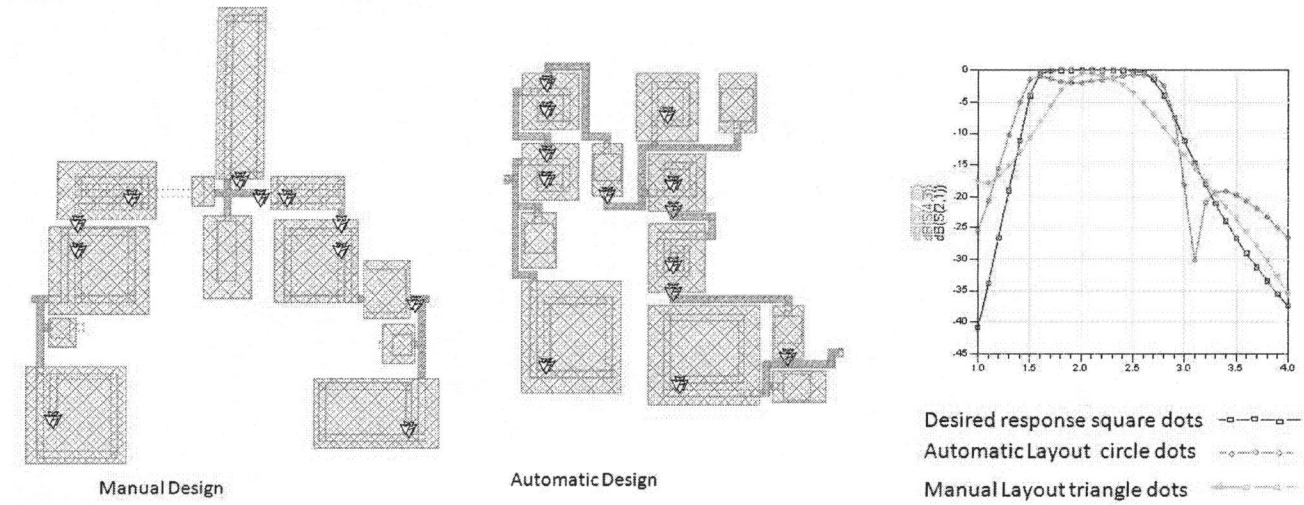

Fig. 2. Frequency response. The line with square, circle, and triangle respectively denote the desired, SONNET, and ADS response.

ADS-based circuit optimization causes the components to change their dominating element values, which in turn change the shapes. In order to prevent any drastic change in the layout during this resizing process—which may damage the initial placement and routing solutions—we perform the post-layout optimization in two steps. During the first step, we impose no restriction on the size of resized components. The new component sizes obtained may degrade the initial routing solution, so we perform placement compaction and rip-up-and-reroute on the affected nets. In this case, the relative position among the components in the placement remains fixed, but only the component dimensions and routing change. During the second step, we ensure that a given routing solution does not change due to component resizing, which is achieved by adding restrictions on the allowed values for component resizing. The maximum allowed size for each component during optimization is chosen such that it does not alter the routing solution. In this case, only the connection from the core of the component to the pins located on the boundary will change. This minor change in the intra-component layout sometimes help improve the overall quality of the design. In both steps of the post-layout optimization, the size of each component typically reduces. Our post-layout optimization plus re-place and re-route basically performs layout compaction, where the whitespace among the components is removed, causing the overall layout are to reduce. Figure 1(b) shows an illustration of the impact of post-layout resizing and compaction.

VI. Experimental Results

We implemented our algorithms in C++/STL and ran our experiments on a linux PC running at 3GHz. We ran our algorithm on a bandpass filter with 12 components. The response of the final layout for each circuit obtained was found by running SONNET on the final layout. In Figure 2, we first show the manual layout done by an expert designer. The overall layout looks very much like the initial circuit-level topology. We also show the automatically generated layout, which is about 44% smaller. It took 15 hours for the manual layout and 50mins for the automatic layout. Next, we show the frequency responses of the ideal, manual, and automatic solutions. One can see that all three responses show similar band-pass behavior. Therefore, we conclude that our automatic layout approach generates solutions that is highly compacted and closely match the desired response within a fraction of the time typically needed in manual design.

VII. Conclusion

In this paper we described a methodology for automatic layout generation of RF embedded passive circuits. We made use of circuit models to optimize layouts and performed non-linear optimization at various stages of the methodology to obtain the desired goals. Full-wave EM simulations is completely out of the design loop, so our methodology significantly reduces the design time.

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