A Study of IR-drop Noise Issues in 3D ICs with Through-Silicon-Vias

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***Abstract*—With the extensive research on through-silicon-via (TSV) and die-stacking technology from both academia and industry, mainstream production of 3D ICs is expected in a near future. However, power delivery is believed to be one of the most challenging problems in 3D ICs. A main objective of the 3D power/ground (P/G) network optimization is to minimize the usage of P/G TSVs while satisfying power supply noise constraint. P/G TSVs consume a considerable amount of routing resources unless designed carefully. In this work, we first investigate the impact of P/G TSVs on the power supply noise as well as 3D IC layouts. We perform sign-off static IR-drop analysis on GDSII layouts of 2D and 3D IC designs using commercial-grade tools. We also explore the impact of 3D P/G network topology on IR-drop by varying P/G TSV pitch. Next, we propose a non-regular P/G TSV placement algorithm to further reduce the number of P/G TSVs used while satisfying the given IR-drop noise requirement. Compared with the conventional regular structure, our non-regular P/G TSV placement algorithm reduces the P/G TSV count, wirelength, and footprint area by 59.3%, 3.4%, and 3.5% on average, respectively.**

I. Introduction

Three-dimensional (3D) system integration has emerged as a promising technology to continue Moore's law beyond the conventional 2D ICs. Through-silicon-via (TSV) is a key enabler for 3D integration, which provides vertical interconnections between stacked dies. Using 3D integration with TSVs, the average and the maximum wirelength between different dies as well as within a same die can be significantly reduced compared to 2D ICs. The shorter wirelength further indicates improvement in performance, power, and foot print area. Although TSVs can improve wirelength, performance and area, they occupy non-negligible silicon area. Excessive or ill-placed TSVs not only increase die area, but also have negative impacts on these objectives in 3D ICs [1].

Power delivery is believed to be one of the biggest challenges in 3D stacked ICs. With the rapid advance of fabrication technology and increase in number of gates in unit chip area, power consumption of a chip increases. As multiple dies are stacked together into a smaller footprint, delivering current to all parts of the 3D stack while meeting the power noise constraints becomes highly challenging. This is mainly because the number of TSVs available for power/ground (P/G) nets is limited, causing severe routing congestions if many 3D connections are desired [2]. In this work, we explore IR-drop noise problems in 3D ICs with TSV based on GDSII layouts.

Our main contributions are as follows. First, we investigate the impact of P/G TSVs on the IR-drop noise as well as 3D IC layouts, and traditional layout-related metrics such as wirelength and footprint area. We perform IR-drop noise analysis on 2D and 3D IC GDSII layouts using existing 2D commercial grade tools. We show how to extend 2D commercial tools to handle TSVs and 3D die stacking during layout generation. We also explore the impact of 3D P/G network topology on IR-drop. P/G TSVs are inserted in a regular fashion (conventional 2D-array style) for flip-chip bonding and the pitch of both P/G TSVs and P/G bumps are assumed to be same. We vary P/G TSV pitch from 150um down to 50um to examine its impact on IR-drop as well as layouts. Finally, we propose a non-regular P/G TSV placement algorithm to further reduce the number of P/G TSVs used while achieving the given IR-drop noise requirement. The results from both conventional regular and non-regular P/G TSV placement are compared in terms of IR-drop noise, P/G TSV count, and other metrics such as wirelength and footprint area.

II. Existing Works

In general, the objective of P/G TSV optimization is to minimize power noise with minimum number of P/G TSVs. Previous works on 3D power delivery networks employed regular P/G TSV placement or optimized the density of P/G TSVs in each P/G tile to meet power noise requirement.

A physical model of 3D power distribution network is presented in [3]. Their model assumed that power is fed from the package through power I/O bumps distributed over the bottom-most die and travels to the upper dies using TSVs and solders. Therefore, P/G TSV locations are predetermined by regularly placed power I/O bumps. Three different TSV topologies for 3D P/G network have been explored in terms of power integrity in [4]; (1) a large single TSV aligned to a C4 bump, (2) multiple TSVs around a C4 bump, (3) and evenly distributed TSVs throughout a die. Again, density and location of P/G TSV were predetermined.

It is shown that 3D die stacking has a higher impact on IR-drop than Ldi/dt noise [5]. 3D stacking inherently increases the resistance of a 3D P/G network due to P/G TSVs which directly impacts IR-drop. On the other hand, Ldi/dt noise due to time varying activities in the modules is caused by

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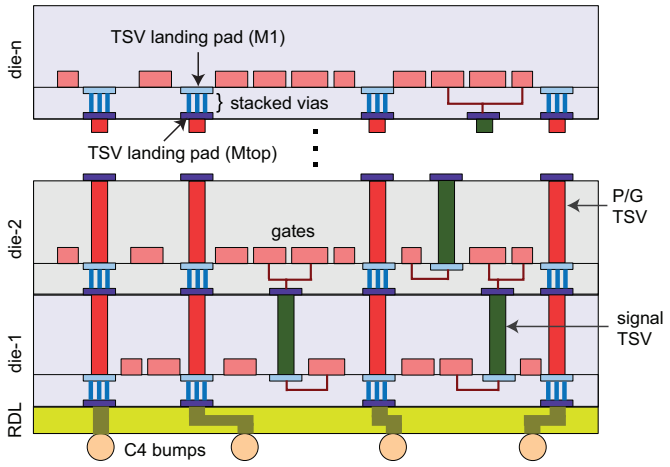

Fig. 1. Target 3D structure with via-first TSVs. P/G TSVs are vertically connected with stacked local via arrays.

dominant off-chip inductive components. They also examined the effects of P/G TSV spacing as well as C4 bump spacing on power noise. However, these approaches also assumed regularly placed P/G TSVs with predefined density.

A simultaneous TSV optimization scheme for both power and thermal integrity is proposed in [6]. They first divide each die into N tiles and define possible TSV placement density. Depending upon the power and thermal noise level in each tile, a minimum TSV density pattern is selected. However, this work only considers noise in P/G planes in the package without considering on-chip power supply routing.

III. P/G TSV Impacts on 3D IC Layouts

Our target 3D structure is illustrated in Figure 1. We assumed adjacent dies are bonded in a face-to-back (F2B) fashion. Depending on their type, via-first TSVs interfere with a device layer, whereas via-last TSVs, which pierce through all stacked dies, interfere with both device and metal layers. In our work, both P/G TSVs and signal TSVs are via-first type assuming only one type of TSV is preferable in a manufacturing process. Thus signal TSVs affect a device layer and top-most and bottom-most metal layer, i.e. M1 and M6 in 130nm technology using six metal layers. However, P/G TSVs are routed through stacked local vias in each die as shown in Figure 1, hence affect metal layers as well as device layer in a similar way as via-last TSVs. Thus, P/G TSVs cause severe routing congestions if many 3D connections are required. Note that power C4 bumps are connected to P/G TSV landing pads at M6 using redistribution layer (RDL).

Figure 2 shows a part of signal net routing result of M5 and M6 for a FFT circuit (256 point and 8-bit precision) using commercial grade tool, i.e. Cadence SoC Encounter. We placed P/G TSVs regularly with $50\mu m$ pitch on top of P/G bumps in this design. This figure clearly shows that not only the space that P/G TSVs occupy, but space between P/G TSVs are not fully exploited for signal net routing, hence causes more severe routing congestions than expected. In the case of M6 (yellow), wires are routed in vertical direction, and space

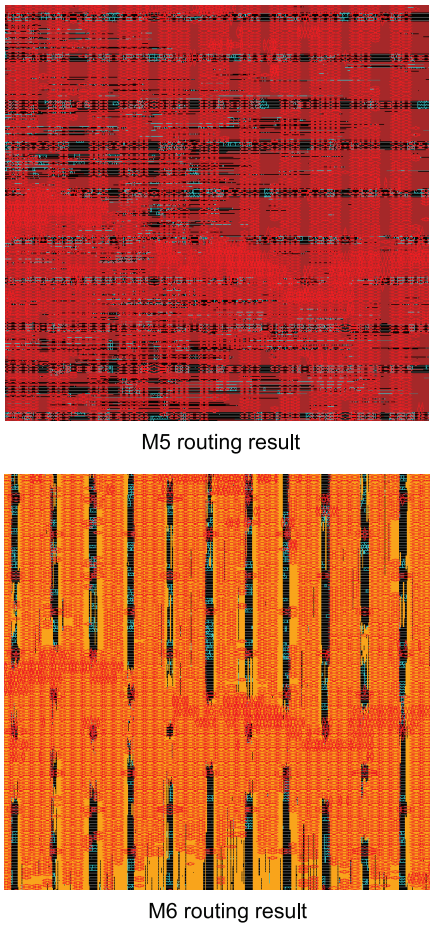

Fig. 2. Routing congestion in M5 and M6 due to regularly placed P/G TSVs

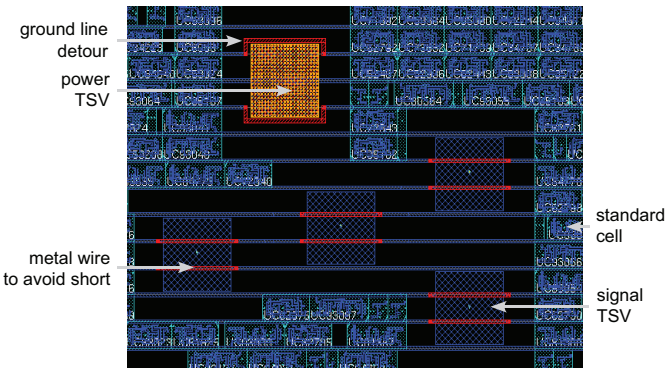

Fig. 3. Power distribution network layout. Additional routing resources are needed for P/G net to detour P/G TSVs and signal TSVs.

between P/G TSVs in vertical direction is not used well since horizontal space between P/G TSVs limits the routing capacity for vertical M6 wires. This phenomenon mostly occurs in higher metal layers which are typically used for long signal net connections. It is possible that regularly placed P/G TSVs make a bottleneck for long wires to route. This might cause wirelength increase and performance degradation. If routing space is not enough, foot print area needs to increase to mitigate routing problems.

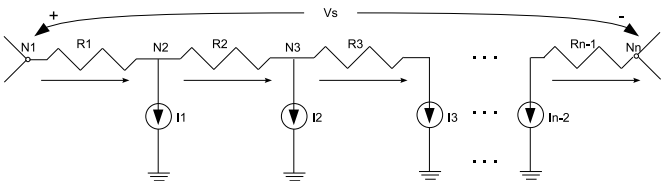

Fig. 4. Series resistor chain in P/G network

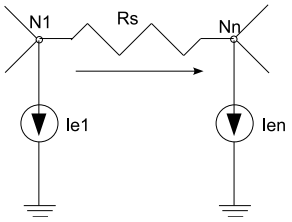

Fig. 5. Series resistor equivalent circuit

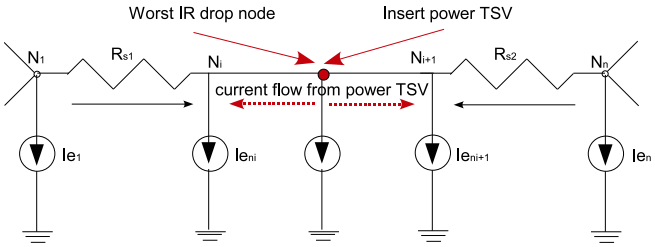

Fig. 6. Boundary voltage and current change due to P/G TSV insertion

A P/G net routing for standard cell rows also becomes challenging. Figure 3 shows a part of P/G net routing result for the same FFT circuit. As P/G TSV size becomes larger than a standard cell height, it is inevitable that single power (ground) TSV also covers the region that ground (power) nets are supposed to be routed. Therefore, power (ground) nets should detour ground (power) TSVs to avoid short between power and ground, which is an additional source of routing congestion. Moreover, P/G nets should also avoid short with an M1 landing pad of a signal TSV. Thus, P/G net routing in 3D ICs consumes more routing resources compared to 2D ICs, hence reduces available routing resources for signal net routing.

These observations call for P/G TSV count reduction. In a chip design phase, we can estimate power consumption profiles based on simulations and power library for standard cells and macro blocks. Thus, it is possible to identify the region that consumes more power and demands more current accordingly than other regions. These high power consuming locations are susceptible to IR-drop noise violation. If IR-drop noise is estimated accurately based on the given power profile, we can identify the power noisy spots. By placing P/G TSVs more in these power noisy spots than other regions, we can efficiently reduce IR-drop noise while using minimum number of P/G TSVs as well as saving routing resources compared to conventional regularly placed P/G TSVs.

IV. Non-Regular Power/Ground TSV Placement Algorithm

A standard cell based design is used in this work. P/G rings are routed on the periphery of circuits and P/G stripes which provide power and ground for each standard cell are routed horizontally. Therefore, we can build a series resistor chain along P/G stripes with current sources, which represents standard cells, based on a given circuit layout and a power profile. IR-drop noise estimation is performed on this resistive circuit. To handle large circuits with millions of nodes, we adopt an equivalent circuit modeling method [7], [8]. Our P/G TSV placement algorithm is applied to this simplified P/G network to obtain the optimal P/G TSV locations.

A. Equivalent Circuit for Series Resistors

Consider a series resistor chain in the P/G network in Figure 4. There will be some voltage V_s, between the two series ends, N_1 and N_n. Conceptually, a voltage source with V_s can be added between the nodes N_1 and N_n without disturbing the network. Suppose the positive current direction for resistive branch R_i is from N_i to N_{i+1}. Superposition can be applied to this network to produce equivalent circuit shown in Figure 5, where the positive current direction of R_s is from N_1 to N_n. The equivalent resistor R_s is just the sum of all the resistors in series.

$$R_s = \sum_{i=1}^{n-1} R_i \tag{1}$$

Superposition can be used to determine how the current from each current source divides between the two ends. All current sources except the one in question are replaced by open circuits, while the voltage source between nodes N_1 and N_n is replaced by a short circuit. The resulting system is a simple current divider, and the additional current at N_1 and N_n is sum of all the divided currents. The equivalent current I_{e_1} and I_{e_n} can be calculated as follows [7], [8]:

$$I_{e_1} = \sum_{i=1}^{n-2} \frac{\sum_{j=i+1}^{n-1} R_j}{R_s} I_i \tag{2}$$

$$I_{e_n} = \sum_{i=1}^{n-2} \frac{\sum_{j=1}^{i} R_j}{R_s} I_i \tag{3}$$

Once the network has been solved with the equivalent series circuit and the voltages at the end nodes are known, the intermediate node voltages and currents are calculated based on superposition as follows:

$$V_{i+1} = V_i - \frac{R_i}{R_s} V_s - R_i I_{e_i} \tag{4}$$

$$I_{e_i+1} = I_{e_i} - I_i \tag{5}$$

B. Equivalent Circuit modeling for P/G TSV placement

The equivalent circuit modeling method was originally developed for the fast P/G network simulation [8]. To apply this method for our P/G TSV placement algorithm, we have to take into account following differences:

1) In a series resistor chain circuit, not all the node voltage information need to be considered for possible P/G TSV placement location. We only need to examine the nodes whose voltages are the local minimum (worst IR-drop) or the local maximum (worst ground bounce). This means that these local maximum and local minimum voltage nodes cannot be suppressed, since these nodes are required to maintain the node voltage information. Thus, other nodes except these local minimum and local maximum can be simplified with two current sources and one resistor as shown in Figure 5. Since each power (ground) stripe in a design will have a single local minimum (maximum) node, each P/G stripe will be divided into two sub-chain circuits. Currents will flow in the same direction in each sub-chain and we only need to consider the voltages at two ends.
2) When we insert P/G TSVs in the worst IR-drop node, the current flow direction is changed in affected P/G stripes. Even though the total current demands for these P/G nets are unchanged, current direction is altered with additional current flow from P/G TSVs. Therefore, the local minimum or the local maximum nodes in these P/G stripes are changed; hence node voltages in these stripes should be updated.
3) Inserting P/G TSVs in some P/G stripes not only changes node voltages at these P/G stripes, but also alters the boundary voltages and currents at the ends of these P/G stripes, which will affect the boundary voltages and currents for other P/G stripes. Figure 6 shows a simple example. Before inserting a power TSV, currents are flowing inwards to the worst IR-drop node. After inserting the power TSV, the amount of current flowing from both ends will be reduced depending upon the amount of current that power TSV provides. This will change the amount of current that outer power ring supply, hence IR-drop through the power ring and the boundary voltages and currents in adjacent power stripes will be changed as well.

C. Non-regular P/G TSV Placement Algorithm

We construct P/G resistive network based on the detailed cell placement results along with a power profile for each stacked die. Then, we calculate IR-drop noise based on Kirchhoff's voltage law (KVL) and current law (KCL), and identify the local minimum and the local maximum node voltages for power and ground net respectively. With this information, we build the simplified circuit to handle large size circuits efficiently using the equivalent circuit model. Next, P/G TSVs are inserted where IR-drop constraint is violated, and IR-drop is re-evaluated using equivalent circuit model. If the current design with P/G TSVs inserted meets the target IR-drop threshold, the P/G TSV placement algorithms finishes. If not, we insert additional P/G TSVs to the current IR-drop violating regions. The flow chart of P/G TSV placement algorithm is shown in Figure 7.

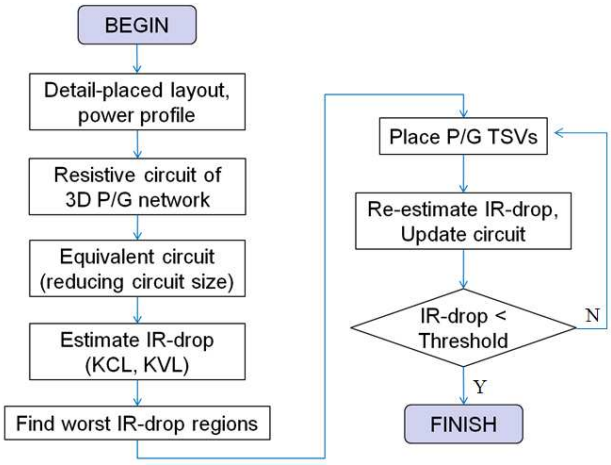

Fig. 7. Flow chart of non-regular P/G TSV placement algorithm

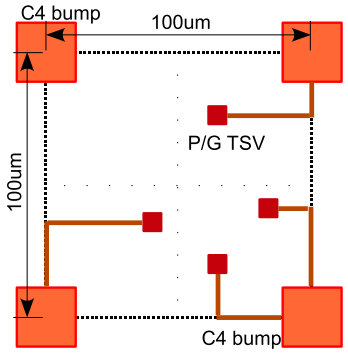

Fig. 8. P/G TSVs are routed to the nearest C4 bump using RDL.

The algorithm first constructs 2D P/G network for each die separately. Based on a given power profile, the amount of current that each gate requires is computed, in our case power consumption values of each gate is divided by the nominal power supply voltage 1.5V, and then every gate is replaced by a corresponding current source. Wire resistance between adjacent gates is calculated by their relative distance and the resistivity of that wire segment. We first assume that P/G bumps are available above P/G rings on the periphery with a predetermined pitch and P/G TSVs are inserted for these locations for 3D P/G connections, which do not affect routing resources in a core region. Then, we calculate the total current demand for each P/G net, and compute boundary voltages and currents at both ends of P/G nets. When we compute the vertical current flow between dies and IR-drop through P/G TSVs, it is assumed that P/G TSVs supply current to the nearest P/G nets. Based on these boundary conditions, each node voltage in 3D P/G nets is estimated by using KVL and KCL. Then, we can identify the worst IR-drop nodes and

TABLE I
BENCHMARK CIRCUITS

Circuit	# gates	# signal TSVs	TSV coverage (%)	Placement density (%)	Clock frequency (MHz)	Profile
FFT1	200K	794	8.9	77.4	200	256 point 8 bit precision
FFT2	405K	1397	8.2	77.3	142	256 point 16 bit precision
FFT3	910K	7089	16.3	77.2	111	512 point 16 bit precision

simplify circuits using equivalent circuit model.

Based on the IR-drop estimation, we insert P/G TSVs where IR-drop exceeds the constraint. Since we perform our algorithm based on a detailed placement result, it is desirable to minimize the change to a design layout. Since signal TSVs are already placed at the locations to improve wirelength and timing objective, we avoid overlaps between signal TSVs and P/G TSVs. If an optimal P/G TSV location overlaps with gates, we move these gates to nearest white spaces using a Cadence SoC Encounter's place refinement. We also consider IR-drop from a C4 bump to a P/G TSV. We assume P/G redistribution layer (RDL), where C4 bumps and P/G TSVs are routed, exists using the top-most metal layer. We further assume that a P/G TSV is routed to the nearest C4 bump only, and that each C4 bump is an ideal voltage source shown in Figure 8.

With inserted new P/G TSVs, node voltages that are attached to P/G TSVs are evaluated again and the simplified circuit is updated. Then, whole worst IR-drop nodes are computed based on new boundary conditions. At this phase, we use the simplified circuit to reduce a computational time. Then, we check whether IR-drop constraint is met for all stacked dies. If the first run is unsuccessful, we insert P/G TSVs at the current worst IR-drop nodes that violate IR-drop constraint, and recalculate IR-drop. We perform iterative P/G TSV insertions until IR-drop constraint is achieved for all dies.

D. Validation

To validate our IR-drop estimation algorithm, we compare the results for both 2D and 3D IC GDSII layouts using existing 2D commercial-grade tools. Our 3D IR-drop analysis tool is based on Cadence VoltageStorm, which is designed for 2D ICs. We take the following steps to handle 3D designs using VoltageStorm:

1) We modify the interconnect technology file (ICT), which contains information on all layers (device layer, dielectric layer, metal layer, vias, and TSVs) and their relative position and resistance values, to model our two die–stacked configuration.
2) We create a 3D technology file (TCH), which contains resistive and capacitive information for all and between layers, using Cadence Techgen.
3) We generate a 3D library exchange format (LEF) file so that layers and gates in different dies can be distinguished by the tools. For example, M1 in top-most die and M1 in bottom-most die should be differentiated so that 2D tools distinguish these M1 layers
4) Power consumption data and layer mapping files, which maps design to appropriate LEF and GDS layers, are modified as well to be used for different dies accordingly.
5) Finally, we create a 3D design exchange format (DEF) file from the final layout of each die to form a single 3D design. After all these preparations are ready, we can run 3D IR-drop analysis on this combined design using Cadence VoltageStorm.

TABLE II
EXPERIMENT SETTINGS FOR TSV

Item	
TSV Diameter (μm)	6
TSV Landing Pad (μm)	10
TSV Keep Out Zone (μm)	6.225
TSV Cell Size ($\mu m \times \mu m$)	18.45×18.45
TSV Height (μm)	30
TSV Resistance ($m\Omega$)	30

Using our IR-drop estimation method, we were able to match both 2D and the two die-stacked 3D IR-drop results from the VoltageStorm within 7% error. Our computed resistance value based on the ICT file for each P/G wire segment overestimated by 6% compared to VoltageStorm. Since this is deterministic error, resistivity value is tuned to match the results. Due to the tools limitation on number of layers it can process, we validated our algorithm up to two die-stacked 3D ICs.

V. EXPERIMENTAL RESULTS

The proposed non-regular P/G TSV placement algorithm has been implemented in C programming language. The experiments were performed on a 64-bit Linux server with two quadcore Intel Xeon 2.5GHz CPUs and 16GB main memory. We use four FFT circuits for our analysis. All circuits are synthesized using Synopsis Design Compiler with the physical library for the target 130nm technology, and designed using Cadence SoC Encounter to 2D and two die-stacked 3D ICs, which are listed in Table I. The number of signal TSVs was chosen for signal TSVs to cover around 10% of the chip area, and the overall placement density including both standard cells and TSVs is targeted to 80%. Experimental settings for the TSV used in our simulations are shown in Table II, which are similar to the data of manufactured TSVs in [9]. Note that the TSV size is large, which occupies 5 standard cell rows in this setting (a standard cell row height is $3.69\mu m$).

A. IR-Drop Analysis Results for 2D And 3D Designs

We first compare IR-drop analysis results between our 2D and 3D designs. We assume that I/O cells are located on the periphery of a chip, and I/O cell pitch is $100\mu m$. We further assume that 50% of all I/O cells are dedicated to power and

TABLE III
IR-DROP, FOOTPRINT AREA, WIRELENGTH, AND POWER CONSUMPTION COMPARISON BETWEEN 2D AND 3D DESIGNS. THE NUMBERS IN PARENTHESES ARE RATIOS TO 2D

	2D					3D				
Ckt	area ($\mu m \times \mu m$)	WL (mm)	Power (mW)	IR-drop (mV)	# P/G IO cell	area ($\mu m \times \mu m$)	WL (mm)	Power (mW)	IR-drop(mV) (top/bot)	# P/G IO cell / P/G TSV
FFT1	2271×2271	13018	845	178	42	1744×1744 (0.59)	14780 (1.14)	839 (0.99)	175 / 157	34 / 170
FFT2	3243×3243	32197	1240	217	62	2412×2412 (0.55)	35772 (1.11)	1246 (1.00)	226 / 200	46 / 230
FFT3	4754×4754	67495	2120	304	94	3851×3851 (0.65)	85405 (1.27)	2162 (1.02)	314 / 310	74 / 370

ground connections. In this section, P/G TSVs are inserted only on the periphery of a chip where I/O cells locate. In our 3D designs, all I/O cells are placed in a bottom die nearest to C4 bumps. P/G C4 bumps are connected to a bottom die through RDL, then P/G TSVs are used to believer power from a bottom die to a top die.

I/O cell density is kept the same for both 2D and 3D designs for fair comparison, and each P/G I/O cell contains 5 P/G TSVs, respectively. The clock frequency for power simulation is set by the slower clock frequency between 2D and 3D designs. Then, statistical power analysis is performed with 0.2 toggle probability for all nets excluding clock nets.

Table III shows IR-drop analysis results of our 2D and 3D designs. We make the following observations. First, the footprint area of 3D is larger than 50% of 2D footprint area mainly because of the large TSV. Second, the total wirelength in 3D design is larger than 2D, again mainly because of the large TSV size [1]. In addition, we still use Cadence 2D placement and routing tools for each die separately, which gave us sub-optimal 3D layout quality. Third, the power consumption is comparable in both 2D and 3D designs. The combined effect of smaller footprint area and larger total wirelength of 3D leads to this comparable power consumption in both 2D and 3D designs. Lastly, the IR-drop is worse in 3D designs compared to 2D designs as circuit size becomes larger. This IR-drop increase in large 3D designs is mainly because the on-chip power delivery resource (P/G I/O cells and P/G TSVs) is less in 3D designs.

B. Impact of 3D P/G Network Topology on IR-drop

The results shown in the section V-A indicate that inserting P/G TSVs only on the periphery of a chip is not sufficient to alleviate IR-drop noise problems in 3D ICs. In this section, P/G TSVs are inserted in a conventional 2D-array fashion for flip-chip bonding. We also vary the P/G TSV pitch from $150\mu m$ down to $50\mu m$ to examine its impact on IR-drop. Most commercial products today have C4 bump pitches around $100\mu m$ to $200\mu m$, however, researchers have demonstrated micro-bumps with pitches below $10\mu m$ [4]. In this experiment, the pitch of both P/G TSVs and P/G bumps are kept same, which is an ideal case for IR-drop noise reduction. The number of P/G TSVs used for different TSV pitch is shown in Table IV.

Figure 9 shows the impact of P/G TSV pitch on IR-drop, power, wirelength, and footprint area. The results are normalized to the baseline 3D design that has P/G TSVs only on the periphery. As the P/G TSV pitch decreases and the available P/G TSVs increase, IR-drop significantly improves up to $100\mu m$ or $75\mu m$ pitch depending on benchmark circuits. With $100\mu m$ P/G TSV pitch, IR-drop improves 60% compared to the baseline design for FFT1.

TABLE IV
NUMBER OF P/G TSVS USED WITH DIFFERENT PITCH. THE NUMBER OF P/G TSVS IN CORE/PERIPHERY IS SHOWN SEPARATELY

Ckt	Peri	$150\mu m$	$125\mu m$	$100\mu m$	$75\mu m$	$50\mu m$
FFT1	0/170	221/170	313/170	481/170	1013/170	2113/190
FFT2	0/230	481/230	685/230	1013/230	2113/230	5725/270
FFT3	0/370	1201/370	1741/370	2665/370	5613/390	14965/430

However, counter-intuitively, as we further decrease the P/G TSV pitch to $50\mu m$ IR-drop noise increases. FFT3 shows even worse IR-drop noise than the baseline design. This is mainly because of the huge TSV size. In our experimental setting, 100 minimum-size inverters can fit into a single TSV area. Previous works did not consider TSV size, thus circuit layouts did not change even though more P/G TSVs are inserted. However, as more P/G TSVs are inserted, more spaces are needed for these P/G TSVs which is shown in Figure 9. As a result, wirelength and power consumption increases as well. These results show that fine P/G TSV pitch in 3D P/G network do not always result in IR-drop noise improvement.

C. Non-regular P/G TSV Placement Algorithm

The results shown in the section V-B indicate that if too many P/G TSVs are used, IR-drop noise does not improve due to increased area and wirelength. In this section, we compare IR-drop analysis results between regularly placed P/G TSVs and our algorithm on two die-stacked 3D designs. We set the 3D design whose P/G TSVs are regularly placed with $100\mu m$ pitch as a baseline, since $100\mu m$ pitch case achieves high IR-drop improvement with less than 3% area overhead. We also set the IR-drop constraint for our algorithm to be the worst IR-drop noise of the baseline. With the P/G TSV locations obtained from our algorithm, we design two die-stacked 3D ICs and validate IR-drop noise using Cadence VoltageStorm.

Table V shows that our algorithm achieves similar IR-drop results within 7% error with much smaller number of P/G TSVs compared to the baseline 3D designs. We were able to save the number of P/G TSVs by 59.3% on average. For instance, FFT3 shows 68.4% reduction in P/G TSV count. It is observed that as circuit size becomes larger, P/G TSV count reduction percentage increases. It is possible that conventional 2D array style P/G TSV placement scheme uses more P/G TSVs than necessary, especially in non-power-noisy spots.

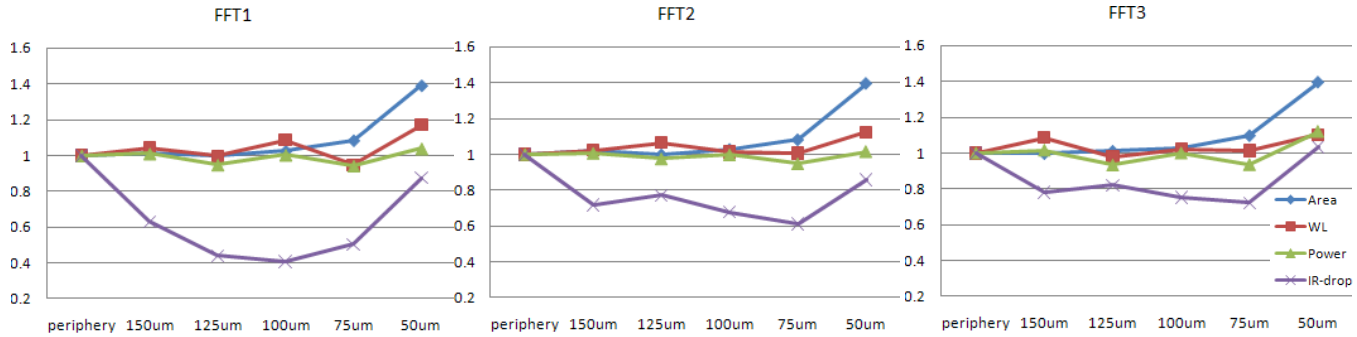

Fig. 9. Impacts of P/G TSV pitch on IR-drop, footprint area, wirelength, and power

TABLE V
COMPARISON OF OUR NON-REGULAR P/G TSV PLACEMENT ALGORITHM AGAINST REGULAR P/G TSV PLACEMENT

	regular P/G TSV ($100\mu m$ pitch)				ours					
Ckt	# P/G TSV (core/peri)	Area ($\mu m \times \mu m$)	WL (mm)	IR-drop (mV)	# P/G TSV (core/peri)	Area ($\mu m \times \mu m$)	WL (mm)	IR-drop (mV)	IR-drop % error	runtime (sec)
FFT1	481 / 170	1776×1776	16056	71	160/170 (49.4% ↓)	1744×1744 (2.6% ↓)	15028 (6.4% ↓)	75	5.6	2.63
FFT2	1013 / 230	2444×2444	36240	153	266/230 (60.0% ↓)	2402×2402 (3.5% ↓)	35152 (3.1% ↓)	148	3.3	6.76
FFT3	2665 / 370	3902×3902	87289	236	592/370 (68.4% ↓)	3821×3821 (4.2% ↓)	86507 (1.0% ↓)	251	6.4	16.44

If an accurate power profile is available in a design phase, the number of TSVs for 3D P/G network can be reduced significantly. With the reduced number of P/G TSVs, footprint area and total wirelength are reduced by 3.4% and 3.5% on average, respectively.

VI. CONCLUSION

In this work, the impacts of P/G TSVs on IR-drop noise as well as 3D IC layouts are explored. Due to the large size of TSVs, both signal and P/G net routing in 3D IC becomes challenging. Experimental results show that increasing the number of P/G TSV beyond certain level could worsen IR-drop noise because of a large TSV size. The non-regular P/G TSV placement algorithm is proposed to minimize the number of P/G TSV used while satisfying IR-drop noise constraint. Experimental results show that our non-regular P/G TSV placement algorithm reduces the number of P/G TSVs by 59.3% as well as footprint area and wirelength compared to the conventional regular P/G TSV placement scheme.

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