A Fine-Grained Co-Simulation Methodology for IR-drop Noise in Silicon Interposer and TSV-based 3D IC

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***Abstract*—In this paper, we propose a methodology which can co-simulate IR-drop noise for 3D IC, silicon interposer, and PCB simultaneously, and demonstrate how severe the IR-drop is in the silicon interposer. This methodology uses not only PCB and package (silicon interposer) stacking information, but also full transistor-level 3D IC switching information for a precise IR-drop calculation. By utilizing these information, we show the IR-drop noise map of the PDN (Power Distribution Network) in the interposer and the 3D IC mounted on it. Based on our results, we found that (1) the IR-drop noise caused by silicon interposer is very severe to few tens of mV, and (2) our co-analysis method fixes the overestimation of IR-drop caused by the traditional method.**

***Index Terms*—IR-Drop; Co-Simulation; Co-Analysis; 3D IC; Silicon Interposer; Chip; Package; PCB;**

I. Introduction

Recently 3D IC and interposer technologies have emerged as two leading contenders for high speed, large-scale integration platform. 3D ICs using TSVs (Through Silicon Via) have already been reported [1], and silicon interposer-based commercial product has also been proposed [2]. However, power delivery issue in silicon interposer has not been fully addressed yet. Silicon interposer uses a very thin metal due to process issues. Compared with an FR4 package, this is less than 10% of the metal thickness used there. What makes it harder to design PDN (Power Distribution Network) in silicon interposer is that it can only use wide metal lines limited to few tens of μm. It does not allow to design large metal planes for PDN while other packaging substrates support it easily. Thus, silicon interposers can cause a high IR-drop noise in the PDN, and this can in turn affect power delivery to the 3D IC mounted on it. In order to accurately calculate the overall power delivery noise in the whole system, it is necessary to simulate the 3D IC, interposer, and PCB in a holistic fashion.

There have been several works related to the co-analysis of chip-package and PCB. However, to the best of knowledge, there is no work that performs co-analysis of package, PCB, and a full transistor switching activity of 3D IC. [3] modeled PDN into small S-parameter blocks and connected them to obtain the whole PDN information of the system. However, it was only possible for periodic structures. [4] suggested to combine Laguerre Polynomials with the FDTD method to analyze the system PDN, but it had limits on simulating a very complicated PDN inside the IC due to different aspect ratio between IC and package. [5] presented a co-simulation on DDR3 DRAM. However, power details inside the IC were not provided.

In this paper, we first discuss how severe the IR-drop noise is in silicon interposers. Then, we present our co-analysis methodology which calculates the IR-drop noise of the whole system with full transistor level power information details. We demonstrate the IR-drop results of a system, when silicon interposer is an alternative to the organic packages. The major contributions of this paper are as follows: 1) This is the first work to co-simulate a system with 3D IC and silicon interposer at a very fine-grained level. 2) We propose a methodology to co-simulate IR-drop with full package (silicon interposer), full PCB, and full transistor level 3D IC power information. 3) We specifically demonstrate the power delivery noise severity in silicon interposer.

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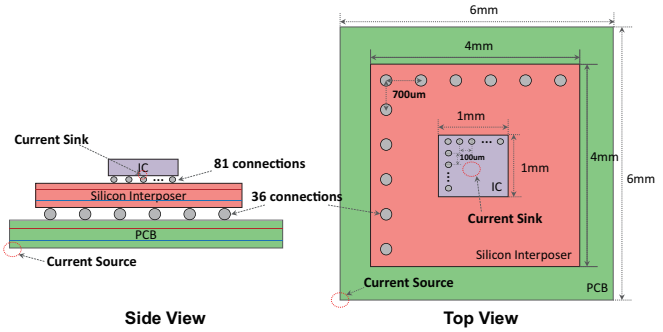

Fig. 1. Side view and top view of the system simulated for IR-drop noise.

II. IR-drop Noise in Silicon Interposer

In this section, we discuss the impact of IR-drop noise on silicon interposer. Here, we design a system which has an IC, an interposer and a PCB, with the dimensions and details described in Figure 1. Due to the process issues, the width and thickness of the metal inside the interposer are limited. Here, we assume a silicon interposer which has the metal thickness of 1μm, maximum width of 50μm, and minimum spacing of 50μm for PDN design. We also assume that our interposer has TPV (Through Package Via) in the height of 100μm and diameter of 20μm. The die size of the IC is 1mm $\times$ 1mm, silicon interposer 4mm $\times$ 4mm, and PCB 6mm $\times$ 6mm (metal thickness: 36μm). 81 power pins are distributed between IC and interposer in 100μm pitch, and are connected with 30μm diameter C4 bumps. The system has 36 solder ball connection between the interposer and the PCB, and is distributed in 700μm pitch. Total power is 1027mW, and 933.6mA flows through the system. One current sink was assigned at the middle of the IC model for worst case analysis.

Figure 2 shows the results. We used Ansoft Siwave to simulate our system, and see that 17.08mV IR-drop noise occurs on the interposer and PCB, while an organic package (metal thickness: 18μm) and PCB shows less than 2.3mV of IR-drop. However, the maximum IR-drop generated by PCB is only 0.8mV. Thus, compared with the packages, we can see the IR-drop on silicon interposer is not negligible.

III. Interposer-3D IC Co-Simulation Methodology

In this section, we describe the details of our co-simulation methodology. We use Synopsys PrimeRail to do the co-simulation. The design and modeling process diagram is shown in Figure 5, and the full details are described in the following subsections.

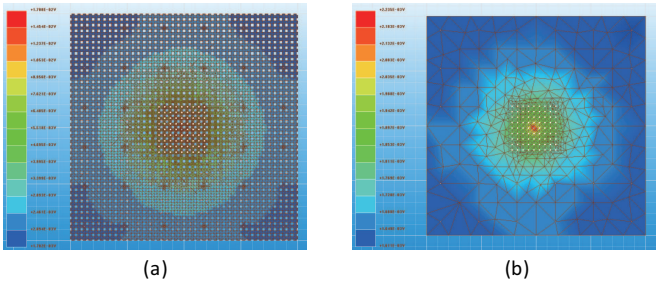

Fig. 2. IR-drop Noise on (a): Si-interposer (17.08mV), (b): Organic package (2.24mV).

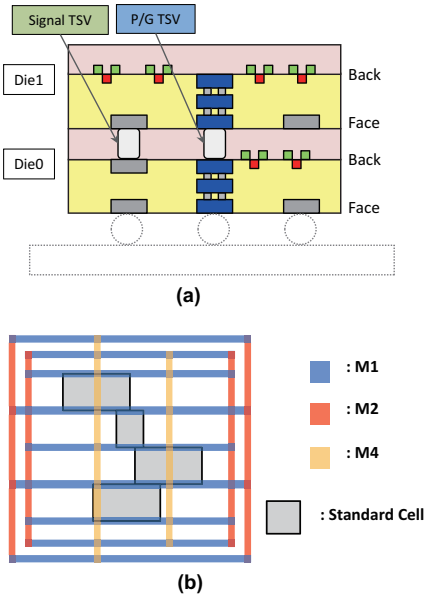

Fig. 3. Details of the 3D IC PDN design (a): Stack information of the two tier 3D IC, (b): PDN design on the 3D IC.

A. 3D IC PDN Modeling

To perform co-simulation of the whole system, we first need to design the PDN of IC. Our design is a two tier 3D IC which has face to back configuration as shown in Figure 3(a). A ring PDN is designed using M1 and M2. M1 is also used to supply power in each standard cells, and M4 were used to support the vertical path. Details of the on-chip PDN are shown in Figure 3(b). Nangate 45nm technology was used for our design. VDD is 1.1V, and TSVs in the 3D IC design has diameter of 5μm and height of 60μm.

B. Interposer and PCB PDN Modeling

For silicon interposer, PCB, and other interconnects, we re-use the design we have made in chapter II (Figure 1). To model the PDN of silicon interposer and PCB, we use unit cell based SPICE method in [6]. Off-chip PDN design (interposer, PCB) could be split into array of unit cells like Figure 4. Each unit cell describes a cluster of SPICE elements, and by connecting these together, the whole PDN can be reconstructed. Figure 4 shows a unit cell of 4×4 array, but other grid sizes are also possible, and this method can also be applied to irregular shaped PDNs. Each unit cell of silicon interposer, and PCB PDN represents 100μm × 100μm. The resistance of each unit cell were extracted using Ansoft Q3D Extractor. C4 bumps, TPV of interposer, and solder bump models were also made. SPICE values

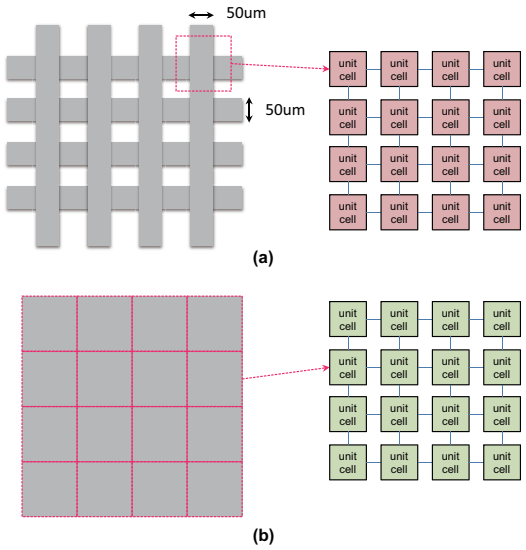

Fig. 4. PDN modeling using unit cell model (a): Silicon interposer, (b): PCB.

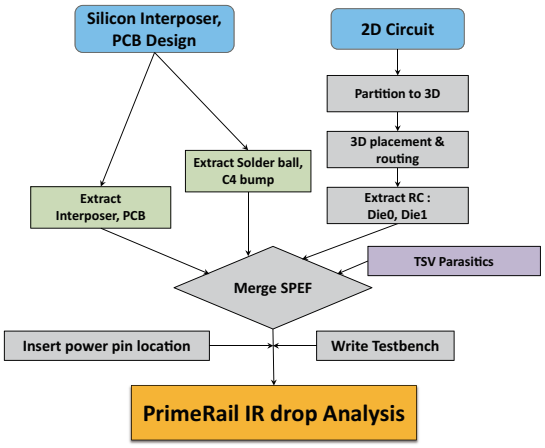

Fig. 5. The proposed co-analysis design flow for IR-drop noise.

of these elements were also extracted using Ansoft Q3D Extractor.

C. Co-Simulation Methodology

Synopsys PrimeRail is a tool which was originally designed to analyze PDN in ICs. It has a limitation of 15 metal layers that can be used. Therefore, if we have an IC design that uses less than 15 metal layers, we can add additional layers for our own purposes.

The proposed co-simulation methodology is shown in Figure 5. First, we generate a 3D IC design using 2D schematic. We partition the 2D circuit into several clusters, and each clusters form each tier on 3D IC. The 3D IC design was performed using Cadence Encounter and our in-house tools [7]. Then, we perform standard cell placement, and power and signal routing. After routing and placement is done, the RC values of each tier are extracted using Synopsys StarRC, and then merged into one SPEF (Standard Parasitic Exchange Format) file. In this file, all the P/G information (power rail, parasitic capacitance...etc) are gathered, including geometry information of each metal layers inside the 3D IC.

Second, we design the PDN of silicon interposer and PCB, and extract the information of each layers and interconnect. The extracted PDN information of interposer and PCB are composed of SPICE

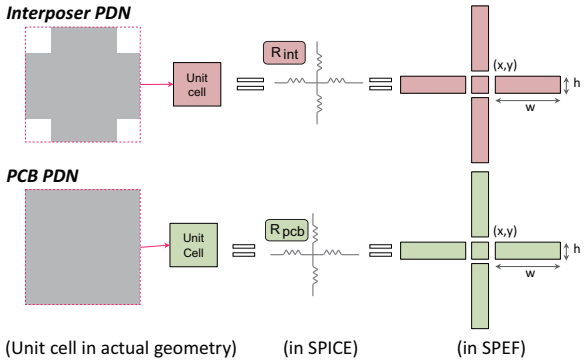

Fig. 6. PDN unit cell translation from physical model to SPEF netlist (a): Silicon interposer, (b): PCB.

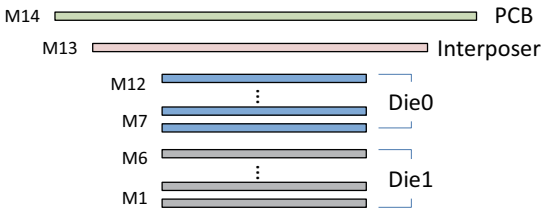

Fig. 7. Metal layers used in Synopsys PrimeRail for IR-drop noise co-analysis.

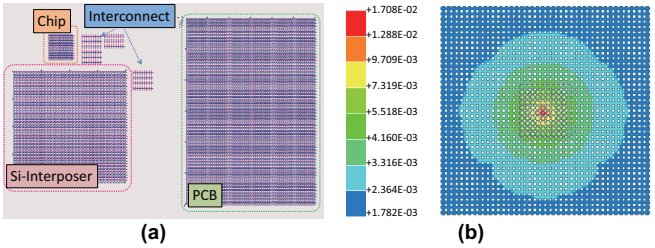

Fig. 8. Validation of the unit cell model in comparison with Ansoft SiWave (a): Agilent ADS (15.86mV, SPICE), (b): Ansoft SiWave (17.08mV).

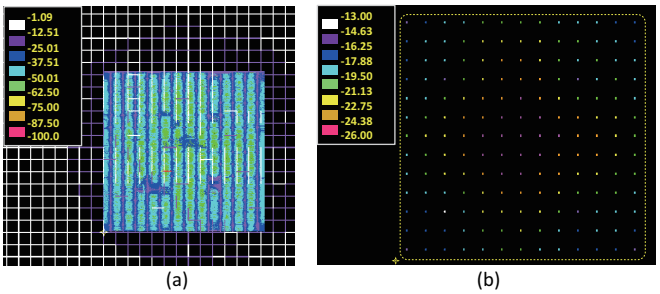

Fig. 9. Co-simulated IR-drop result of FFT3 circuit in Synopsys PrimeRail (a): IC + Si-Interposer + PCB (full system), (b): C4 bumps

elements and nodes connecting them. The extracted information is converted, then added into the same SPEF file which has the 3D IC information. To convert SPICE into the SPEF format, we assign each SPICE elements a virtual width and length, and assign each nodes to a virtual location. Here, the unit cell of a mesh PDN and a plane PDN both look like the same cross shape in SPEF file like Figure 6. Therefore, when these unit cell are combined together, the mesh PDN, and plane PDN would look like the same mesh shape in SPEF file. Using these converted information, we logically connect the IC and the system components in the SPEF file.

The silicon interposer and PCB are assigned to metal layers which has not been used for IC routing. Therefore, it is important to leave a few metal layers empty during IC design. If the IC PDN consumes all 15 metal layers, then there would be no space left to insert the extracted system components in the SPEF file. Figure 7 shows the metal usage of our design. We use 6 metal layers for each tier of IC, one for silicon interposer PDN, and one for PCB PDN.

Third, we insert the SPEF file, and other files into Synopsys PrimeRail, and perform the simulation. We insert a LOC (location) file, which has the layer number and the geometry information where the VDD source is located. A verilog testbench which defines the vector activity of the standard cells is also inserted.

IV. Experimental Results

We first validate the unit cell method to SiWave. Figure 8(b) shows the IR-drop map of silicon interposer flowing 933.6mA in SiWave, and the equivalent SPICE model in Figure 8(a) using Agilent ADS. The maximum IR-drop between SiWave and SPICE was compared, and each voltages were 17.08 mV (SiWave), and 15.86 mV(ADS). We verified that SPICE model shows consistency with SiWave.

In Figure 9(a), the result of a co-simulated PDN is shown. The 3D IC PDN is on the bottom, and the silicon interposer and PCB PDN mesh lays on the top like Figure 7. Figure 10 shows the top-down view of each layers. (a) shows the IR-drop map of the PCB, (b) shows the interposer, and (c), (d) show each tiers. From Figure 10(b), we can see that silicon interposer generates a big IR-drop noise.

We see the importance of co-analysis in Figure 9(b), which describes the irregular IR-drop map of C4 bumps between interposer and IC. Without the gate level switching information, it is impossible to determine which particular spot the IR-drop would be most severe, and which interconnect would supply how much current in which voltage. Figure 9(b) is a valuable result because this describes the actual detail on how much IR-drop is generated on each interconnect, which cannot be anticipated on separate analysis. Therefore, in co-analysis, transistor level power details are very important.

To demonstrate the IR-drop co-simulation results of the system using silicon interposer, we use three FFT (Fast Fourier Transform) circuits which are described in Table I. When separate analysis are done in FFT3 circuit, the IR-drop of the IC only PDN is 122.2mV, and IR-drop of interposer + PCB PDN is 35.0mV. However, when co-analysis is performed both on IC, interposer, and PCB simultaneously, the IR-drop is total of 147.7mV. The IR-drop of co-analysis is 9.5mV smaller than the separate analysis. 6.43% more IR-drop is overestimated in the separate analysis. The overestimation is also due to the non-uniform switching activity of transistors in different locations, which can only be demonstrated in co-simulation. Table II details the results that have been performed with other circuits.

As the power consumption of the system increases, separate analysis overestimate more IR-drop than co-analysis (see Figure 11(a)). By this, we can expect to prevent more overestimated IR-drop by co-analysis when a system with a higher power consumption is analyzed. This is important because IR-drop is tightly connected to the total power consumption. Even with the same IR-drop, the total power loss of a system changes with the total power consumption. With an IR-drop overestimate trend like Figure 11(a), the trend of overestimated power in higher power systems would be the square of Figure 11(a), like Figure 11(b). Therefore, co-analysis is also necessary to estimate power correctly.

The ratio of IR-drop on silicon interposer to the total system is also

TABLE I
DETAILS OF THE CIRCUITS USED IN THIS PAPER

CKT	# of Gates	2D area	3D area	# Power TSV	# GND TSV	Profile
FFT1	140k	864.9 μm × 862.4 μm	639.2 μm × 637.2 μm	36	25	256 point 8 bit precision
FFT2	297k	1274.4 μm × 1272.6 μm	922.3 μm × 920.2 μm	81	64	512 point 8 bit precision
FFT3	616k	1850.5 μm × 1849.4 μm	1329.2 μm × 1327.4 μm	169	144	512 point 16 bit precision

TABLE II
IR-DROP RESULTS COMPARISON

CKT	Power Consumption	IR-drop: IC (PrimeRail)	IR-drop: Si-Int. + PCB (SiWave)	Co-analysis IR-drop (IC + Interposer + PCB PDN)	Maximum IR-drop (ΣSeparate Analysis)	Δ(ΣSeparate analysis - Co-analysis)
FFT1	558 mW	94.9 mV	9.6 mV	103.8 mV	104.5 mV	0.7 mV
FFT2	1027 mW	70.5 mV	17.1 mV	85.1 mV	87.6 mV	2.5 mV
FFT3	2137 mW	122.2 mV	35.0 mV	147.7 mV	157.2 mV	9.5 mV

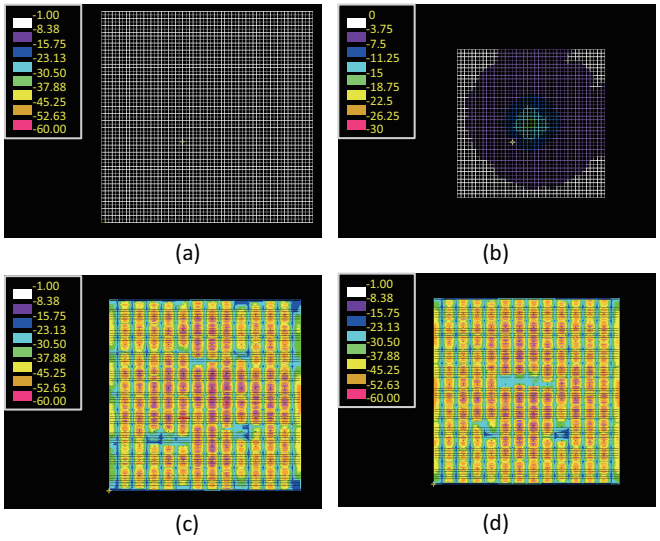

Fig. 10. IR-drop map of each layers on the co-simulated PDN (a): PCB, (b): Si-interposer, (c): Die0, (d): Die1.

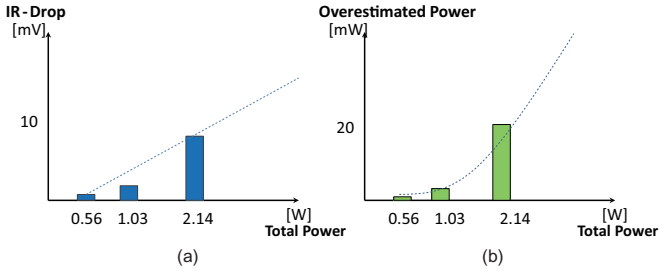

Fig. 11. Benefits anticipation of co-simulation on (a): IR-drop, (b): Power saving.

high, compared to organic package. When using package between IC and PCB, IR-drop is less than a few mV, lower than 3% to the total IR-drop. However, when using silicon interposer, designers must consider a few tens of mV more. This is 16% to the total IR-drop, which is unnecessary in organic packages (see Figure 12).

V. CONCLUSIONS

In this paper, we analyzed the severity of IR-drop noise in silicon interposer, and proposed a methodology which can co-simulate IR-drop noise in the entire system. This co-simulation methodology not only can simulate 2D IC, package, and PCB, but also can

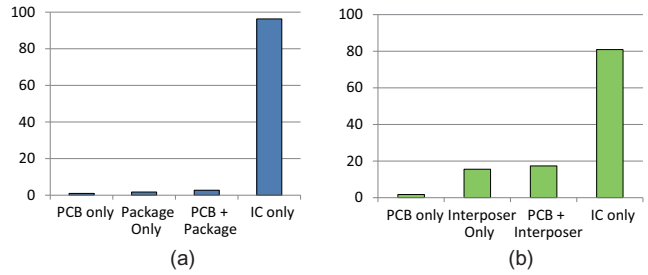

Fig. 12. Ratio of each system components on IR-drop generation (Average of three circuits used on Table II) (a): System with organic package, (b): System with Si-interposer.

simulate a system which consist of 3D IC, silicon interposer, and PCB simultaneously with full transistor level power information. Our study shows that the IR-drop noise in silicon interposer goes up to a few tens of mV, which is more than 8 times organic packages. We also found that the traditional (= separate) analysis overestimates the IR-drop noise significantly and that our co-analysis provides more accurate power noise values.

REFERENCES

[1] J.-S. K. et al, "A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4×128 I/Os Using TSV-based Stacking," in *Proc. Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 496–498.

[2] P. Dorsey, "Xilinx Stacked Silicon Interconnect Technology Delivers Breakthrough FPGA Capacity, Bandwidth, and Power Efficiency," 2010.

[3] J. K. et al, "Chip-Package Hierarchical Power Distribution Network Modeling and Analysis Based on a Segmentation Method," in *IEEE Trans. on Advanced Packaging*, vol. 33, no. 3, Aug. 2010, pp. 647–659.

[4] M. H. et al, "Chip-Package Co-Simulation with Multiscale Structures," in *IEEE Electrical Performance of Electronic Packaging and Systems*, Oct. 2008, pp. 339–342.

[5] H.-H. C. et al, "Power Integrity Chip-Package-PCB Co-Simulation for I/O Interface of DDR3 High-Speed Memory," in *Proc. IEEE Electrical Design of Advanced Packaging and Systems Symp.*, Dec. 2008, pp. 31–34.

[6] L. S. et al, "Power plane SPICE models for frequency and time domains," in *IEEE Electrical Performance of Electronic Packaging*, 2000, pp. 51–54.

[7] D. H. K. et al, "A Study of Through-Silicon-Via Impact on the 3D Stacked IC Layout," in *Proc. IEEE Int. Conf. on Computer-Aided Design*, Nov. 2009, pp. 674–680.